Adaptive Power Regulation and Data Delivery for Multi-Module Implants

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***Abstract*—Emerging applications for implantable devices are requiring multi-unit systems with intrabody transmission of power and data through wireline interfaces. This paper proposes a novel method for power delivery within such a configuration that makes use of closed loop dynamic regulation. This is implemented for an implantable application requiring a single master and multiple identical slave devices utilising a parallel-connected 4-wire interface. The power regulation is achieved within the master unit through closed loop monitoring of the current consumption to the wired link. Simultaneous power transfer and full-duplex data communication is achieved by superimposing the power carrier and downlink data over two wires and uplink data over a second pair of wires. Measured results using a fully isolated (AC coupled) 4-wire lead, demonstrate this implementation can transmit up to 120 mW of power at 6 V (at the slave device, after eliminating any losses). The master device has a maximum efficiency of 80 % including a dominant dynamic power loss. A 6 V constant supply at the slave device is recovered 1.5 ms after a step of 22 mA.**

I. Introduction

Implantable Medical Devices (IMDs) such as pacemakers, cochlear implants and deep brain stimulators have already demonstrated a significant impact to the quality of life of millions of users. These devices interface with the human body by monitoring and/or manipulating activity, and are able to restore function by bypassing dysfunctional organs/pathways. Although the field of IMDs is not new (the first implantable pacemaker dates back to 1959), with the advent of microtechnology and capability this brings, the ambition and reach of such devices are now targeting significantly more advanced disease/treatments. Examples include neural prostheses for depression, eating disorders and epilepsy [1].

Recently, due to improved power efficiency and integration density, the volume per implant and power required per single function have been significantly reduced. We are now seeing new opportunities emerging for closed-loop therapies both in academia and industry. Although the power per given function is generally decreasing, the complexity of the overall systems is increasing (for example including more channels, more capability), and thus the power budget remains a challenge [2]. The limitations imposed by the energy density of implantable batteries, and safe operating conditions for thermal dissipation present challenging trade-offs.

An emerging approach to mitigating such challenges is to employ multi-module, or multi-node implants as illustrated in Fig. 1. By effectively partitioning the system into physically-separated units, with the different functions located at different sites. The most common configuration is to have one relatively large central implant (CI), typically implanted in the upper chest that houses the battery, processing and communication functions. Smaller peripheral implant (PI) units can then be located close to the target interface sites. One good example is the Networked Neuroprosthesis System (NNP) developed at Case Western Reserve University [3]. This allows for a single CI unit to be connected to multiple PI units via a digital wireline interface. As this however is targeted to Functional Electrical Stimulation (FES) applications, the required number of stimulation and/or recording channels (and bandwidth) is limited.

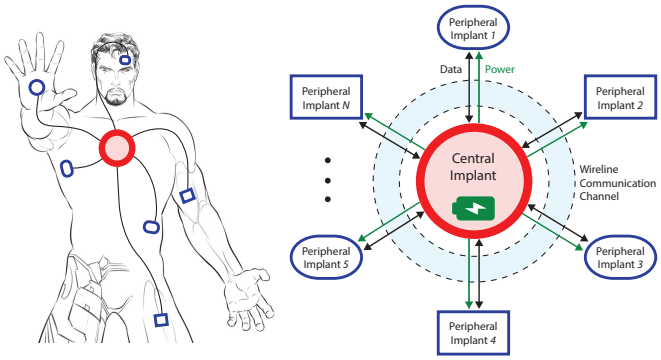

Fig. 1. Concept of wired intrabody multi-module Implants.

The work presented in this paper has been developed as part of the CANDO project (www.cando.ac.uk). CANDO aims to develop an implantable device to provide a closed-loop therapy for focal epilepsy. The CANDO system consists of one CI unit for control and power and multiple PI units for bidirectional neural interfacing [4], [5]. The different units are connected via a shared implantable lead.

This paper describes a new method developed to transmit and adaptively regulate power (whilst also communicate data) from a single CI to multiple PIs through a wired communication channel. The rest of this paper is organised as follows: Section II describes the dynamic power regulation concept; Section III describes the system architecture and circuit implementation; Section IV presents measured results; and Section V concludes the work.

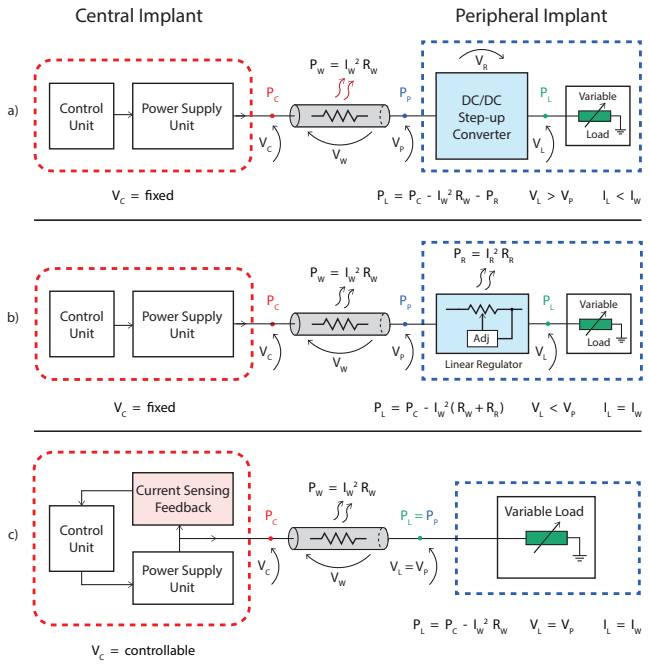

Fig. 2. Three methods for power delivery, utilising: (a) DC/DC conversion; (b) linear regulation; (c) adaptive, closed-loop regulation.

II. Intrabody Power Transmission

The need to reliably transmit power from a single CI to multiple PI modules poses certain challenges. It is essential that any configuration adopted is safe, reliable and efficient. For these reasons the majority of such links are wire-based despite there being significant effort in the community to develop various wireless modalities. Even so, wireline transmission poses certain challenges – the number of wires must be kept to a minimum, DC voltages must be avoided, and there is a need to achieve full duplex communication.

For the system to operate reliably, any transmission scheme must guarantee uninterrupted power delivery with a constant supply (V_L) irrespective of battery level, a load that changes with configuration, and a dynamic current profile.

Different methods for delivering dynamic power through an implanted cable have been reported in the literature [6] [7]. The power regulation typically occurs within the PI units, employing either DC/DC converters and/or linear voltage regulators. For systems using DC/DC converters (Fig. 2(a)) it is possible to generate boosted supply voltages, albeit sacrificing current supply and increasing complexity (silicon area and/or off-chip discrete components). Using linear regulators on the other hand provide a simple, compact solution at the expense of efficiency. Furthermore, it is essential to provide a significantly higher voltage level to compensate for the regulator drop (Fig. 2(b)). Both methods require additional circuitry at the PI module, increasing power and adding to the inevitable IR loss on the wires of the communication channel.

The method proposed herein mitigates the need to coarse regulation within the PI modules, by instead adaptively regulating the power within the CI unit through closed-loop feedback. By continually sensing the current supply (I_W) within the CI, the IR drop across the cable can be calculated (Fig. 2(c)). The CI output voltage V_C can subsequently be dynamically adjusted based on the instantaneous load V_C to ensure a constant voltage level is received at the PI modules. As a result, the power loss in the delivery process is due exclusively to the IR drop across the wired link.

This can be extended to multiple identical PI modules – in this case the current measured by the feedback path corresponds to the sum of the load currents of all the PIs, with the voltage received being common to all units.

III. System Implementation

As mentioned previously, the key requirements for the system implemented are safety, reliability and efficiency. To reduce the risk of corrosion due to DC electric fields, in addition to a failsafe in the event of a conductor breakage, DC blocking capacitors are used. The system implemented uses an implantable lead with 4-wires organised as two differential wire pairs: one for power and downlink data transmission (CI to PIs), and the other for uplink data transmission (PIs to CI). The interface is AC-coupled using phase (Manchester) encoding for data. In our application, the CI unit needs to deliver a maximum current of 20 mA at 6 V to all the PI modules. The communication link is a lossy cable with a total resistance for a pair of wires of 220 Ω (adapted from [8]). PI to CI data communication is to have a maximum data rate of 1.6 Mbps, and 100 kbps vice versa. More details on the interface can be found in [8], [9].

The system presented herein has been implemented on a PCB to interface between an FPGA-based controller and the 4-wire implantable lead. It receives commands and data packets through a UART connection from a PC-based GUI and updates the downlink and uplink modules as necessary. The top level architecture of this system is divided into five main blocks: (1) power management; (2) downlink drivers; (3) feedback; (4) uplink receivers; and (5) digital controller. The circuit implementation of the 4-wire PCB interface is shown in Fig. 3.

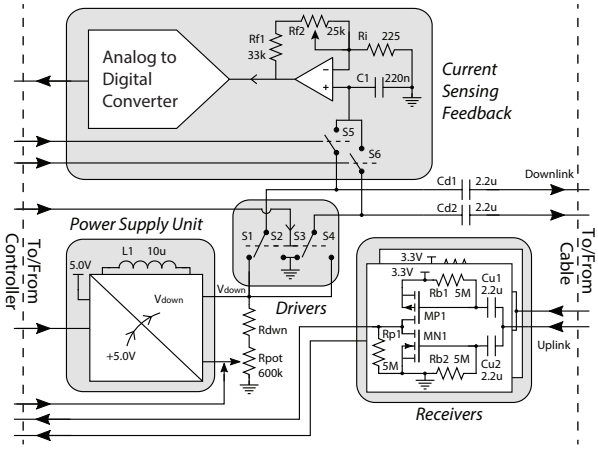

Fig. 3. Top level circuit schematic for the power management and data transceiver within the CI unit.

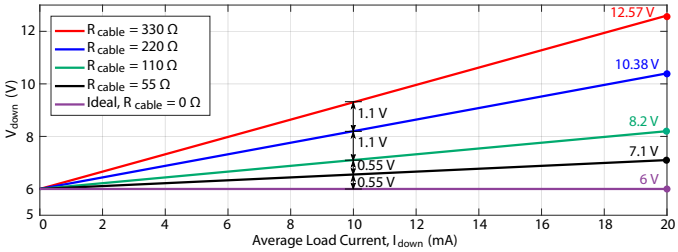

Fig. 4. V_{down} vs. I_{down} for different values of R_{cable}.

A. Power Management

The voltage, V_{down}, required to maintain a constant 6 V supply to the PI modules, depends on the current flowing through the communication link. This is described in Eqn 1.

$$V_{down} = 6\,V + I_{down} R_{cable} \tag{1}$$

Considering different values for R_{cable} gives the characteristics shown in Fig. 4. These show that the choice of cable is critical since this directly affects power losses in the communication link and thus the efficiency of the whole system. For an R_{cable} of 220 Ω, a DC-DC converter was chosen (LTC3130) so as to be able to supply a voltage (at the CI unit side) of between 6 and 10.5 V from a 5 V supply. The output voltage of this boost converter is set by a potential divider connected to the output pin (V_{down}), feedback pin, and ground. In our system, this is provided through digital potentiometers that are controlled by the FPGA. Three 200 $k\Omega$, 32-tap, digital potentiometers are here connected in series, ensuring a high resistance so as to minimise power consumption.

B. Downlink Drivers

This was implemented by using four SPST (2 NO, 2 NC) switches, S1 to S4 (available in one package as the MAX4679), connected as one SPDT switch per pair (1 NO, 1 NC) with inverted input connections (V_{down} and GND). Alternating between V_{down} and GND, these switches deliver power and Manchester encoded data (at 100 kbps) concurrently through the cable. To reduce the power losses at the chest unit it is important to have switches with a very low on-resistance. Also break-before-make circuitry is essential, to ensure that the normally closed switch is disconnected before connecting the normally open switch (and vice-versa). This is required to avoid an instantaneous short circuit at the transitions (i.e. between V_{down} and GND).

C. Current Sensing Feedback

To be able to adjust V_{down} depending on the load current, a current sense circuit is required. This is usually achieved by measuring a voltage drop across a current sense resistor placed in series with the load which results in an additional loss of power. In this case, however, the voltage drop across the on-resistance of the switches was measured instead. To avoid dealing with high voltages, low side current sensing was implemented. This required two SPST switches (S5 and S6) so as to multiplex the driver output that is connected to ground. The switch outputs are then sampled by a hold capacitor, and an amplifier to make use of the full scale input range of the ADC. The value for the hold capacitor was set so as to reduce the voltage droop from leakage currents, limit the change in voltage from charge injection, and to ensure that the capacitor charges to the set voltages within the available minimum time.

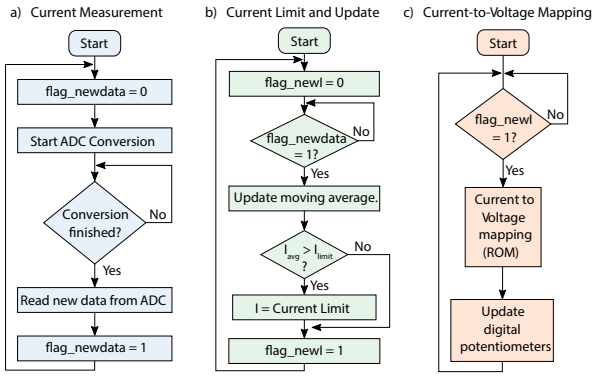

Fig. 5. Digital control algorithms for evaluation and feedback (implemented as a finite state machine on FPGA).

D. Uplink Receivers

For the uplink receiver, a CMOS inverter is used for each wire so as to be able to monitor each line separately. The gate of each MOSFET is biased at either 3.3 V or ground to make sure that both MN_x and MP_x are off during idle operation (i.e. no activity on uplink). Thus for a valid output value during idle operation (as both transistors are off), a pull-down high-value resistor is connected to the output of the inverter. During normal operation, the received uplink signal is superimposed on the DC gate voltage by a capacitor. The inverter then converts this signal to an LVCMOS33 digital signal which is then processed by the FPGA to decode the data received.

E. Digital Controller

This was implemented in VHDL on an IGLOO Nano FPGA board (AGL250V2-VQG100 Starter Kit) consisting of several modules to control and monitor each part of the system based on the commands received through UART. During normal operation, voltage regulation is achieved by first requesting a new acquisition from the ADC to sample the current flowing

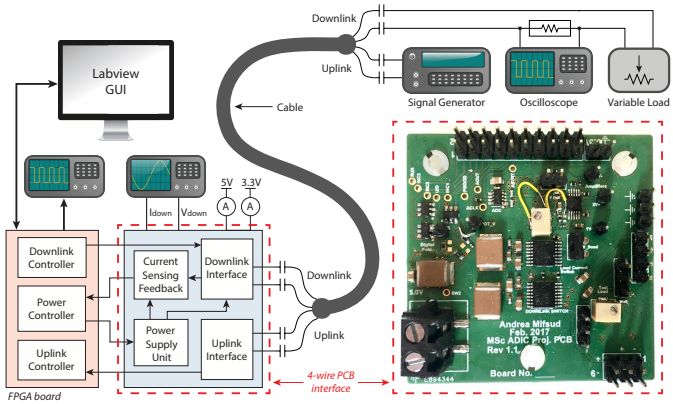

Fig. 6. Experimental setup and prototype 4-wire interface board within CI.

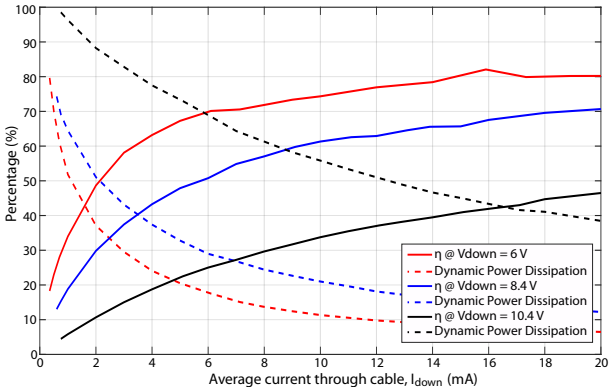

Fig. 7. System efficiency for different values of V_{down}, and load current.

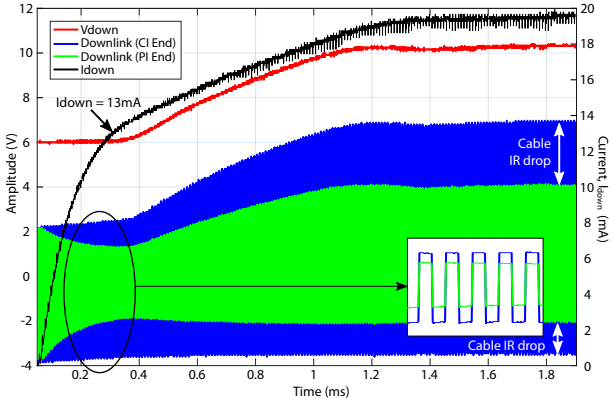

Fig. 8. System step response. $I_{dwn} = 22$ mA at $V_{down} = 10.4$ V, $R_L = 470\,\Omega$

through the cable. Once the new sample is received, an 8-sample moving average is updated, and the result mapped to a voltage by a ROM which stores this mapping based on specific parameters of the system (see Fig. 5). This voltage is then converted into a number of taps, for the digital potentiometers to be updated, thus updating V_{down}. For data communication, data is sent to the PIs by controlling the drivers as required, and any new data received from the PIs is sent through UART. During idle operation, the downlink drivers are switched at a frequency of 100 kHz to keep transmitting power, whilst sending a logic low.

IV. Measured Results

The CI power delivery and downlink data communication was tested for various load conditions and V_{down} values using a dummy resistive load [8], as shown in Fig. 6. Two tests were carried out, one to determine the efficiency of the PCB based chest unit, and another for the worst case step-response of the system. Key system specifications are summarised in Table I.

TABLE I
Achieved System Specifications

Function	Parameters	Value
Power	V_{in}, $I_{down,max}$ $V_{down,min}$, $V_{down,max}$	5 V, 20 mA 5.5 V, 10.4 V
Feedback	F_s, Resolution, $t_{s,max}$	100 ksps, 8 bits, 1.5 ms
Driver	AVDD, DVDD t_r, t_f, Datarate	5.5-10.4 V, 3.3 V 250 ns, 100 ns, 100 kbps
Receiver	DVDD, $Datarate_{max}$	3.3 V, 1.6 Mbps

The measured results for efficiency are shown in Fig. 7. This shows that the efficiency increases when V_{down} decreases and(/or) when the load current, I_{down} increases. The main loss in the system is found to be dynamic power dissipation of the downlink drivers, measured at 8.6 mW for V_{down} of 6 V, and increasing by an order of magnitude at 10.4 V.

The stability of the system was tested by applying a step in I_{down} of 22 mA as illustrated in Fig. 8. Initially, the current settles at approximately 13 mA, increasing linearly as V_{down} increases to compensate for the voltage drop on the cable, until the current measurement saturates at 20 mA. Thus, the measured worst case settling time of the system is 1.5 ms.

V. Conclusion

This paper has presented a novel adaptive power delivery method with full duplex data communication for a wired multi-module implantable device. A prototype system testing the circuit implementation of the central implant has been implemented occupying 5×5 cm on a PCB substrate. The proposed power management system can however, deliver up to 120 mW power at 6 V (to the peripheral implant) superimposed on a phase encoded serial bitstream with datarate of 100 kbps (downlink). The maximum efficiency achieved for this implementation is 80%, with the dynamic power dissipation of the drivers being the dominant source of power loss across all load current ranges. Measured results show that a worst case recovery for a 6 V constant supply at the peripheral implant takes 1.5 ms for a step of 22 mA. Uplink communication is achieved through a separate pair of wires using phase encoding at a maximum datarate of 1.6 Mbps.

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References

[1] S. Bhunia *et al.*, *Implantable Biomedical Microsystems: Design Principles and Applications*. Elsevier, 2015.
[2] T. Lehmann *et al.*, "Low-power circuit structures for chip-scale stimulating implants," in *Proc. IEEE APCCAS*, 2012, pp. 312–315.
[3] B. Smith *et al.*, "Development of an implantable networked neuroprosthesis," in *Proc. IEEE/EMBS Neural Engineering*, 2005, pp. 454–457.
[4] H. Zhao *et al.*, "A CMOS-based neural implantable optrode for optogenetic stimulation and electrical recording," in *Proc. IEEE BioCAS Conference*, 2015, pp. 1–4.
[5] R. Ramezani *et al.*, "An optrode with built-in self-diagnostic and fracture sensor for cortical brain stimulation," in *Proc. IEEE BioCAS Conference*. IEEE, 2016, pp. 392–395.
[6] L. H. Jung *et al.*, "Towards a chip scale neurostimulator: System architecture of a current-driven 98 channel neurostimulator via a two-wire interface," in *IEEE EMBS Conference*, 2011.
[7] N. Tran *et al.*, "A complete 256-electrode retinal prosthesis chip," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 751–765, 2014.
[8] S. S. Ghoreishizadeh *et al.*, "Four-wire interface ASIC for a multi-implant link," *IEEE Transactions on Circuits and Systems I*, pp. 1–12, 2017.
[9] S. S. Ghoreishizadeh *et al.*, "A 4-wire interface SoC for shared multi-implant power transfer and full-duplex communication," in *Proc. IEEE LASCAS*, 2017.