Power Quality and Efficiency Improvements for Transformerless Grid Connected PV Inverters

by

Leslie Alan Bowtell, MEng, BEng, RPEQ

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Abstract

There is currently significant growth in the number of residential scale grid-connected photovoltaic (PV) systems. Generally, if environmental costs are not accounted for, the cost of generation from PV sources remains high compared to conventionally generated electricity. There is, therefore, a strong incentive to reduce the cost of PV systems and improve their efficiency while satisfying injected power quality standards. The focus has been on the power electronic single phase converter bridge which is typically used as interface between the DC output of the PV panels and the terminals of the AC network. One of the two main objectives was to investigate the possibility of operating an inverter connected to the AC grid without an interfacing power transformer, while keeping DC injection into the grid below levels specified by Australian and International Standards. A low cost method of controlling the DC offset content of the current injected into the AC mains has been proposed. A mathematical model of the DC offset controller has been developed and experimentally validated. A design procedure for the controller has also been developed. The second objective was to investigate the dependence of efficiency on inverter switching strategies such as bipolar and unipolar switching. It was confirmed by specially designed tests that unipolar switching meant significantly lower switching losses when compared with bipolar switching. However, the quality of current injected into the AC mains in the case of unipolar switching was not considered acceptable because of significant current distortion near the AC mains voltage zero crossing. A new method of inverter switching has been proposed which exploits the efficiency advantage of unipolar switching while avoiding the problem of current distortion. The main outcomes of this project are a DC offset controller which allow transformerless operation and an inverter switching strategy that results in significantly reduced switching losses while maintaining the quality of injected current. Implementation of the proposed DC offset controller and inverter switching strategy will result in both capital cost savings and higher conversion efficiency.

Certification of Thesis

I certify that the ideas, experimental work, results, analyses, software and conclusions reported in this dissertation are entirely my own effort, except where otherwise acknowledged. I also certify that the work is original and has not been previously submitted for any other award, except where otherwise acknowledged.

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Signature of Candidate **Date**

ENDORSEMENT

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Signature of Supervisor **Date**

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Signature of Supervisor **Date**

Acknowledgments

I wish to convey my most sincere thanks to my supervisor Dr Tony Ahfock for his help throughout this project. He has provided excellent supervision, skilful guidance and tactful mentoring from the inception of this project right through to the compilation of this thesis. He has made this a rewarding although sometimes challenging experience for which I am sincerely grateful to have had such a gifted and fervent mentor.

I wish also to thank USQ's technical staff, in particular Mr Don Gelhaar for his assistance in the Laboratory, and for his kind words of encouragement.

It also goes without saying that without the continuous support and motivation received from my family, particularly my wife Shelley, that this dissertation would not have been possible. Lastly but certainly not least I wish to thank my three children for the tolerance and patience that they have shown me over the last three years and for foregoing all the weekend activities for which I am now once again available.

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i_i	inverter output current
i_c	DC offset correction current (output of the DC offset controller)
i_{comp}	component of i_{ref} to compensate for switching delay(see figure 4.28)
i_o	inherent DC offset content of the inverter output
i_p	output current from PV array
i_{pr}	active power component of current reference
i_{qr}	reactive power component of current reference
i_{ref}	current reference to hysteretic current controller
i_s	AC mains or grid supply current
k_c	DC bus voltage sensor constant (V/V)
k_e	proportional gain of analogue PI controller
k_h	Hall effect current sensor constant (V/A)
k_m	coupling factor of 1:1 inductor pair (see figure 6.2)
k_p	Hall effect current sensor on DC side(V/A)
k_s	AC mains voltage sensor constant (V/V)
k_z v_z	= k_{d1} or k_{d2} = constant integration rate of the integral element of the digital DC offset PI controller
t_{dr}	switching delay on current rise (see figure 4.23)
t_{df}	switching delay on current fall (see figure 4.23)
τ_d	time constant of first order digital filter used in the digital DC offset sensor
τ_f	RLLC DC offset sensor filter equal to R_2C_2 (see figure 6.1)
τ_f	time constant of each nominally identical stage of the dual RC DC offset sensor
τ_m	time constant of the DC Bus voltage sensor for maximum power tracker
τ_i	analogue PI controller integration time constant
τ_p	L/R ratio of each inductor making up the RLLC DC offset sensor
T_{bi}	Mixed-mode current controller bipolar operation time
T_{A+}	Inverter H-Bridge IGBT, top left (see figure 4.4)
T_{A-}	Inverter H-Bridge IGBT, bottom left (see figure 4.4)
T_{B+}	Inverter H-Bridge IGBT, top right (see figure 4.4)
T_{B-}	Inverter H-Bridge IGBT, bottom right (see figure 4.4)

v Inverter output voltage

v_f input voltage across dual stage RC DC offset sensor

v_c PV Array bus voltage

v_m digitally filtered PV Array bus voltage for MPPT

v_i integrator output voltage in analogue PI controller

v_L AC component of v_f (defined above)

v_o output voltage of dual stage RC DC offset sensor (see figures 6.4, 6.8)

v_{ref} reference DC bus voltage

v_s Mains or grid supply AC voltage

v_z output voltage of digital filter in digital DC offset controller

v_1 output of first stage of dual stage RC DC offset sensor (see figure 6.4)

D_{A+} Inverter H-Bridge free-wheeling diode, top left (see figure 4.4)

D_{A-} Inverter H-Bridge free-wheeling diode, bottom left (see figure 4.4)

D_{B+} Inverter H-Bridge free-wheeling diode, top right (see figure 4.4)

D_{B-} Inverter H-Bridge free-wheeling diode, bottom right (see figure 4.4)

ACRONYMS

EMC	Electromagnetic Compatibility
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
MPPT	Maximum Power Point Tracking
PV	Photo-Voltaic
PWM	Pulse Width Modulation
RLLC	DC offset sensor based on 1:1 coupled inductor (see figure 6.2)
RFI	Radio Frequency Interference
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supplies
VSVC	Voltage sourced voltage controlled inverter
VSCC	Voltage sourced current controlled inverter

Publications

The following publications are the direct outcomes of this research project:

A.Ahfock and L.Bowtell, "DC Offset Elimination in a Transformerless Single Phase Grid-Connected Photovoltaic System*", Australasian Universities Power Engineering Conference, 'AUPEC 06'*, Victoria University, Melbourne, 2006.

L.Bowtell and A.Ahfock, "Comparison Between Unipolar and Bipolar Single Phase Grid-Connected Inverters for PV Applications"*, Australasian Universities Power Engineering Conference, 'AUPEC 07'*, Curtin University, WA, 2007.

L.Bowtell and A.Ahfock, "Direct Current Offset Controller for Transformerless single-Phase Photovoltaic Grid-connected Inverters", *IET Renewable Power and Generation*, vol. 4, iss. 5, pp. 428-437, 2010.

L.Bowtell and A.Ahfock, "Dynamic Analysis of a DC Offset Controller for Grid-Connected Inverters"*, Australasian Universities Power Engineering Conference, 'AUPEC10'*, Christchurch, NZ, 2010.

A.Ahfock and L.Bowtell, "Mixed Mode Switching of Single-phase Grid-connected Photovoltaic Inverters", *IET Renewable Power and Generation,*(submitted, Nov 2010).

Chapter 1: Introduction

1. Justification for the Research Project

The possibility of severe climate change caused by fossil fuel consumption and the social consequences of depletion of accessible fossil fuel reserves are now of major concern. As a result, the search for more sustainable energy resources is being intensified. On a national scale, the direct conversion of sunlight into electricity (photovoltaic generation) is a relatively small but growing part of the electrical energy mix. Electrical energy suppliers have to accommodate photovoltaic (PV) system connection to their network.

As shown in figure 1.1, a grid connected PV system consists mainly of a set of solar panels and a DC to AC converter. The solar panels convert light energy into direct current (DC). Electrical energy can be fed into the electricity network in alternating (AC) form only. Hence the role of the DC to AC converter (that is, the inverter) is to convert direct current from the solar panels to alternating current (AC) at the standard frequency of 50 Hz before injecting it into the AC network.

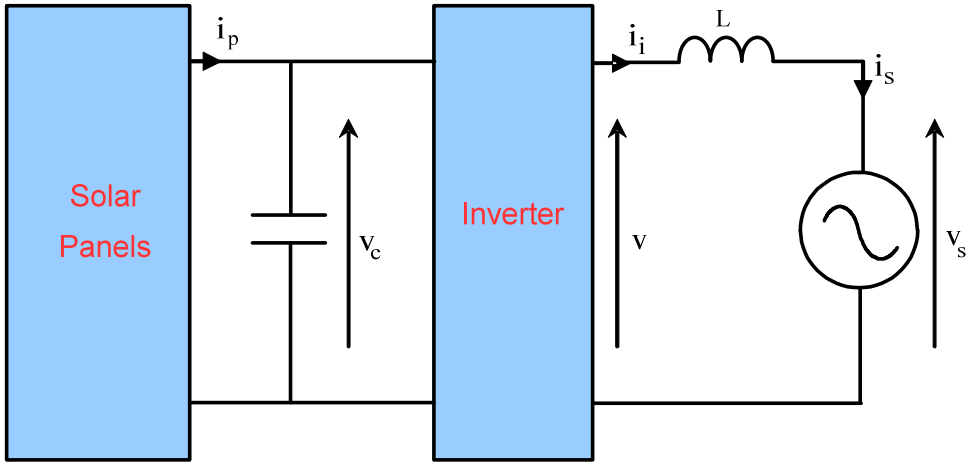


Figure 1.1: Essential Components of a Grid-Connected Photovoltaic System

By definition, the highest quality alternating current (AC) would be one which is purely sinusoidal, that is, a current which is a sinusoidal function of time. In practice, however, even the very best inverter will not supply a purely sinusoidal current. The undesirable effects of non-sinusoidal current injection can be serious. For that reason AC network operators impose limits on the degree of distortion away from the ideal sinusoidal current. In particular they specify a limit on the direct current (DC) content of the inverter output, on the lower order harmonic content and on the higher order harmonic content. The low frequency harmonic content typically consists of current components with frequencies equal to multiples of the standard frequency of 50 Hz up to about 1 kHz. Harmonic content at higher frequencies are also present. These are associated with the switching frequencies of devices within the inverter. Limits are also imposed on electromagnetic interference (EMI) caused by fast switching within the inverter.

Apart from the quality of the AC current being injected into the AC network and the level of EMI, two other important factors need to be considered. These are cost and energy conversion efficiency. Cost, conversion efficiency, quality of injected current and the level of EMI generation are not independent factors. For example many suppliers of grid-connected PV systems include a 50 Hz transformer between the output of the inverter and the AC supply so that, among other things, the requirement on DC injection is met. It is well-known that DC current does not flow through a transformer. Thus, while the 50 Hz transformer helps meet injected current quality requirements it adds to system mass, volume, cost and energy losses. Similarly some inverter control or switching strategies lead to better current waveform quality but at the expense of reduced efficiency.

As will be elaborated in the literature review (section 3), very little has been published on DC injection by grid-connected inverters. While feedback control has been suggested for elimination of DC injection, no mathematical models have been proposed for dynamic performance evaluation of DC offset control loops. Similarly, while there are claims that some transformerless inverter switching methods may offer efficiency advantages, to the author's knowledge there is little published physical evidence to support these claims.

1.2 Aim and Objectives

The aim of this work is to select a control and switching strategy for an inverter which is to be used as part of a transformerless single-phase grid-connected PV system, so as to economically achieve better overall efficiency while satisfying operational requirements, in particular those relating to quality of supply.

The objectives are:

(1) To review different inverter switching strategies and select one on the basis of efficiency, power quality and cost.

(2) To develop a cost effective DC offset control system for the grid connected PV system that would keep the level of DC injection into the AC network below the Australian Standard requirement;

(3) To develop mathematical models that would help with design and implementation of the DC offset controller and other control loops used within the inverter system.

1.3 Outline of Dissertation

Chapter 2 of the dissertation is a review of existing inverter control and switching strategies. Their respective advantages and disadvantages, with specific reference to single phase photovoltaic systems, are discussed. This review, together with the literature review carried out in Chapter 3, has helped with the search for inverter control features that could potentially improve performance and cost. Chapter 3 also provides justification for the adopted methodology for this research project.

Chapter 4 is devoted to inverter switching. A detailed comparison of unipolar and bipolar switching is provided. Test results are presented which confirm that significant reduction in switching losses is possible if unipolar switching is adopted. However, there is unacceptable current distortion near the AC supply voltage zero crossing. It is demonstrated that appropriate combination of bipolar and unipolar switching techniques can achieve the switching loss reduction whilst avoiding the current distortion effects at the zero crossing of the AC supply voltage waveform.

Chapter 5 details the active power balance controller. The controller incorporates PV array maximum power tracking and DC bus voltage control.

Chapter 6 presents the details of three DC offset controllers. The first two are implemented using discrete analogue devices and are essentially PI controllers with two different types of sensing arrangements. The third one is digitally implemented. Mathematical models are developed and these are validated by test results. Chapter 6 also provides both theoretical and practical confirmation that there is no interaction between the DC offset control loop and either of the other two control loops.

Chapter 7 concludes the dissertation. It presents a summary of research achievements together with a discussion on their significance.

1.4 Summary of Outcomes

A single phase transformerless grid-connected photovoltaic system has been implemented and tested. Listed below are a number of its features which are considered to be novel and/or significant.

(a) It incorporates a DC offset controller, which can be of analogue or digital design.

(b) It can operate, as a four quadrant AC current controller, in a mixed unipolar/bipolar switching mode. It has been proven by experiment that the mixed switching method retains the efficiency advantage of unipolar switching without the typical current distortion that occurs near the AC supply voltage zero crossing.

(c) Its control system requires modest speed and memory capabilities as typically found in small industrial programmable controllers.

(d) Modulation of the current reference signal in response to insolation level is carried out using a digital potentiometer, thus avoiding analogue multiplication or the requirement for fast digital multiplication within the programmable controller.

The following publications are the research outcomes:

(1) A.Ahfock and L.Bowtell, "DC Offset Elimination in a Transformerless Single Phase Grid-Connected Photovoltaic System*", Australasian Universities Power Engineering Conference, 'AUPEC 06'*, Victoria University, Melbourne, 2006.

(2) L.Bowtell and A.Ahfock, "Comparison Between Unipolar and Bipolar Single Phase Grid-Connected Inverters for PV Applications"*, Australasian Universities Power Engineering Conference, 'AUPEC 07'*, Curtin University, WA, 2007.

(3) L.Bowtell and A.Ahfock, "Direct Current Offset Controller for Transformerless single-Phase Photovoltaic Grid-connected Inverters", *IET Renewable Power and Generation*, vol. 4, iss. 5, pp. 428-437, 2010.

(4) L.Bowtell and A.Ahfock, "Dynamic Analysis of a DC Offset Controller for Grid-Connected Inverters"*, Australasian Universities Power Engineering Conference, 'AUPEC10'*, Christchurch, NZ, 2010.

(5) A.Ahfock and L.Bowtell, "Mixed Mode Switching of Single-phase Grid-connected Photovoltaic Inverters", *IET Renewable Power and Generation,*(submitted, Nov 2010).

Chapter 2

Common Inverter Switching Control Strategies

2.1 Inverter Control Strategies

There are a large number of inverter configurations that could be used in grid connected photovoltaic systems. Different switching and control strategies could be adopted with each one of those configurations. It would not be possible to consider all possible combinations in a single document such as this one. Only those configurations with highest potential to achieve the aim of this research project are covered in detail. The purpose of this chapter is to provide background information that will assist with understanding of the reasons behind the short-listing of particular inverter configurations and control strategies.

2.2 Voltage versus Current Controlled

A number of inverter control techniques can be used to inject power into the AC network. Two general possibilities are the voltage sourced voltage controlled inverter (VSVC) and the voltage sourced current controlled inverter (VSCC). The term 'voltage sourced' implies that the DC input to the inverter (v_c in figure 1.1) is essentially constant, at least within the time frame of a few inverter output cycles. Current sourced inverter systems are not normally used in photovoltaic applications and are not considered here.

In the case of voltage control, the output voltage of the inverter (v_i in figure 1.1) is directly controlled. It is normally in the form of a sine-coded pulse width modulated (PWM) voltage, unipolar or bipolar. Assuming the power electronic switches in the inverter were

perfect, as shown in figure 2.1, unipolar voltage levels in the positive half cycle is (v_c) and 0 and in the negative half cycle they are ($-v_c$) and 0. In the bipolar case, as shown in figure 2.2, voltage levels in any of the half cycles, positive or negative, are ideally (v_c) and ($-v_c$). In practice the number of pulses per inverter half cycle (or inverter switching frequency) is much higher than shown in figures 2.1 or 2.2.

In voltage control mode the rms value and phase of the inverter output voltage is directly controlled and the inverter output current will assume a magnitude, waveshape and phase that would depend on the AC network Thevenin voltage and the total series impedance that it experiences.

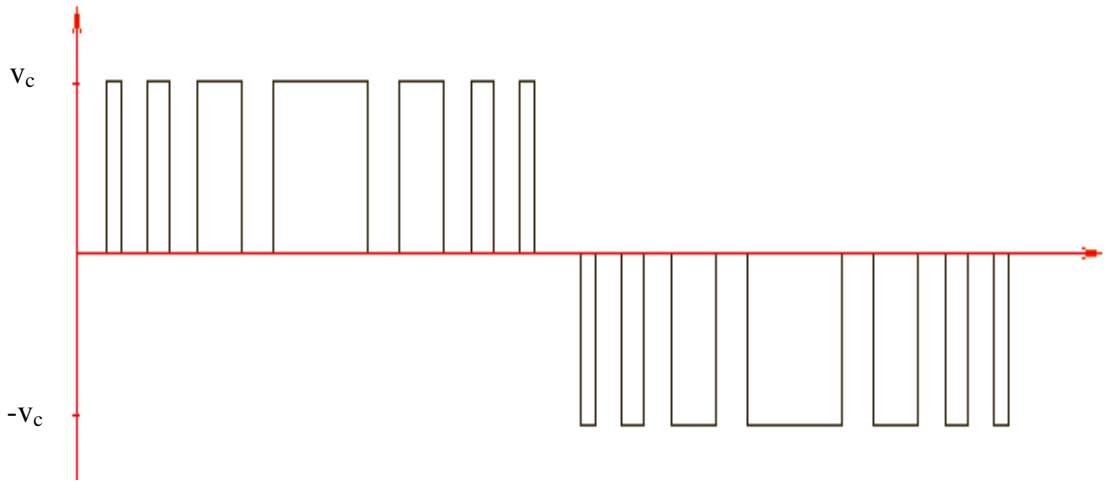


Figure 2.1: Output Voltage from Unipolar Switched Inverter

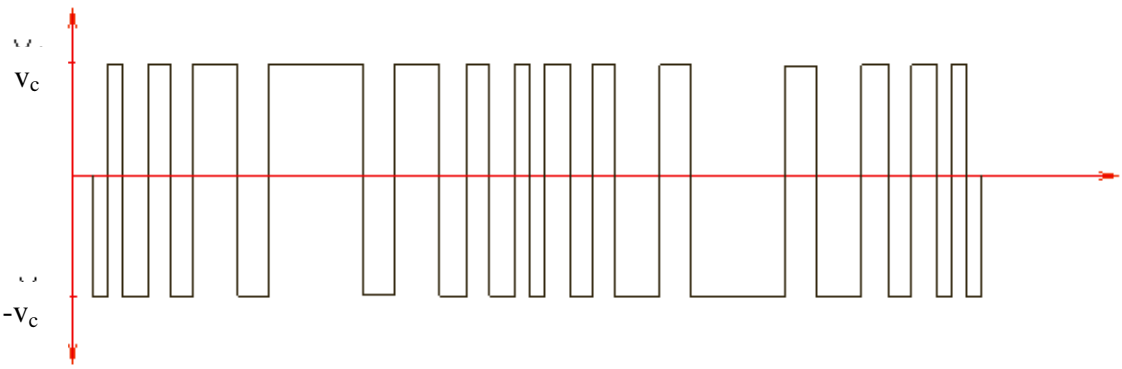


Figure 2.2: Output Voltage from Bipolar Switched Inverter

In the case of current control, the output current of the inverter (i_i in figure 1.1) is directly controlled. Typically a hysteretic controller is used. If the current falls outside a limit of the hysteretic band then the inverter power electronic devices are switched so that the current returns inside the band. A typical output current waveform from a current controlled inverter is shown in figure 2.3. The aim is to force the output current (i_i) to follow the reference current (i_{ref}).

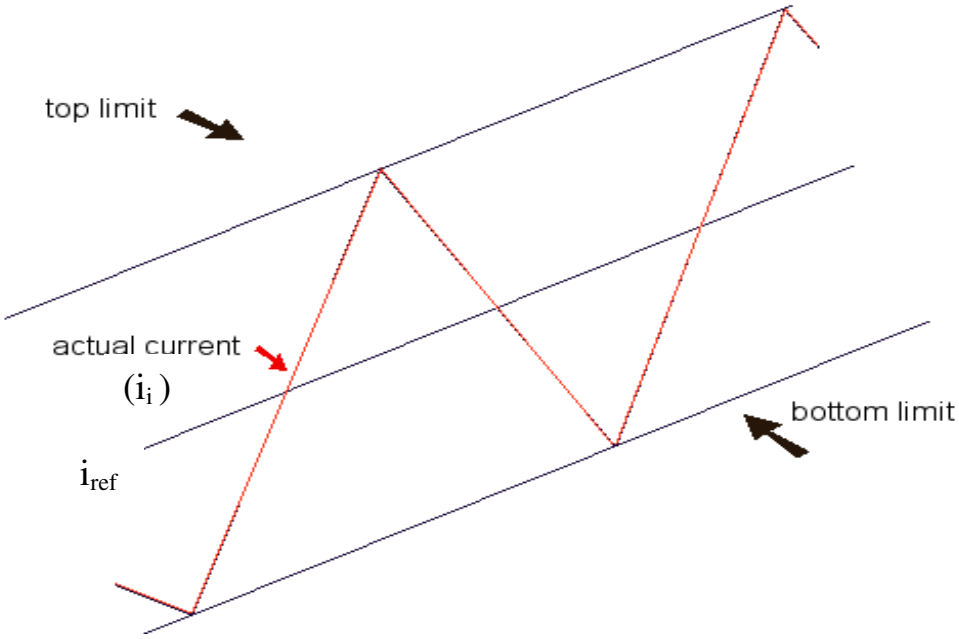


Figure 2.3: Typical Unfiltered Output Current of a Current Controlled Inverter

In general voltage sourced voltage controlled (VSVC) inverters have been more popular in stand-alone systems as they tend to be less expensive in this application. However, meeting the Australian Standard[1] requirements on DC level injection with grid-connected transformerless voltage controlled inverters is inherently more difficult with VSVC inverters. With current controlled inverters synchronisation with the AC mains presents no difficulty and DC content is significantly easier to control. The decision was made, therefore, to consider only voltage sourced current controlled (VSCC) inverters for this project.

2.3 Bipolar versus Unipolar Switching

The inverter shown in figure 2.4 is grid-connected, voltage-sourced, and current-controlled. It may be unipolar switched or bipolar switched.

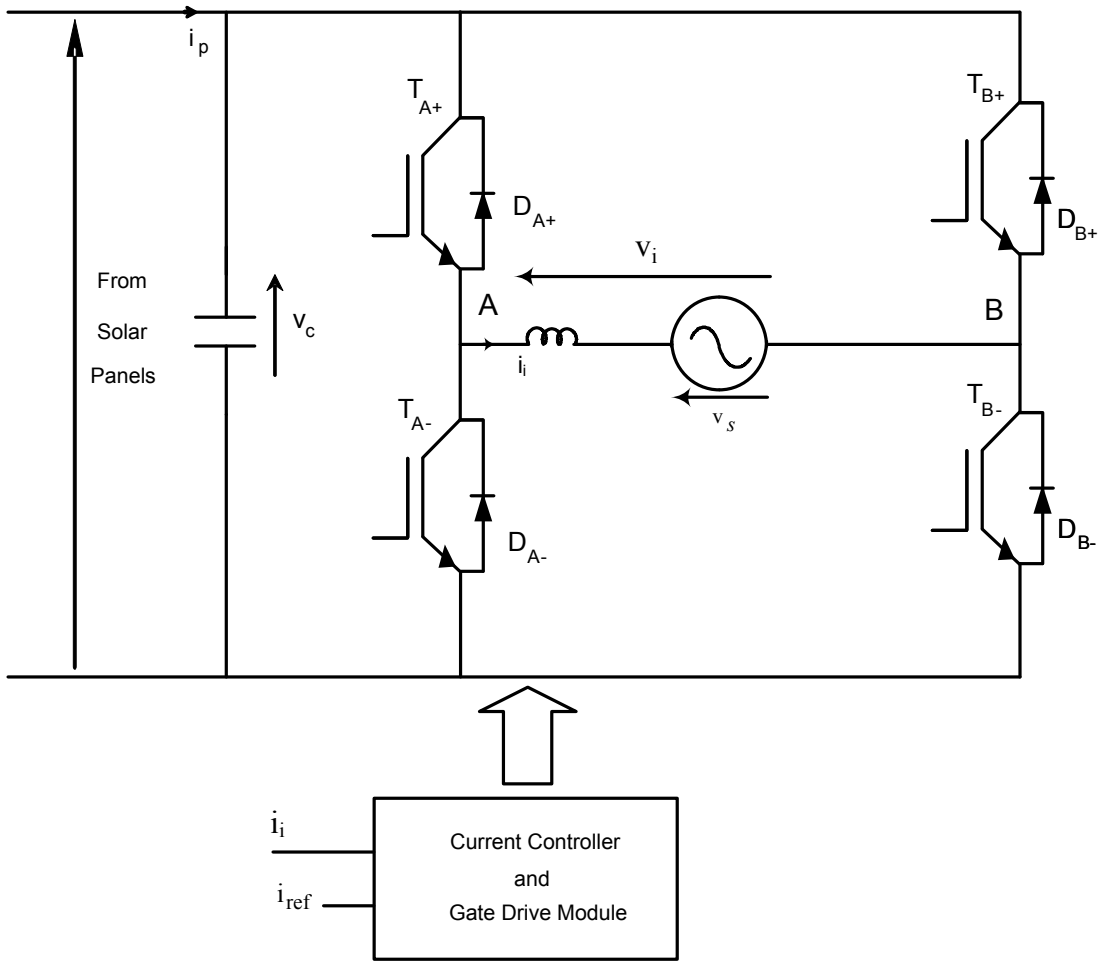


Figure 2.4: Current Controlled Grid Connected Full Bridge Inverter

2.3.1 Bipolar Switching

Consider the inverter in figure 2.4. If the aim is to achieve unity power factor, current reference signal (i_{ref}) is arranged to be in phase with the supply voltage (v_s). During the positive half cycle of the source voltage (v_s), when current (i_i) falls below the bottom limit of the hysteretic band, T_{A+} and T_{B-} are switched on. As a result the current rises through

T_{A+} and T_{B-}. If the current rises above the top limit of the hysteretic band, T_{A+} and T_{B-} are switched off and current (i_i) falls through D_{A-} and D_{B+}.

During the negative half cycle of the source voltage (v_s), when current (i_i) goes above the top limit of the hysteretic band, T_{A-} and T_{B+} are switched on. As a result the current rises negatively through T_{A-} and T_{B+}. When the current goes below the bottom limit of the hysteretic band, T_{A-} and T_{B+} are switched off and current (i_i) falls towards zero through D_{A+} and D_{B-}.

In practice when a transistor pair is switched off (say T_{A+} and T_{B-}), the next pair (say T_{A-} and T_{B+}) is not switched on straight away. This is to ensure that the transistors being turned off are fully off before the next pair is turned on. The short time that is allowed to elapse between initiation of turn-off of one pair and initiation of turn-on of the next pair is called the blanking time. The blanking time used is of the order of one or two microseconds. Without a long enough blanking time, there is a risk of short-circuiting the inverter DC supply.

It appears from the previous paragraphs that T_{A-} and T_{B+} are not needed during the positive half cycle of i_{ref} and similarly T_{A+} and T_{B-} are not needed during the negative half cycle. Ideally that would be the case at unity power factor. But generally speaking,unity power factor cannot be assumed and except for the duration of the blanking time there should always be one transistor pair switched on.

In other words, when one transistor pair is switched off the other pair should be switched on straight after expiry of the blanking time.

2.3.2 Unipolar Switching

Assuming unity power factor operation, reference current (i_{ref}) is arranged to be in phase with AC supply voltage (v_s). During the entire positive half cycle of the source voltage(v_s), insulated gate bipolar transistor T_{B+} is kept off and T_{B-} is kept on. Transistor T_{A+} is switched on when the inverter output current (i_i) goes below the bottom limit of the hysteretic band. This causes current (i_i) to rise while it flows through T_{A+} and T_{B-}. When current (i_i) goes above the upper limit of the band T_{A+} is switched off. This causes (i_i) to fall while it flows through D_{A-} and T_{B-}.

During the entire negative half cycle of the voltage (v_s), transistor T_{B-} is kept off and T_{B+} is kept on. Transistor T_{A-} is switched on when the inverter output current (i_i) goes above the top limit of the hysteretic band. This causes current (i_i) to rise negatively while it flows through T_{B+} and T_{A-}. When current (i_i) goes outside the lower limit of the band T_{A-} is switched off. This causes current (i_i) to fall towards zero while it flows through D_{A+} and T_{B+}.

Compared to the bipolar case switching frequency in the unipolar case becomes significantly low on approach of the zero crossing. The reason for this is that while the rise time of the inverter output current within the hysteretic band is proportional to (v_c - $|v_s|$), the fall time is proportional to $|v_s|$. Thus as the zero crossing is approached fall time becomes longer and switching frequency is effectively lower. This, together with the necessary blanking time is responsible for zero-crossing distortion.

It appears from the previous paragraphs that T_{A-} is unnecessary during the positive half cycle of i_{ref} and similarly T_{A+} is not needed during the negative half cycle. Ideally that would be the case at unity power factor. Generally speaking, unity power factor cannot be

assumed and except for the duration of the blanking time there should always be one of either T_{A+} or T_{A-} switched on. That is when T_{A+} or T_{A-} is switched off then the complementry transistor T_{A-} or T_{A+} should be switched on straight after expiration of the blanking time.

Note that irrespective of the operating power factor, transistors T_{B+} and T_{B-} are switched only at the zero crossing of the AC supply voltage. The relatively low switching frequency of T_{B+} and T_{B-} is the reason behind the fact that a unipolar switched inverter suffers lower switching losses compared to the bipolar switched inverter.

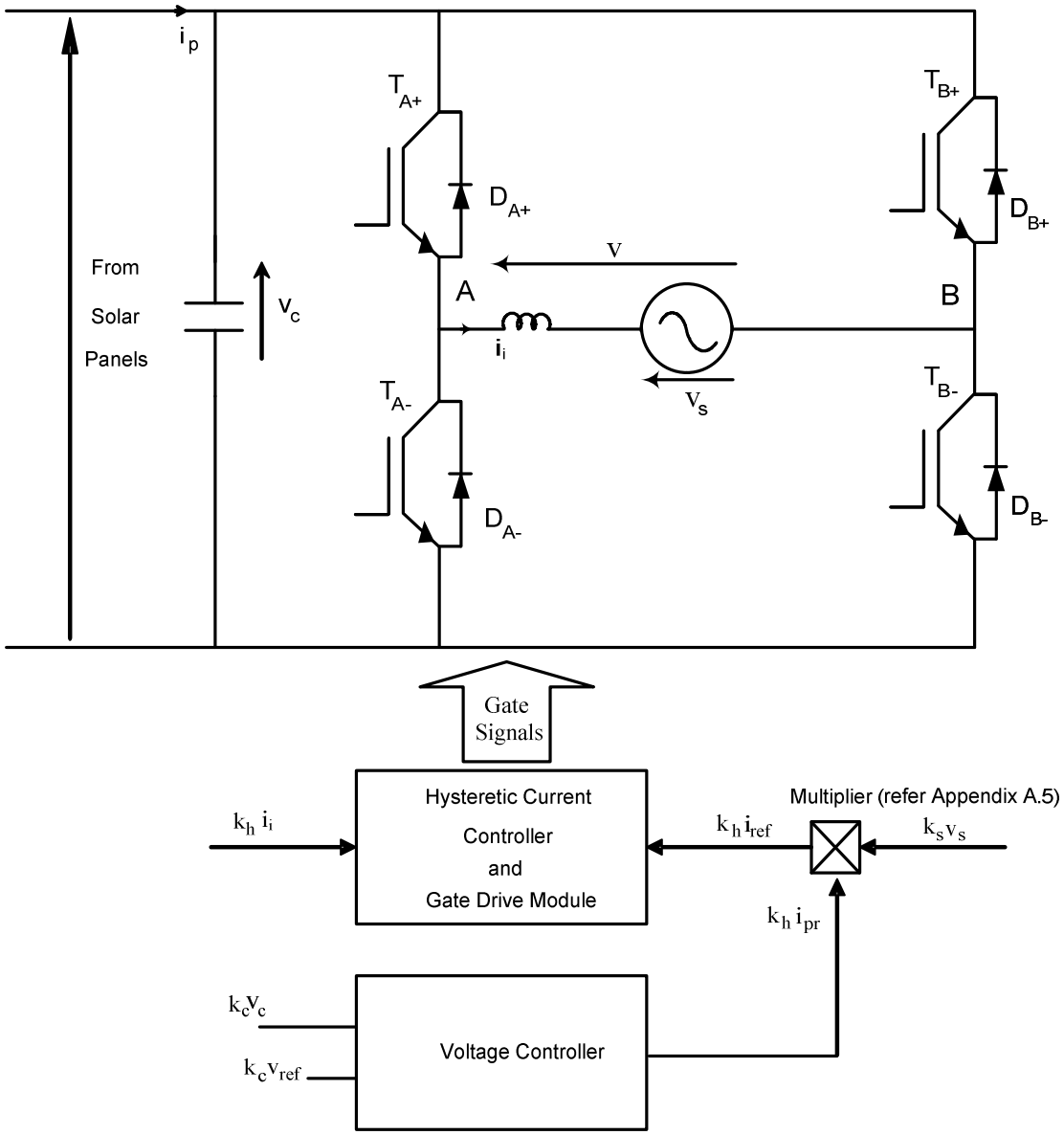
2.4 System Control Loops

The hysteretic controller described in section 2.2 forms the innermost control loop of the grid-connected PV system. Since there is no substantial storage between the output of the solar array and the output of the inverter, there is a need for control of power. The idea is to continuously adjust the rms value of the inverter output current(I_i) so that it is proportional to the power output from the solar array which is itself continuously changing. In other words, as insolation level rises or falls, the reference current (I_{ref}) should automatically rise or fall in proportion so that power balance is preserved. It is the role of the voltage control loop to maintain balance between the solar array power output and power input into the AC network. This section covers the principles behind the voltage control loop. It also covers the maximum power tracker. The maximum power tracker is a control loop in its own right. Whereas the voltage control loop aims for balance between power output from the array and power output of the inverter, the maximum power tracker aims to operate the solar array at a voltage level that would result in maximum extraction of power.

2.4.1 DC Bus Voltage Control

As shown in figure 2.5, the DC bus voltage signal ($k_c v_c$) and the reference voltage ($k_{c.} v_{ref}$) are inputs to the voltage controller. At steady state, the DC bus voltage signal ($k_c v_c$) will be practically equal to the DC bus reference voltage ($k_{c.} v_{ref}$) and the controller output ($k_h i_{pr}$) will be a constant. The output of the voltage controller is multiplied by the mains AC voltage signal ($k_{s.} v_s$) to produce the current reference signal ($k_{h.} i_{ref}$). The inverter output current signal ($k_h i_i$) and the current reference signal ($k_{h.} i_{ref}$) are inputs to the hysteretic current controller which generates gate signals to switch appropriate inverter devices as described in section 2.3.

A rise in output power from the solar array tends to cause a rise in DC bus voltage(v_c) which in turn causes a rise in ($k_h i_{pr}$). This causes I_{ref} (rms of i_{ref}) to rise resulting in inverter output current I_i (rms of i_i) rising because it tracks (i_{ref}). The rise in current I_i restores power balance between the DC power output of the solar array and the AC power output of the inverter. Thus the aim of the voltage control loop is to maintain power balance by getting the DC bus voltage signal ($k_c v_c$) to be practically equal to the reference ($k_c v_{ref}$). The system shown in figure 2.5 is a single stage power balance controller unlike the system in [2] where a DC to DC converter stage is used. Some flexibility is lost in array configuration but this is offset by simplified control and removal of a switching stage and associated devices. Details of analysis and implementation of the voltage control loop are presented in chapter 5.



k_h = Current sensor constant (V/A)

k_c = DC bus voltage sensor constant (V/V)

k_s = AC mains voltage sensor constant (V/V)

Figure 2.5: Inverter and Bus Voltage Control Loop

2.4.2 Maximum Power Tracker

Although the grid connected PV system can operate with a constant bus voltage reference (v_{ref}), the consequence would be significantly reduced efficiency. The I-V curve of a solar array at a particular insolation level is shown in figure 2.6. If the array is operated well into the "current source" region, at operating point (*X*) for example, current is relatively high but voltage is low and consequently power output is low. On the other hand if the array is operated well into the "voltage source" region at operating point (*Z*) for example, voltage is relatively high but current is low and again power output is low. Note that in figure 2.6 power output is represented by the area of a rectangle. It is clear that there exists a point (*Y*) along the I-V curve somewhere between (*X*) and (*Z*) that corresponds to maximum power. The purpose of the maximum power tracker is to determine that point and to set the reference voltage (v_{ref}) to correspond to that point. Assuming the maximum power tracker is operating correctly, the voltage controller would ensure that the array operates at the maximum power point.

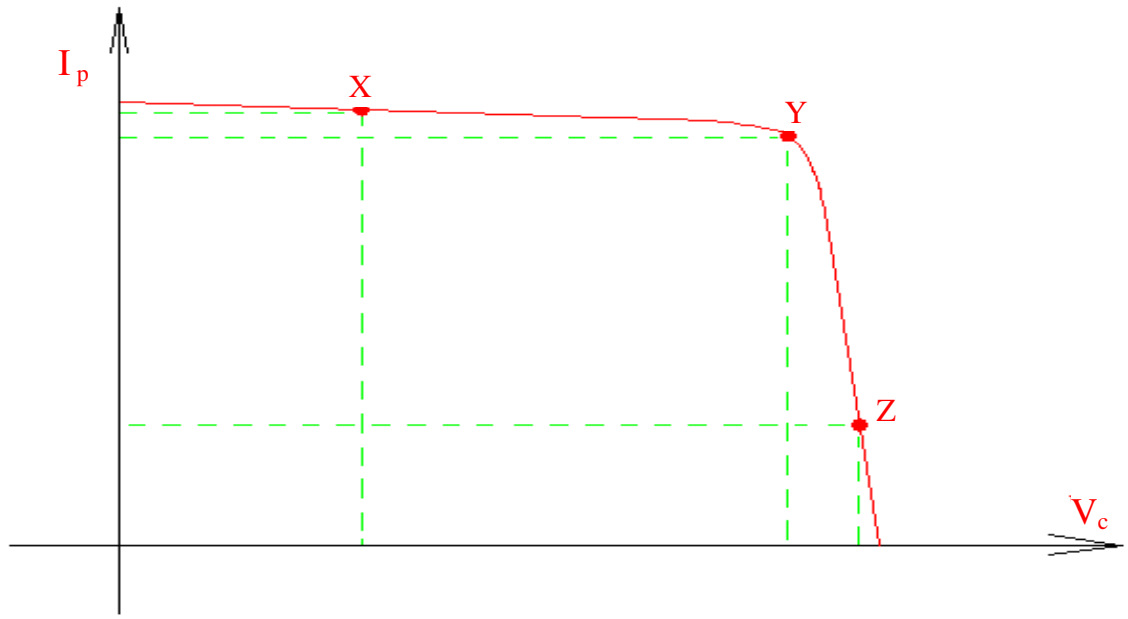


Figure 2.6: PV Array Characteristic at Given Insolation and Temperature

The I-V characteristics of a solar array is a function of insolation level and temperature. This means that as insolation level or temperature changes the operating point changes. Referring to Figure 2.7, assume that the system is initially operating at optimum point (Z_1). This implies that (v_{ref}) is practically equal to (v_c). However, if there is an increase in insolation level and the maximum power tracker is inactive, the operating point will shift to non-optimal point (Z_{no}). But the maximum power tracker is normally designed to continually check whether or not operation is optimal, and change the reference voltage accordingly. As shown in figure 2.7, as a result of the increased insolation level, the maximum power tracker will cause the operating point to shift from *(Z_1)* to *(Z_2).*

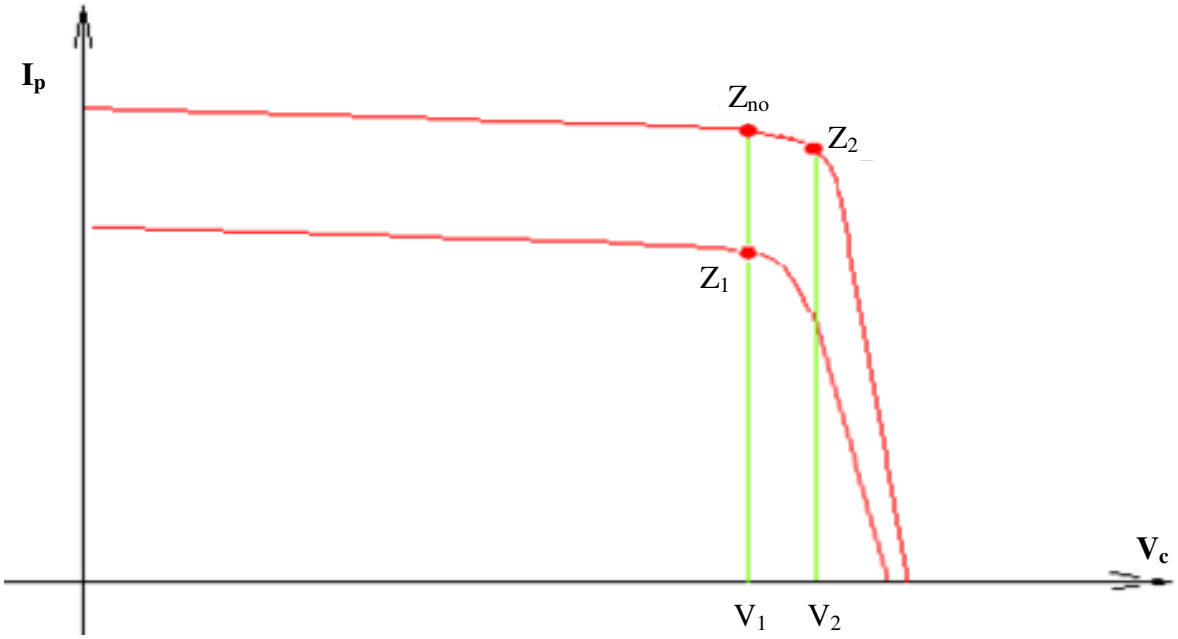


Figure 2.7: The Need for Maximum Power Tracking

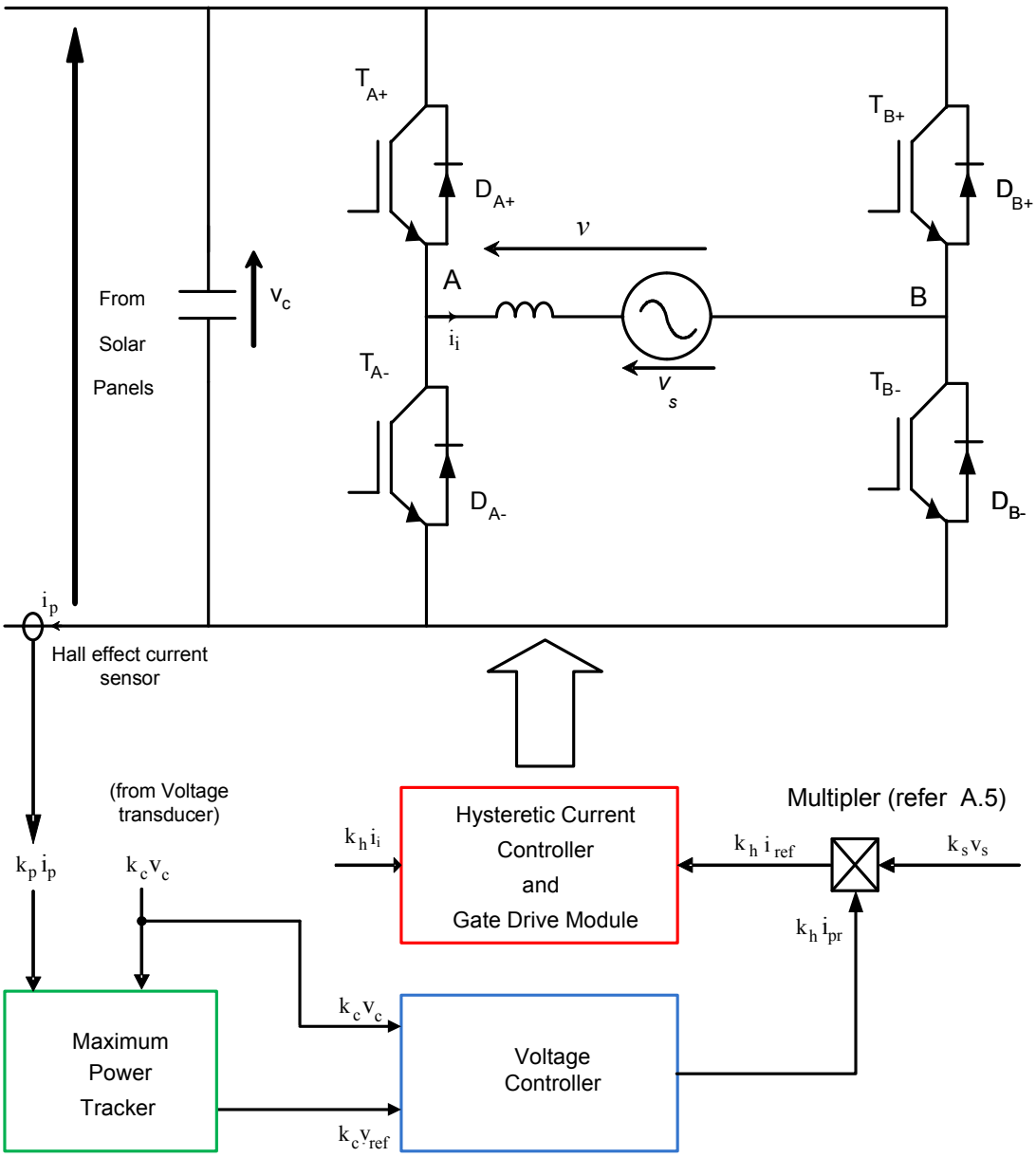


Figure 2.8: Grid Connected PV System with Maximum Power Tracker

In essence, the maximum power tracking procedure involves the following steps:

(a) Calculate and record array output power ($v_{c.}i_p$ in figure 2.8);

(b) Adjust the voltage reference by Δv_{ref}, where Δv_{ref} is a small value;

(c) Wait 30 seconds, allowing (v_c) to settle to its new value;(refer section 5.2)

(d) Calculate and record the new value for array output power(averaged over the waiting time for step (c).

(e) Calculate ΔP, the change in array output power compared to the previous value.

(f) Reverse the previous change in reference voltage if $\Delta P \leq 0$ otherwise change the voltage reference by ΔV in the same direction as the previous change.

(g) Repeat steps (c) to (f).

Referring back to figure 2.7, the increase in insolation level will result in the maximum power tracker increasing the reference voltage from (v_1 +/- ΔV) to (v_2 +/- ΔV). More specific details of the final MPPT implementation are given in chapter 5. More rapid changes can occur with cloud movement and this has been covered in previous work AUPEC93 where it was the focus of study, in the case of rapid transients the Bus voltage control loop will react accordingly.

2.5 Potential for Cost and Performance Improvement

The review presented in this chapter, on inverter configurations and common switching and control strategies point to a number of questions which directly relate to potential cost and/or performance improvement.

These are:

(a) Can the current controlled inverter work without a mains frequency isolating transformer and still operate within DC injection limits imposed by Australian and other standards? Would a DC offset controller have to be integrated in the inverter control system? Would that DC offset controller interfere with other inverter control loops? How would DC offset be sensed? How would the control parameters of the DC offset controller be arrived at?

(b) Compared to bipolar operation, does unipolar operation, as a result of its lower number of switching operations per inverter cycle, have the advantage of lower power loss? How can the difference in power loss be measured in practice? Is there a power quality penalty if unipolar operation is adopted instead of bipolar operation?

The aim of the literature review presented in the next chapter is to identify previous research findings that could help address the above questions.

Chapter 3

Literature Review and Project Plan

This chapter covers a literature review and a summary of the adopted plan for the project. The literature review is focussed on the quality of power from grid-connected inverters, in particular the question of DC injection into the AC network by single phase photovoltaic systems and on the comparison between unipolar and bipolar switching methodologies.

3.1 Review of Literature

3.1.1 DC Offset Control

Ideally the output current of the inverter, forming part of a grid connected PV system, will be purely AC. However, in practice, unless special measures are taken, it will contain a small amount of DC. Injection of DC into the AC mains, if excessive, can lead to problems such as corrosion in underground equipment [3], transformer saturation and transformer magnetising current distortion [4] and malfunction of protective equipment [5]. Therefore guidelines and standards have been set up to regulate DC injection [6,7,8]. For example Australian Standard AS4777.2 [1] limits DC injection to 5mA or 0.5% of rated output whichever one is greater and, in the United Kingdom, ER G83/1 [8] imposes a limit of 20mA.

The simplest way to eliminate DC injection is to include a grid frequency transformer between the output of the inverter and the AC network. This has been the solution adopted in a number of commercial systems [6,9]. Inclusion of a grid frequency transformer implies major disadvantages such as added cost, mass, volume and power losses. Some

commercial systems include a smaller higher frequency transformer or are transformerless. Salas [6], reports on measurements of DC currents from the AC output of commercial systems. Compared to the limits imposed by AS4777.2 [1] or by ER G83/1 [8], the measured DC currents were found to be very significant. Methods to solve the DC injection problem have been proposed by Masoud [3], Sharma [10] and Armstrong [11]. Masoud [3] and Sharma [10] both propose the use of a feedback loop to eliminate the DC offset in the inverter output. Masoud [3] suggests using a voltage sensor at the inverter output consisting of a differential amplifier and a low pass filter. Any DC detected at the output of the low pass filter is fed back to the controller which in turn operates the inverter in such a way as to reduce the DC offset. A simple mathematical model is suggested for the control system and it is assumed that the inverter is voltage controlled. However, experimental results are not reported.

Armstrong [11] proposes an automatic adjustment scheme to negate the effect of DC offset contributions from the Hall-effect current sensor in series with the DC input. Software is used to ensure that the current measurement made during freewheeling intervals is subtracted from all measured current values. This technique is however limited to unipolar switched inverters whose control enables the freewheeling intervals to be easily determined. Blewitt [12] considers using a large series electrolytic capacitor to block any DC component of current. This method requires an additional fast control loop and a slower capacitor offset voltage control loop while reporting a maximum of 5mA injected into the mains. Buticchi[13] also uses a sensor at the output of the inverter to detect DC voltage offset and a DSP to effect control. However it incurs additional losses and fails to meet the requirements of AS4777 [1].

Sharma [10] considers a current controlled inverter. Again a sensor is connected at the output of the inverter to detect the presence of any DC offset voltage. The sensor consists of an RC circuit and a 1:1 signal transformer. It is recognised that the DC signal is of the order of less than a few mV and needs to be extracted from a total signal of more than two hundred volts which is essentially the grid supply voltage. The RC circuit is connected in series with the secondary side of the 1:1 signal transformer. The series combination is connected across the inverter output. The primary side of the 1:1 signal transformer is connected across the AC supply. Thus, if it is assumed that the signal transformer is perfect and that the secondary voltage of the transformer opposes the AC supply voltage, only DC appears across the capacitor in the RC branch. The capacitor voltage is fed back to the controller which in turn adjusts the inverter current reference so that the DC offset is eliminated. No quantitative experimental results are reported, except for a statement that the DC offset controller has been found to operate correctly. A mathematical model of the controller is presented in a subsequent paper by Ahfock [14]. The mathematical model is experimentally validated and it is shown that the 1:1 transformer is effective only if its primary winding time constant is sufficiently low. In other words a relatively large core and a low winding resistance are necessary, making the DC offset sensor bulky and expensive.

In this project a simple two-stage RC filter will be used as DC offset sensor. Unlike the DC sensors in Masoud [3] and Sharma [10], where sensing is carried out across the AC supply terminals, the DC offset sensor in this project will be connected across the ripple filter inductor at the output of the inverter bridge as in Bowtell [15]. The disadvantage of sensing across the AC supply terminals is that the sensed DC offset could be due to sources other than the inverter. On the other hand the DC offset detected by the proposed sensor is guaranteed to be caused by the inverter being controlled. A design procedure will be

developed for the proposed DC offset controller. This will require investigating possible interactions between the DC offset control loop and other control loops within the system.

As pointed out in the previous section, the three other control loops are:

(a) the Current Control Loop;

(b) the DC Bus Voltage Control Loop;

(c) and the Maximum Power Tracking Loop.

The design of those control loops is greatly simplified if, from a control point of view, they do not interact. A number of authors such as Raoufi [16] and Varjasi [17] have either implicitly or explicitly assumed that the DC bus voltage control loop does not interact with the other loops and they invariably use a mathematical model based on capacitor power balance to design the DC bus voltage controller. An objective of this research is to consider the dynamic response of each control loop in detail. The DC bus voltage control loop operates outside the current control loop. The voltage controller provides the reference signal for the current controller. The current loop operates much faster than the outer voltage loop. So they can be designed independently. When designing the voltage loop, the current loop may be assumed to be a pure gain. The current loop, on the other hand is designed under the assumption that the controlled current does not influence the reference current. In this project, as is normal practice, the voltage control loop and current control loop will be independently designed. However experimental verification will be carried out to confirm that there is no interaction between them.

The maximum power tracker, unlike the other loops, does not have a reference input. It is an extremum seeking loop. In single stage conversion systems, such as the one considered for this project and by others such as Varjasi [17] and Gonzales [19], the maximum power tracker provides the voltage reference for the voltage control loop. That voltage reference, once set by the maximum power tracker, is not immediately influenced by any other

control loop. After setting the reference voltage to a new value, the maximum power tracker waits for the voltage controller to get the DC bus voltage to that value before operating again. Therefore the voltage control loop can be designed under the assumption that its operation does not influence its reference voltage.

There is very little that has been published on controlling the DC offset current at the output of a grid-connected PV system. There appears to be no work done so far on the question of possible interactions between a DC offset control loop and other control loops in the system. As part of this project, an attempt will be made to show that the design of a DC offset control loop can be made independent of the other control loops. In other words the aim will be to show that the DC offset control loop does not affect operations of the other loops and vice-versa.

3.1.2 Output Current Harmonic Distortion

Apart from a possible DC component, the output current of a grid-connected photovoltaic system contains harmonics. The harmonics can generally be classed as switching (or ripple) harmonics and low frequency harmonics. The ripple frequency, for systems in the kilowatt range, can be between a few kilohertz and tens of kilohertz. Low frequency harmonics are at integral multiples of the AC supply frequency.

Switching within the inverter can cause very fast charging and discharging of stray capacitances. The frequency spectra of the associated stray currents are in the megahertz range and can be a major cause of electromagnetic interference. Low frequency harmonics; ripple frequency harmonics; and electromagnetic interference will be considered in turn.

Grid connected PV systems have to meet the requirements of standards such as AS4777.2[1] which states that total harmonic distortion in the injected current should be less than 5% for harmonics up to the 50^{th}. Many researchers have explored the question of such systems harmonic injection into the AC network, for example Kirawanich [20], and [21-23]. In common with other publications, all of these studies were based on measurements made on commercially available grid connected systems. Their results show that while the levels of low frequency harmonics are small they are still significant relative to the requirements of standards such as AS4777.2 [1]. Therefore there is a need to look carefully at causes of low frequency harmonics in grid-connected inverters with the aim of eliminating them or reducing their effects. There has been significant research activity in this area but the focus has been on voltage controlled systems. Oliva [25] lists possible causes of harmonics in voltage controlled converters as filter nonlinearities, dead-times, device voltage drops and DC link voltage harmonics. Mohan [26] provides an explanation of relationship between dead-time and voltage harmonics. The use of dead-times causes harmonics that manifest themselves as distortion at the current zero crossings. Kotsopoulos [27] suggests a simple mathematical model to quantify harmonic levels due associated with zero-crossing distortion. Oliveira [28] suggests a technique for reducing zero-crossing distortion due to dead-times. The proposed technique is, however, applicable to voltage controlled inverters. If the current reference is free of harmonics, the output current of current controlled inverters should be virtually free of low frequency harmonics. Nevertheless, Bowtell [29] has reported the presence of significant low frequency harmonic content at the output of current controlled inverters. There is very little in the published literature about the causes of low frequency distortion in current controlled inverters.

Possible reasons for low frequency distortion are:

(a) distortion in the current reference signal[30];

(b) distortion in the control signal generated by the voltage control circuit [31];

(c) switching delay [32,33]

(d) dead-time.

In the case of a unipolar switched inverter, there can be distortion near the negative going zero- crossing due to inability of the available AC supply voltage to bring the current down quickly enough so it can follow the reference. Similar distortion happens in switch-mode rectifiers at the positive going zero crossing of the rectifier input current Salmon [34]. It appears that bipolar switched current controlled inverters suffer significantly less zero crossing distortion. Lindgren [35], Ordonez [51] and Li [52] suggests using unipolar switching for most of the inverter cycles to exploit the potential switching loss reduction advantage and to use bipolar switching near the zero crossing to avoid zero crossing distortion.

An investigation into the causes of low frequency distortion, including zero crossing distortion, in current controlled inverters will be carried out as part of this project. A better understanding of those causes will make it easier to meet requirements specified by standards and help avoid the possibility of AC voltage distortion due to resonance effects.

Compared to low frequency harmonics, ripple frequency harmonics can be filtered out by relatively small and low cost components. Possibilities for ripple filtering are the L, LC and LCL filters. The LCL filter will be used in this project because it is the one that provides assurance against the occurrence of resonance. Bojrup [36] provides design guidelines for filter design. Although AS4777.2 [4], does not provide explicit guidelines on allowable ripple harmonic content, IEC 61000-3-2 [37], gives limits for harmonic currents up to the 40^{th} and considers this inverter a class A device [37]. An important

reason for limiting injection of ripple frequency current is to avoid interference with systems that use power lines for communication. Practical guidelines for harmonic and voltage flicker are also found in [38] and [39]. The frequency range of ripple current from typical inverters overlaps with the frequency band used by power line communication systems. References [36,51,52] fail to adequately consider reasons for the existence of low frequency harmonics or ripple filter transients at the transition points between unipolar and bipolar operation.

Careful circuit layout is necessary if EMC requirements are to be achieved. It should also be taken into consideration that different circuit configurations results in drastically different levels of EMI emission depending on the level and the distribution of stray capacitive currents that result from inverter switching. Gonzalez [19] offers some theoretical insight into the charging and discharging of stray capacitances between the solar panels and earth, but no test results are provided. Jiang [40] reports on simulation carried out to study EMC of different inverter configurations. But the configurations are not relevant to those being investigated in this project. Gonzalez [19] argues that in the case where the ripple filter is made up of two identical inductors, one connected between terminal A of the inverter (see figure 2 in [19]) and the neutral and the other between inverter terminal B and the active terminal, EMC performance is much better with bipolar operation than unipolar operation. As part of this project EMC performance will be investigated for the case where both inductors of the LCL filter are on neutral side. This particular case is of interest because this positioning of the inductors allows them to be readily used for DC offset current sensing.

3.2 Project Plan

As a result of the above literature review and the assessment of inverter technologies reported in chapter 2, the following activities were planned and carried out:

(a) *Design, construction and testing of a single-phase transformerless, grid-connected, voltage sourced, current controlled inverter, that can operate both in bipolar and in unipolar modes:* The main objective was comparison of power output quality and switching loss. The design incorporated several innovative features which are detailed in chapter 4. These included multi-mode switching to improve power quality and conversion efficiency. The inverter was designed to operate with a DC input voltage of up to 600V and to interface with the 240V, 50 Hz network.

(b) *Design and implementation of a software based power balance controller incorporating maximum power tracking and DC bus voltage control:* A commercial programmable controller, the Siemens CPU222 [41], was used because it had the advantage of cost effectiveness, robustness and immunity to noise. A mathematical model was developed to help with the choice of control parameters.

(c) *Theoretical and practical investigation into DC offset controllers that use the inherent resistance of the current steering inductor (L_i in figure 2.5) for DC offset current sensing*: Both an analogue controller and a digital controller were planned. An integral control element was considered necessary since the design objective was to maintain zero steady state DC offset. Mathematical models were developed for both controllers. These models were used to help with controller design.

Chapter 4

Comparison of Bipolar and Unipolar Control

4.1: Introduction

This chapter is a detailed presentation on inverter operation. Three switching topologies are investigated. These are the unipolar mode, the bipolar mode and mixed-mode which is partly bipolar and partly unipolar. The main theoretical findings are supported by experimental results.

Section 4.2 deals with the bipolar switching mode which is conceptually the simplest. It is demonstrated in section 4.3 that the, potentially more energy efficient, unipolar switched inverter has the disadvantage of current distortion at the supply voltage zero crossings. In section 4.4 a hybrid mode switching technique is explored which is a combination of unipolar switching and bipolar switching. It is shown that with the mixed-mode switching scheme distortion at the zero-crossings is practically eliminated.

The effect of switching delay, which is ignored in section 4.4, is investigated in section 4.5. It is confirmed that switching delay, if significant enough will cause low frequency current distortion, even in the mixed-mode case. A solution to the problem is proposed and implemented. Section 4.6 provides practical evidence that unipolar switching and mixed-mode switching result in significantly lower switching losses when compared to a bipolar switching scheme.

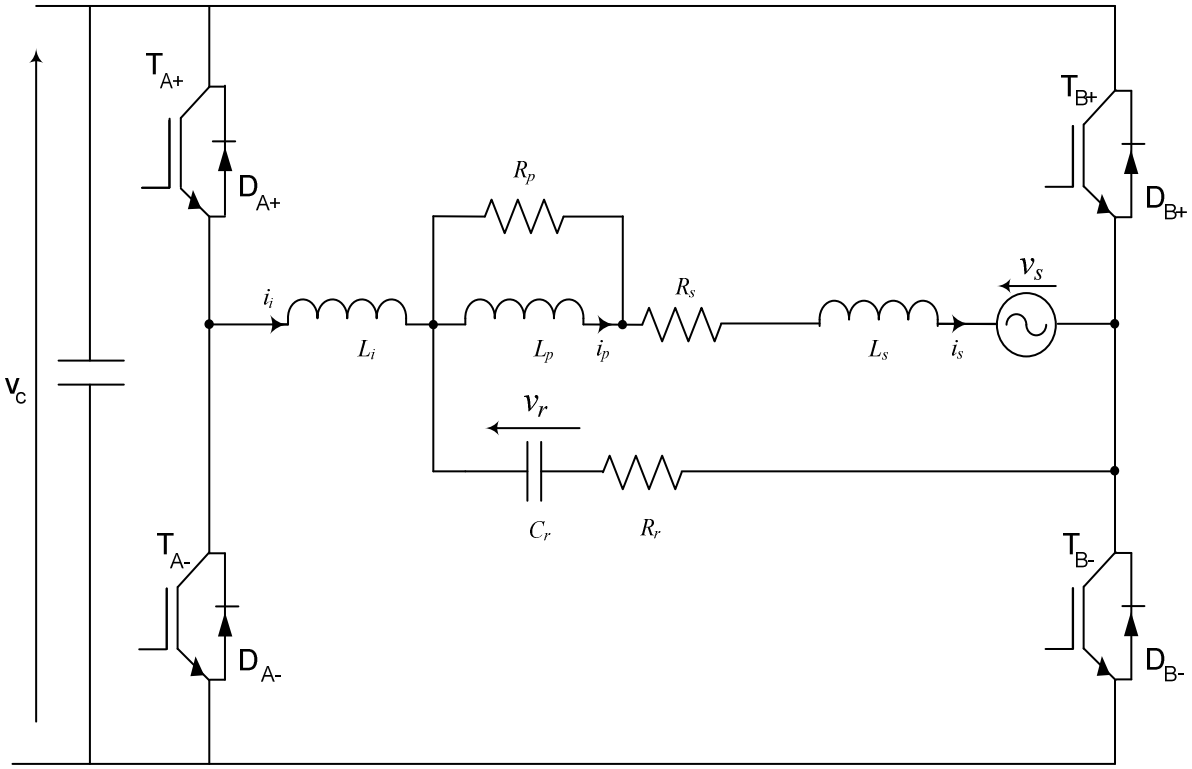


Figure 4.1: Inverter Components including LCL Filter

Figure 4.1 represents the inverter being considered in this chapter. The DC input voltage is fixed at 400V and the AC supply voltage is nominally 240V. R_s and L_s are the supply internal resistance and inductance respectively. Inductors L_i, L_p and C_r form the LCL ripple filter. Resistors R_p and R_r are for filter damping.

4.2 Bipolar Switching without Ripple Filter

A Simulink® model of the ideal bipolar switched inverter is shown in figure 4.2.

The ripple filter, which will be considered later, has been left out here.

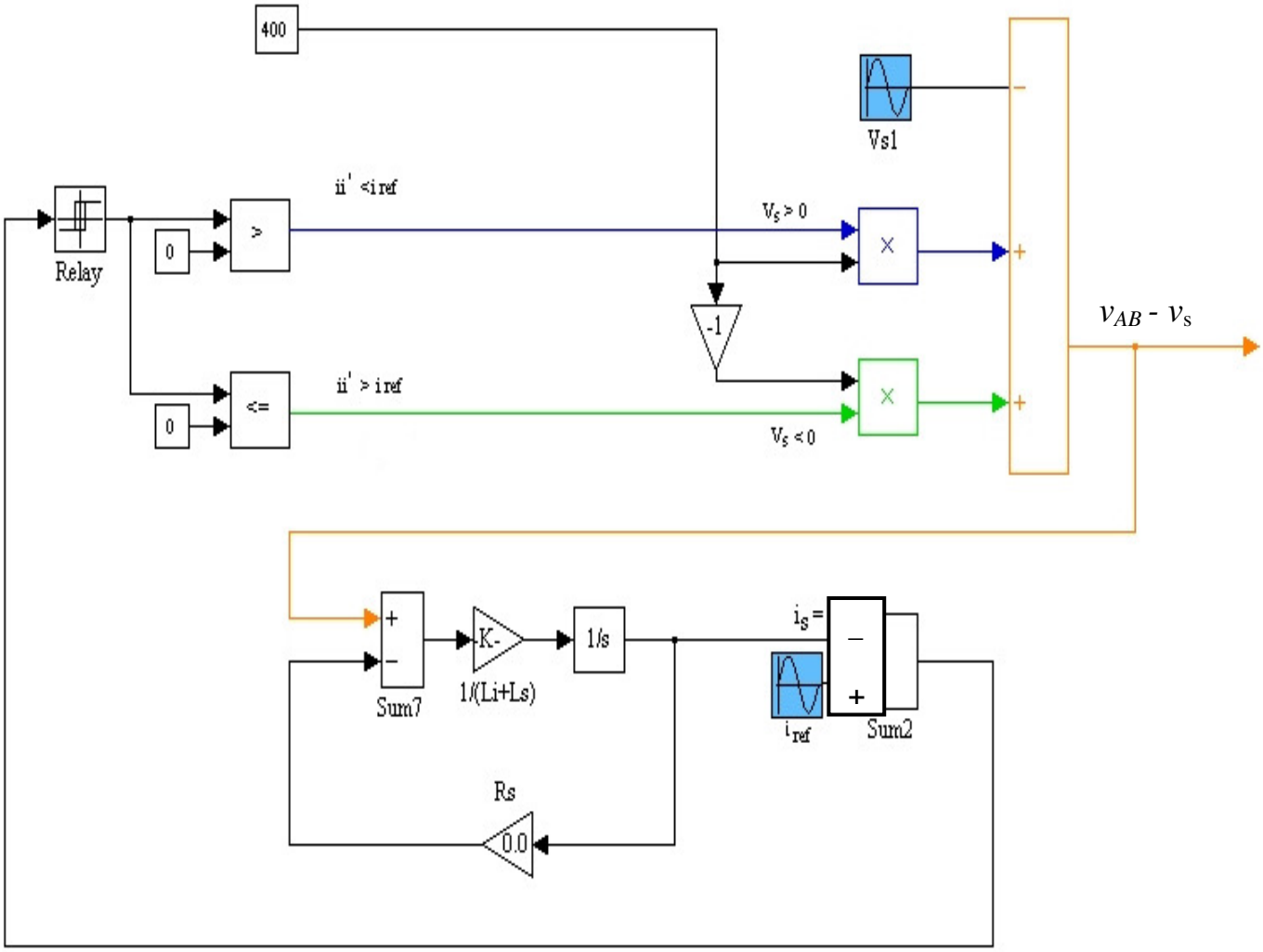


Figure 4.2: Simplified Bipolar Inverter Control Model

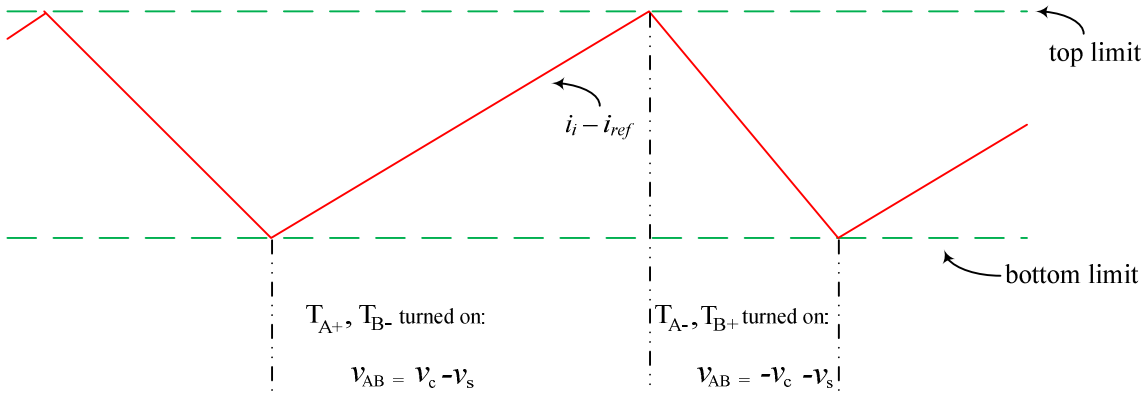


Figure 4.3: Hysteretic Control (no Ripple Filter)

Inverter switching is modelled by the relay block which operates in accordance with figure 4.3. The relay limits, +0.75A and -0.75A, represent the tolerance band of the current controller. When the current error $(i_i - i_{ref})$, reaches the bottom limit of the tolerance band, the output of the relay changes state. The voltage across the series combination made up of L_s, R_s and L_i is equal to $(v_c - v_s)$. Conversely, when the current error $(i_i - i_{ref})$ reaches the top limit of the tolerance band, the relay output changes state.

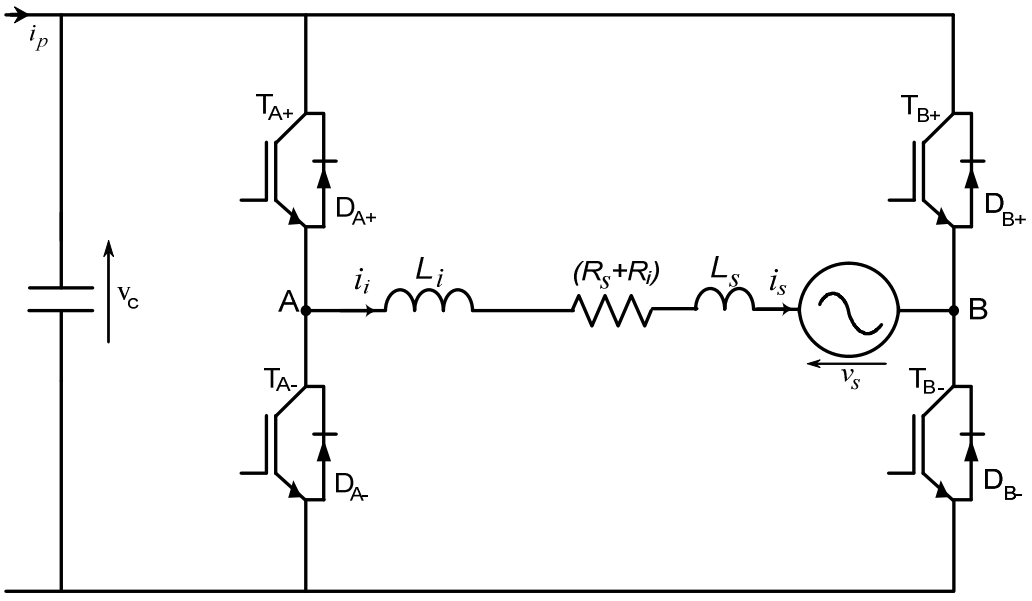


Figure 4.4: Simplified Bipolar Inverter Circuit

In this case the voltage across the series combination, as shown in figure 4.3, is equal to $(-v_c - v_s)$. The values of L_s and R_s were estimated from fault level information at the point of

supply. A value of 10mH for L_i was considered reasonable because it allowed the maximum frequency requirement of 30kHz be met with a theoretical tolerance band of ±0.75A. R_i was measured as 0.36Ω. Note that L_s and (R_i+ R_s) in figure 4.4 are relatively small and could have been neglected.

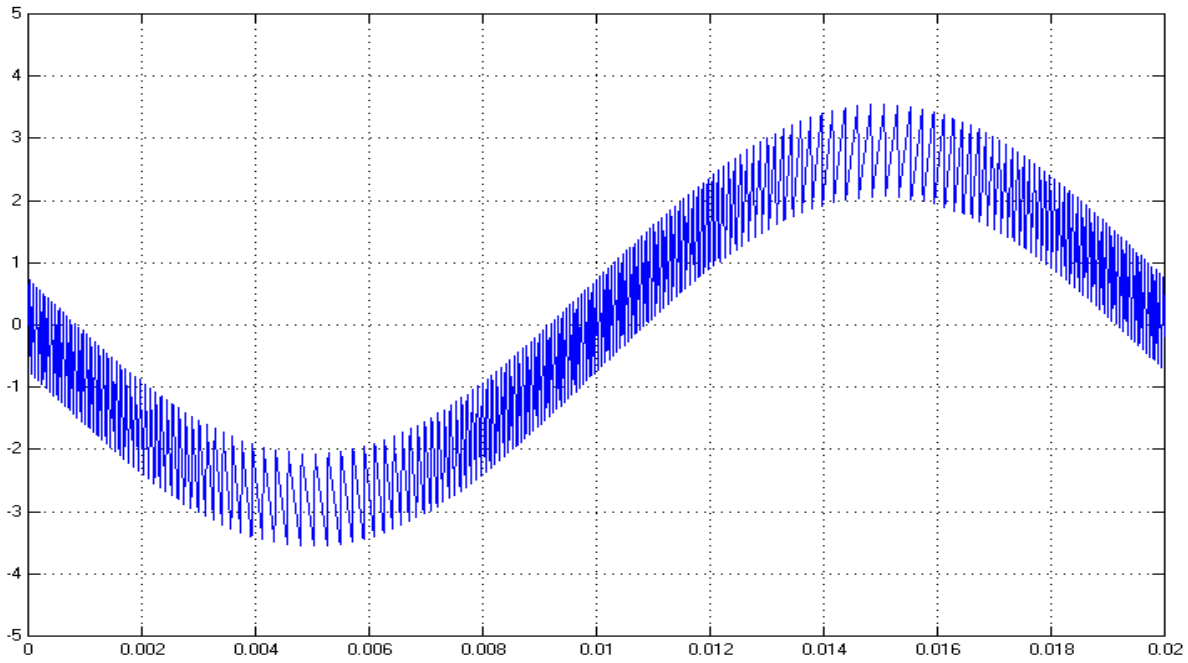


Figure 4.5: Theoretical Bipolar Operation (I_i = 2A)

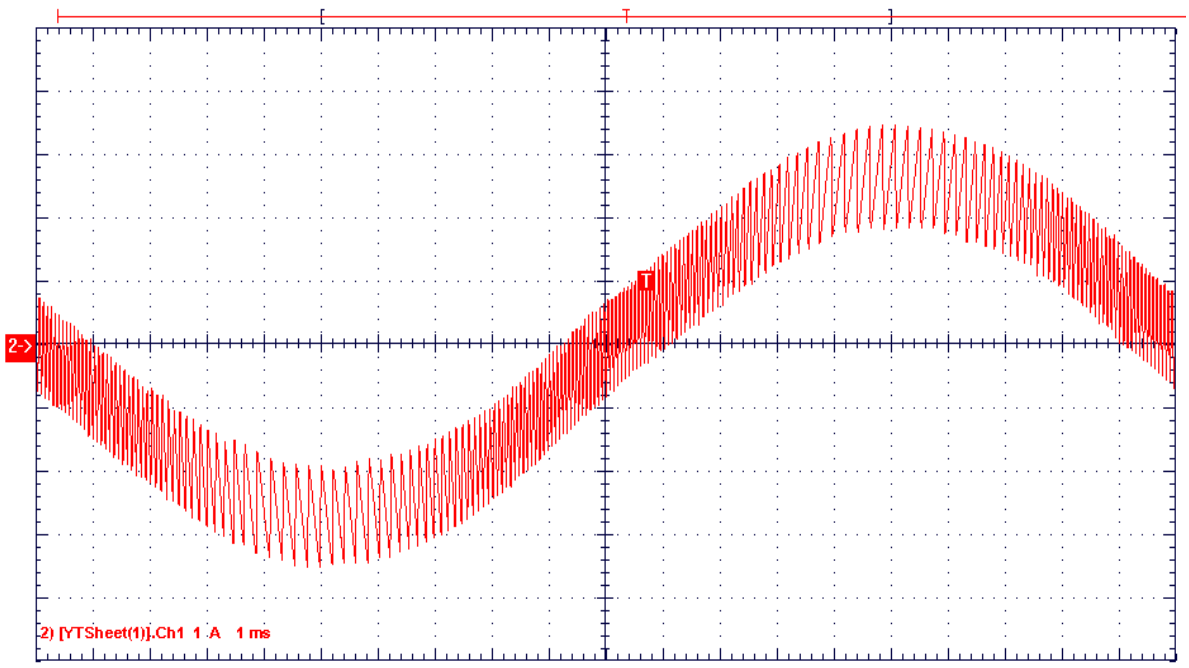


Figure 4.6: Experimental Bipolar Operation (I_i = 2A)

Figures 4.5 and 4.6 are respectively the theoretical prediction and test results for a reference current of 2.0A. There is very good correlation between them.

4.3 The Ripple Filter

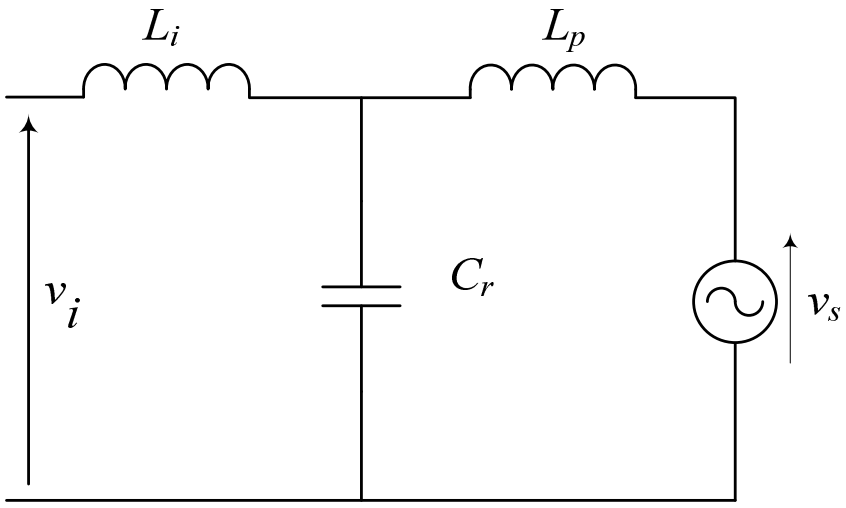


Figure 4.7: LCL Filter Components

Injection of significant levels of ripple frequency current into the AC network is not acceptable. The LCL filter represented in figures 4.1 and 4.7 can be used to attenuate ripple frequency current injection. The rationale behind the choice of filter components is given below.

In summary, the design procedure for the filter consists of the following steps:

(a) Determine the value of L_i so that maximum switching frequency is not exceeded, the tolerance band is reasonable and the cost, mass and volume of the inductor is acceptable. A maximum switching frequency is imposed to limit switching losses. This helps with efficiency and reduces cooling requirements. For bipolar operation, the inverter switches at maximum frequency near the zero crossing of the supply voltage.

The relevant equation to determine L_i is:

$$L_i = V_c \Delta t / \Delta i \quad 4.1$$

where:

V_c = the DC bus voltage

Δt = half the minimum allowable switching period

Δi = size of the tolerance band

(b) Calculate the lowest expected switching frequency of the inverter. For the bipolar inverter this will happen near the peak of the AC supply voltage. The relevant equations to estimate the minimum expected switching frequency is:

$$\Delta t_r = \frac{L_i \Delta i}{(V_c - \hat{V}_s)} \quad 4.2$$

$$\Delta t_f = \frac{L_i \Delta i}{(V_c + \hat{V}_s)} \quad 4.3$$

f_{min} = minimum switching frequency

$$= \frac{1}{(\ddot{A}t_r + \Delta t_f)} \quad 4.4$$

For the prototype inverter constructed, f_{min} was found to be 6.5kHz. This value is based on V_c= 410V; $\hat{V}_s$ = 339V; L_i = 10mH and Δi = 1A

(c) Based on the specified ripple attenuation and neglecting resistive components and AC supply impedance, calculate the required value of L_pC_r .Assuming that the values of L_p and C_r are such that the inverter operates as intended, the ripple magnitude is constrained by the tolerance band and ripple attenuation is given by:

$$\frac{1}{k_r} = \frac{-1}{1-\omega^2 L_p C_r} \qquad 4.5$$

where ω = ripple frequency

and k_r = specified attenuation at the lowest inverter switching frequency

From equation 4.5 we have:

$$L_p\, C_r = (k_r + 1) / \omega^2 \qquad 4.6$$

For the prototype inverter that was constructed $L_p\, C_r$ was calculated as $4\text{x}10^{-9}\text{S}^{-2}$

for an attenuation factor of 5.6 at ω_{min}.

(d) Select values for L_p and C_r based on the value of L_pC_r determined in step (c). Choosing a small value for L_p has the advantage of low cost. The impedance presented by the parallel LC circuit to the ripple current from the inverter is given by:

$$Z_p = j\omega L_p / k_r \qquad 4.7$$

(e) Equation 4.7 implies that using a small value for L_p makes Z_p small. This has the advantage of keeping the inverter switching as intended. In other words the L_pC_r parallel contribution does not have a significant or detrimental effect on inverter switching. However, for a given value of L_pC_r if L_p is made too small then the required value of C_r can become excessive. A large value of C_r demands a leading component of power frequency current which should normally be limited.

(f) Taking the above two opposing factors into consideration L_p and C_r were respectively chosen to be 2mH and 2μF. With those values Z_p is equal to 12Ω at the lower limit of the inverter switching frequency. This value is thirty times lower than $L_i\omega$ at the same frequency. Since Z_p appears in series with $L_i\omega$, it is expected that Z_p will not influence the inverter current flowing through L_i. The power frequency leading current due to C_r is 0.14A which is considered acceptable.

4.4 Filter Damping

The values of filter capacitance and inductance arrived at in the previous section were based on steady state analysis. In practice the filter will not be purely in the steady state. From time to time it will be subject to transients. Examples are transients at inverter turn-on and transients due to sudden changes in the reference current magnitude. Without damping, as shown in figure 4.8, an oscillatory component of current gets injected into the AC network after such transient events. The frequency of that current component is approximately equal to: $1/\sqrt{L_p C_r}$.

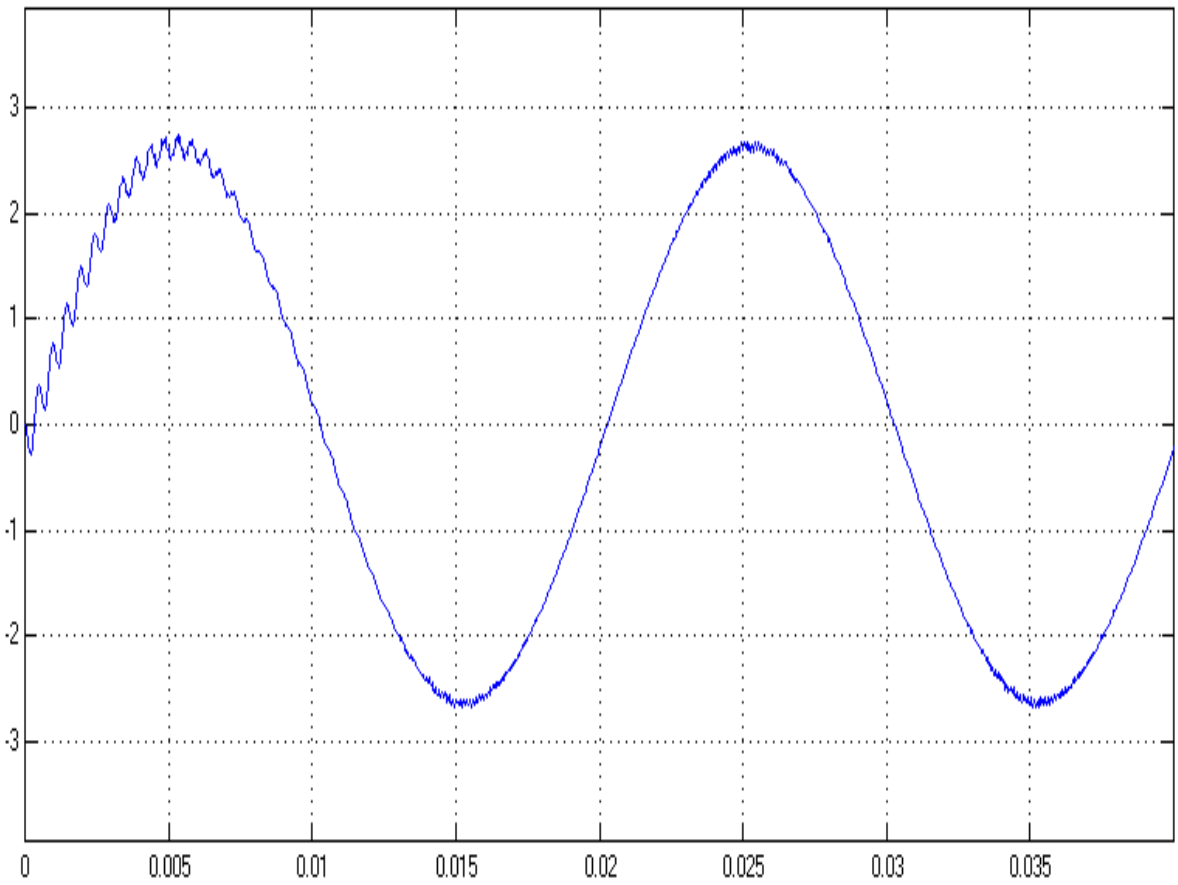


Figure 4.8: Undamped Filtered Waveform (simulated)

Three possibilities were explored for the addition of damping to the ripple filter. These are illustrated in figure 4.9. A damping resistor will have the following effects:

a. Natural filter oscillations will decay relatively quickly

b. Filter power loss will increase

c. The ripple attenuation will be adversely affected.

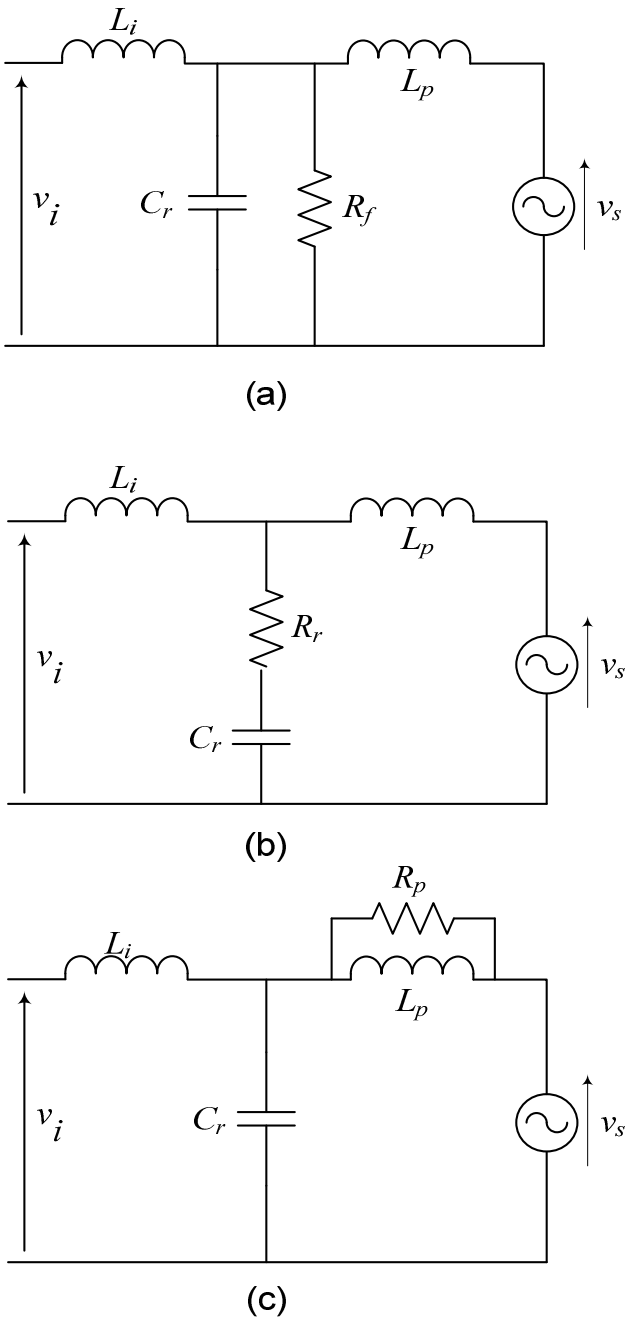


Figure 4.9: Filter Damping Options

The choice of filter resistance is based on balancing the desirable damping effect against the undesirable increase in filter losses and decrease in ripple attenuation. Equations 4.8 to 4.13 have been derived to assist with the selection of the damping resistance.

The three filter damping configurations shown in figure 4.9 respectively have the following characteristic equations:

$$sL_i [s^2 + s / (R_f C_r) + (1/ L_p + 1/ L_i) / C_r] \quad 4.8$$

$$sL_i [s^2 + s(1 + L_p / L_i)(R_r /L_p) + (1 + L_p / L_i) / (L_p C_r)] \quad 4.9$$

$$sL_i [s^2 + s / (R_p C_r) + (1/ L_p + 1/ L_i) /C_r] \quad 4.10$$

The decay time constants from the above expressions are respectively:

$$\tau = R_f C_r \quad 4.11$$

$$\tau = L_p / [R_r (1 + L_p / L_i)] \quad 4.12$$

$$\tau = R_p C_r \quad 4.13$$

For each of the damping options, damping resistance power loss is respectively given by:

$$(a) \quad Power\ loss \approx V_s^2 / R_f \qquad 4.14$$

$$(b) \quad Power\ loss \approx (V_s\, C_r\, \omega_s)^2 R_r + I_{tol}^2 R_r \qquad 4.15$$

$$(c) \quad Power\ loss \approx (I_i)^2\, \omega_s^2\, L_p^2\, R_p / (\omega_s^2 L_p^2 + R_p^2) \qquad 4.16$$

The previous three equations are based on the following reasonable assumptions:

i. The voltage across the capacitor is practically equal to the AC supply voltage.
ii. Practically all the ripple current flows through the capacitive branch of the filter.
iii. For the case of R_p (equation 4.16), power loss is a function of inverter output current.

Table 4.1 shows the respective power loss for a range of resistance values used with each of the three methods described above.

Table: 4.1 Filter Power Loss Comparison (L_p = 2mH; V_s = 240V; C_r = 2µF, I_i = 4.5A; I_{tol} = 0.75A)

Power loss	**0.1W**	**0.2W**	**0.4W**	**2.5W**	**5W**	**7.5W**	**10W**
R_f	580k Ω	270k Ω	150k Ω	22kΩ	12kΩ	8.2kΩ	5.6kΩ
R_r	0.18 Ω	0.33 Ω	0.68 Ω	4.4Ω	8.6Ω	12.8Ω	17.1Ω
R_p	100 Ω	47 Ω	22Ω				

Based on the data of table 4.1, equations 4.11 and 4.13, it is clear that for a given power loss level resistor R_p is much more effective at damping filter oscillations when compared to resistor R_f. This is particularly the case when the inverter output is less than rated. Similarly it can be deduced, from equations 4.12, 4.13 and the data of table 4.1 that if filter power loss is to be kept low, resistor R_p presents a much better alternative for the damping of filter oscillations when compared to resistor R_r. Examples presented in the next section illustrate this point. In summary, the filter parameters, chosen on the basis of cost, efficiency and filter oscillation decay time are:

$L_i = 10mH$

$L_p = 2mH$

$C_r = 2\mu F$

$R_p = 47\Omega$

Filter performance was verified by means of a Simulink® model, which is detailed in the next section.

4.5 Bipolar Switching with Ripple Filter

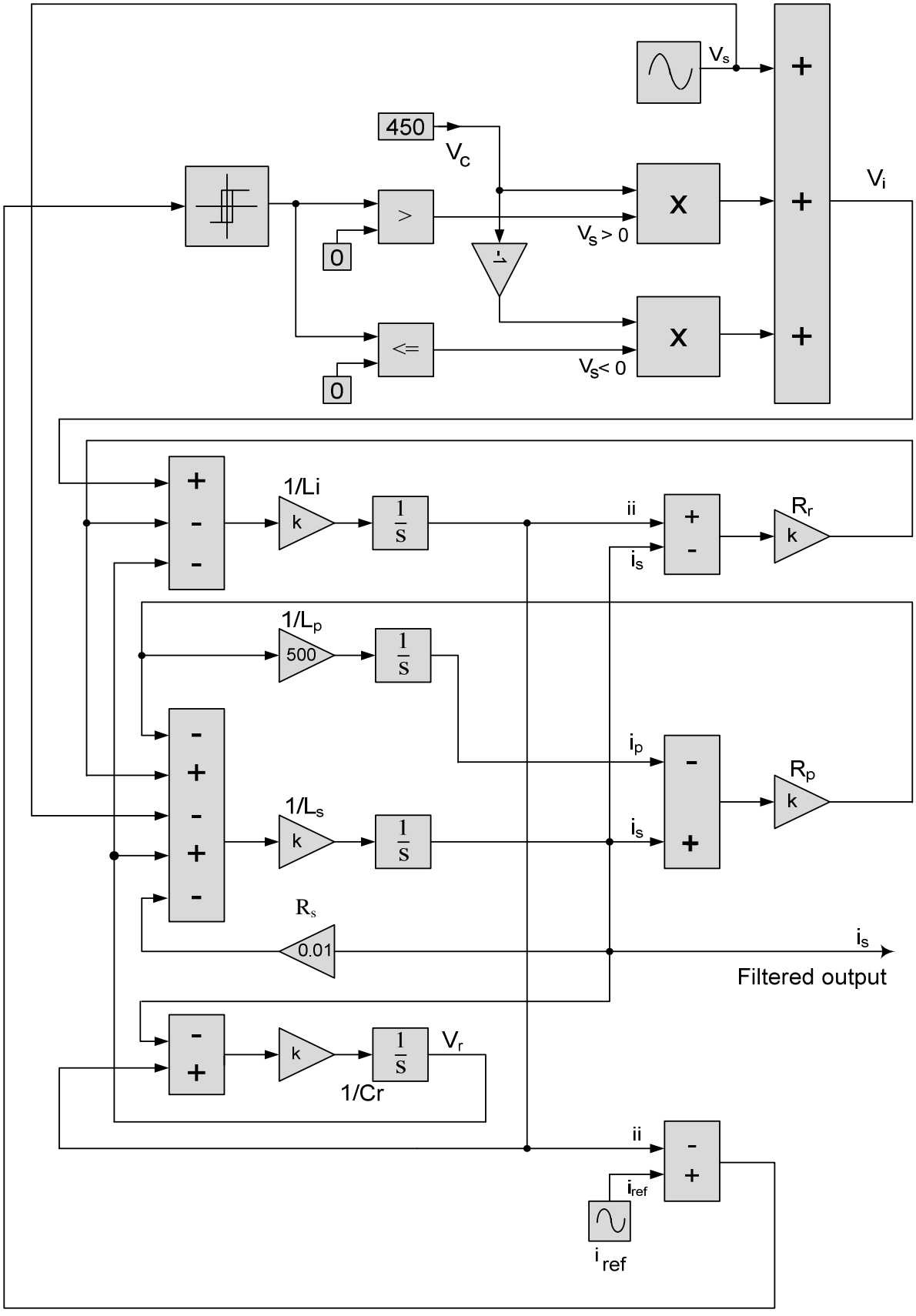


Figure 4.10: Simulink Model of the LCL Filter

Figure 4.10 is similar to figure 4.2 except that the current steering inductor block has been replaced by the LCL filter block, which is designed to satisfy the following equations:

$$L_i \frac{di_i}{dt} + (i_i - i_s)R_r + v_r = v_i \quad 4.20$$

$$L_p \frac{di_p}{dt} - (i_s - i_p)R_p = 0 \quad 4.21$$

$$L_s \frac{di_s}{dt} + i_s R_s + (i_s - i_p)R_p - v_r - (i_i - i_s)R_r = -v_s \quad 4.22$$

$$C_r \frac{dv_r}{dt} + (i_i - i_s) = 0 \quad 4.23$$

All symbols used above are defined in figure 4.1.

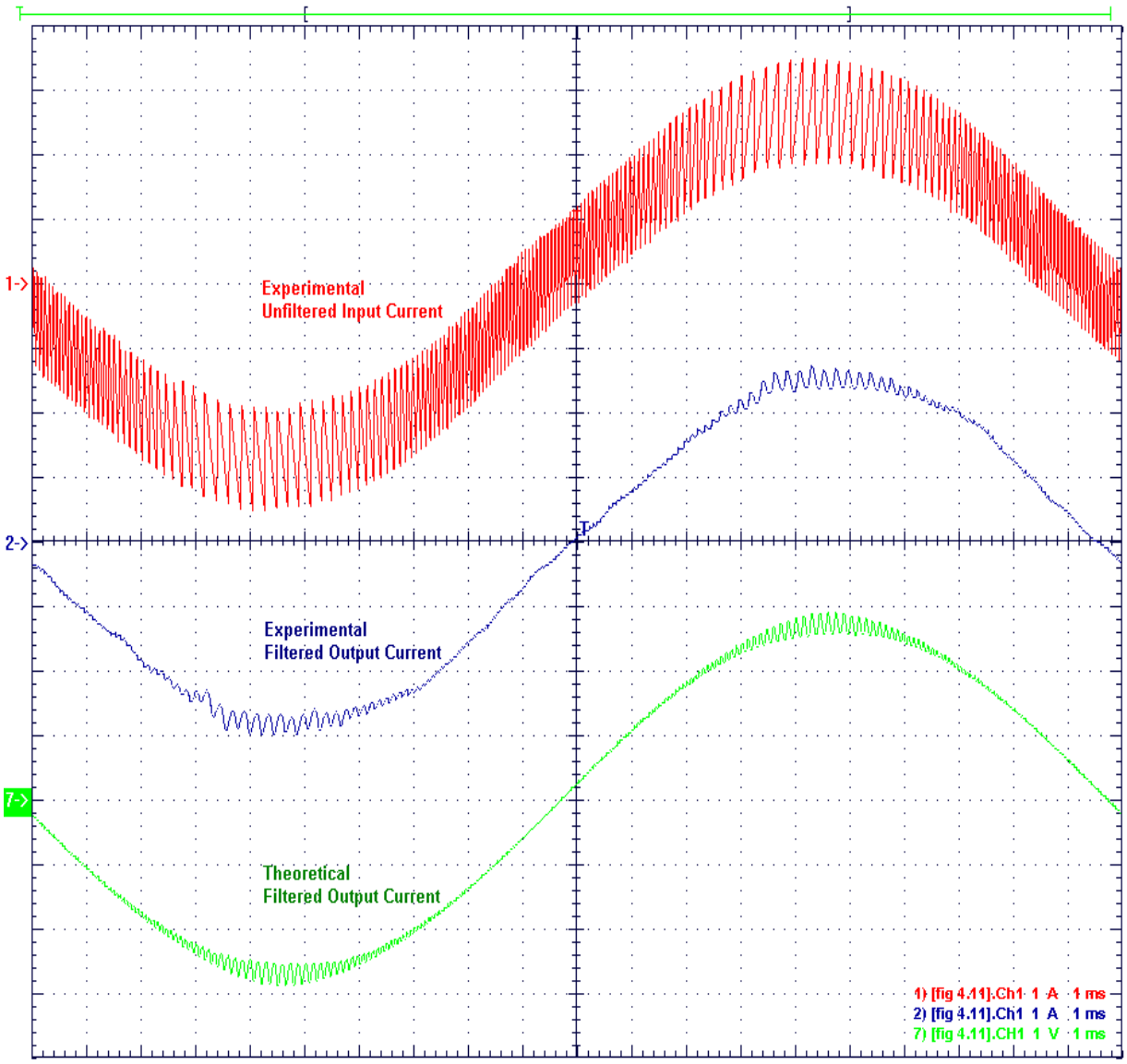


Figure 4.11: Theoretical and Experimental LCL Filter Effect

The effect of the LCL ripple filter is illustrated in figure 4.11. There is good correlation between experimental and practical current ripple attenuation results.

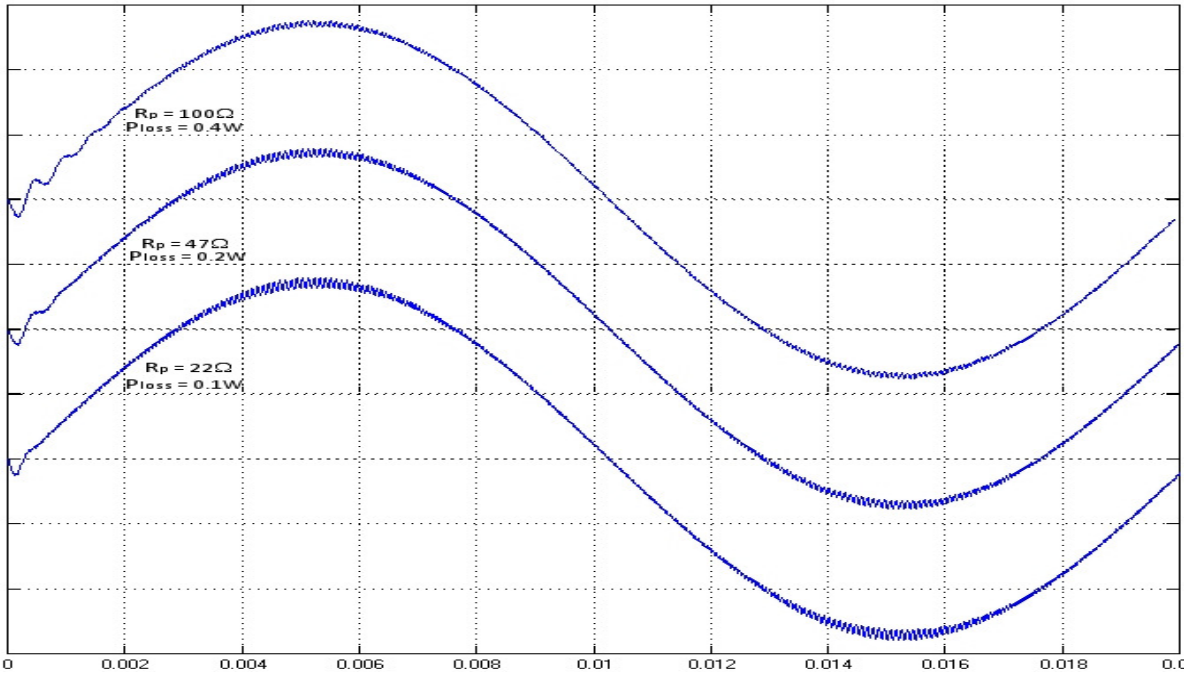


Figure 4.12(a): Damping Performance of R_p(simulated)

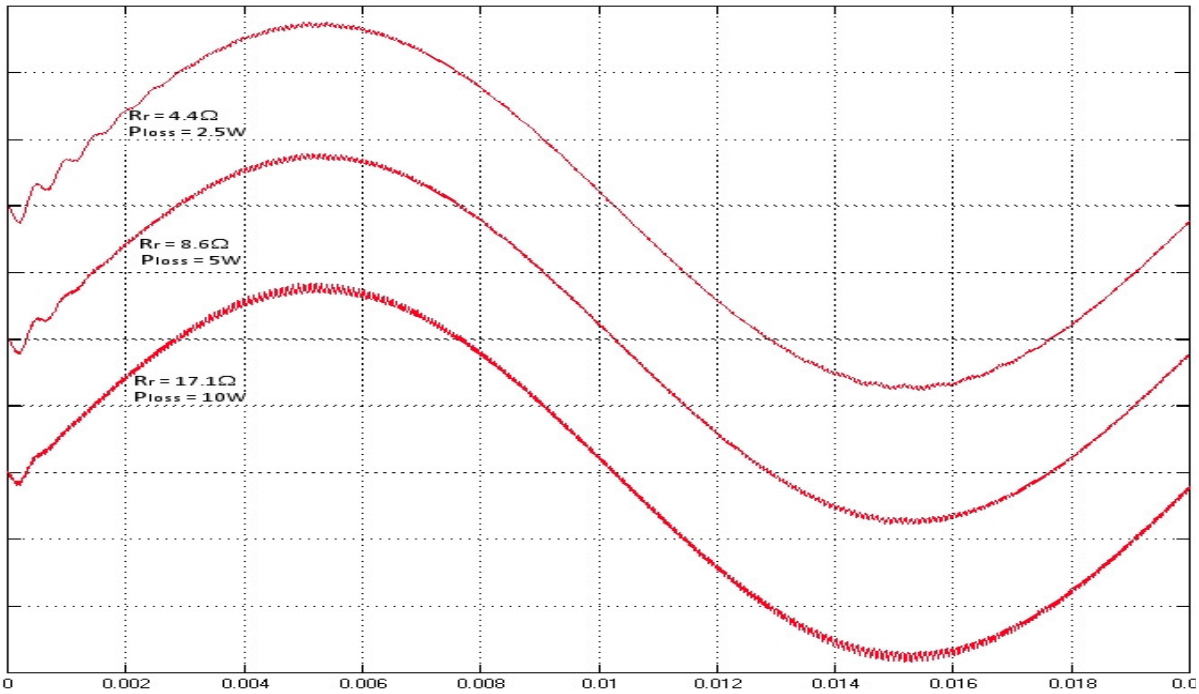


Figure 4.12(b): Damping Performance of R_r(simulated)

Figures 4.12(a) and 4.12(b) confirm that R_p can provide damping at much lower power loss in comparison to resistor R_r.

4.6 Expected Switching Loss Reduction with Unipolar Switching

Generally in the case of bipolar switching, for each hysteretic cycle two transistors and two diodes would go through a switching cycle. In contrast, in the case of unipolar switching, generally for each hysteretic cycle only one transistor and one diode would go through a switching cycle. Therefore it would be expected that switching loss in the case of unipolar switching would be approximately half that of bipolar switching.

Predetermination of actual switching loss can only be carried out on a case by case basis using datasheet information for the devices (IGBT's) that are used to realise the inverter. As a first approximation it could be assumed that during turn-off the current through the IGBT remains constant at its on-state value while the voltage across it rises linearly to the DC bus voltage value. After that the current collapses linearly to zero.

This means that the switching energy loss during turn-off is given by [41]:

$$E_{off} = \tfrac{1}{2} V_c \cdot I \cdot t_{off} \qquad 4.24$$

where

V_c = *DC bus Voltage*

I = *on-state current*

t_{off} = *IGBT turn-off time*

Similarly during turn-on, as a first approximation it could be assumed that current rises linearly to its on-state value while the voltage across the IGBT remains equal to the DC bus voltage.

This means that the switching energy loss during turn-on is given by:

$$E_{on} = \tfrac{1}{2} V_c \cdot I \cdot t_{on} \qquad 4.25$$

where

t_{on} = *IGBT turn-on time*

For inverters of one or two kVA rating (t_{on} +t_{off}) will be of the order of one or two microseconds. This means that, neglecting savings associated with diode switching, and assuming an average switching frequency of 5kHz, a power saving in the order of 10W is to be expected if unipolar switching is adopted. This estimate is based on V_c being 400V and the average on-state current being 5A. Considering that the full load efficiency of grid-connected inverters is typically around 90%, a power loss reduction of around 1% is significant. While the cost to achieve this loss reduction is practically zero, the benefits would be seen in the form of reduced cooling requirements and increased efficiency. Unipolar switching is analysed in detail in the next two sections.

4.7 Unipolar Switching (without Ripple Filter)

A Simulink® model of the ideal unipolar switched inverter is shown in figure 4.13. Figure 4.13 is similar to figure 4.2 except that the inverter block, which is now unipolar switched, is designed to satisfy the rules of logic defined in table 4.2. The ripple filter, which will be considered later, has been left out.

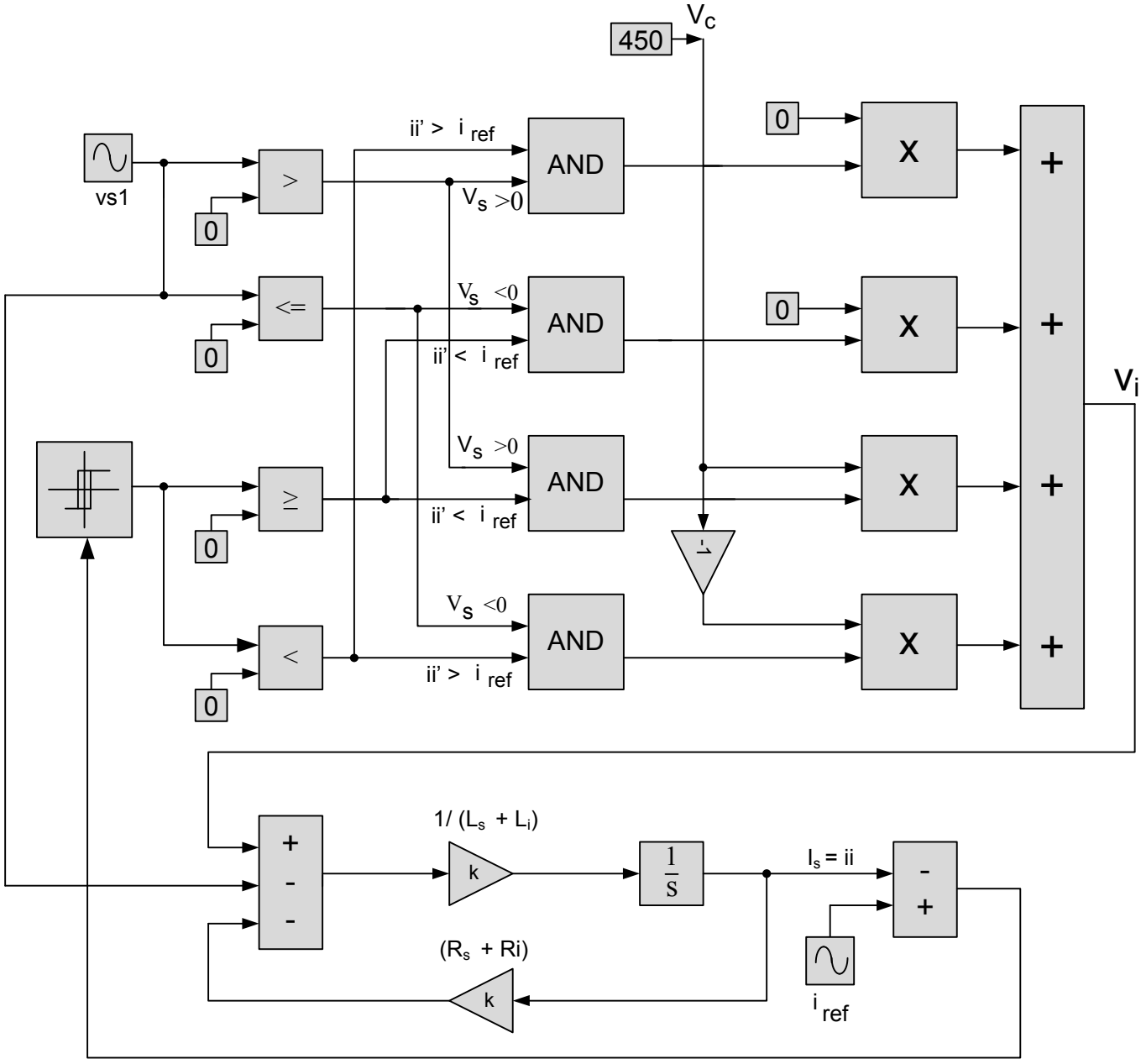


Figure 4.13: Unipolar Switched Inverter Model

Table 4.2: Unipolar Switching Logic

Current Error $(i_i - i_{ref})$	**Value of** v_s	**Inverter output** v_i
$(i_i - i_{ref}) \geq (I_{tol}/2)$	$v_s \geq 0$	0
$(i_i - i_{ref}) \leq (-I_{tol}/2)$	$v_s \geq 0$	V_c
$(i_i - i_{ref}) \geq (I_{tol}/2)$	$v_s < 0$	$-V_c$
$(i_i - i_{ref}) \leq (-I_{tol}/2)$	$v_s < 0$	0
$(-I_{tol}/2) < (i_i - i_{ref}) < (I_{tol}/2)$	any v_s	No change

As in the bipolar case, unipolar inverter switching is modelled by the relay block which operates as shown in figure 4.13. When the current error $(i_i - i_{ref})$ reaches the bottom limit of the tolerance band, the output of the relay changes state and the voltage across the series combination made up of L_s, $(R_s + R_i)$ and L_i is equal to $(v_c - v_s)$. On the other hand when the current error $(i_i - i_{ref})$ reaches the top limit of the tolerance band, the output of the relay changes state and the voltage across the series combination, as shown above in figure 4.13, is $-v_s$. The values of L_s, $(R_s + R_i)$ and L_i used in the bipolar case were retained.

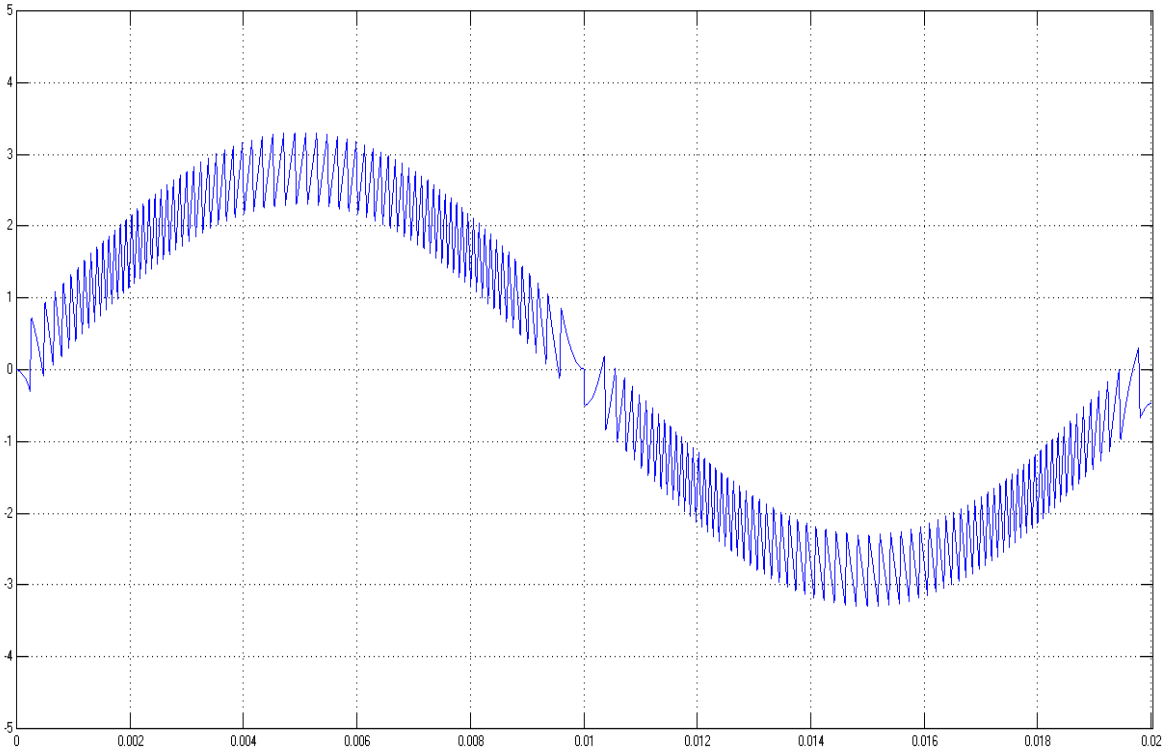


Figure 4.14: Theoretical Unfiltered Unipolar Operation (I_i = 2A)

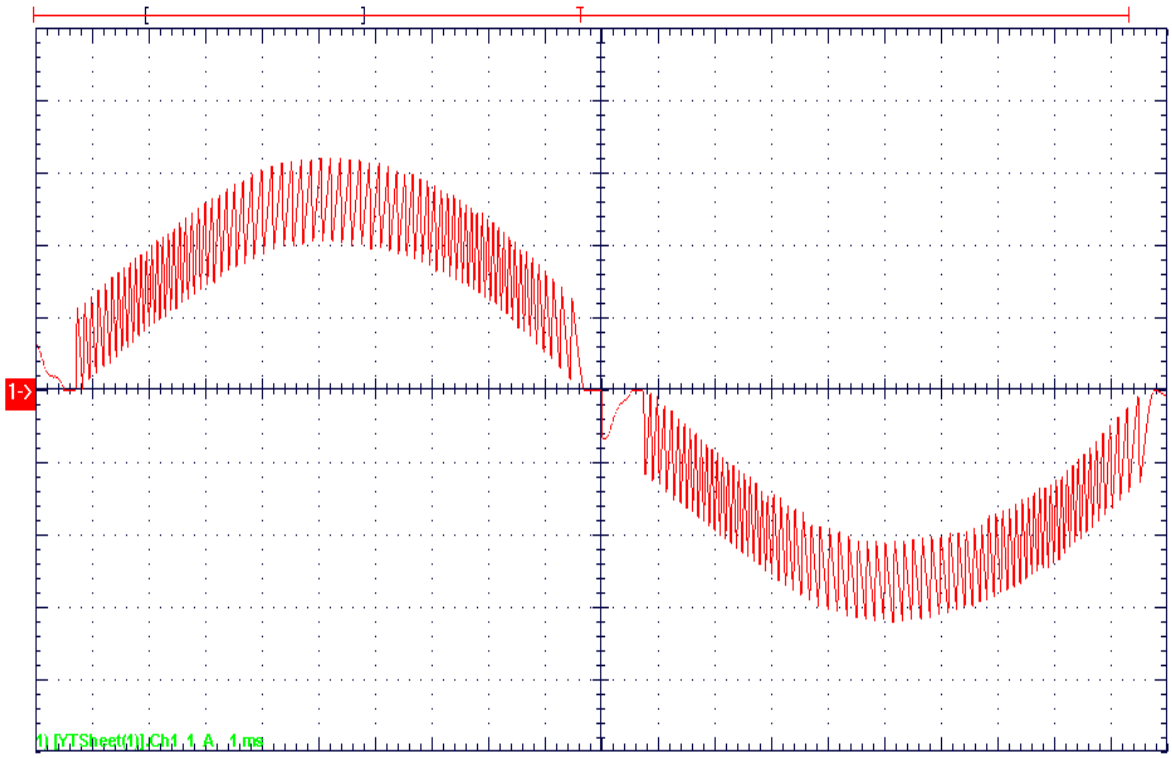


Figure 4.15: Experimental Unfiltered Unipolar Operation (I_i = 2A)

Figures 4.14 and 4.15 are respectively theoretical prediction and corresponding test results for a reference current of 2A. Correlation between them is reasonable, but not as good as in the bipolar case. The following observations can be made:

(a) The theoretical switching frequency near the peak of v_s is similar to the bipolar case. This is to be expected since the frequency is mainly determined by the so-called 'voltage headroom' which is (v_c - $v_{s(peak)}$) in both cases.

(b) While the lowest frequency of switching occurs near the peak of v_s in the bipolar case, in the unipolar case the lowest frequency occurs at, or near, the zero crossing of v_s. This is to be expected because near the zero crossing of v_s the switching frequency in the unipolar case is directly proportional to v_s. The low switching frequency near the zero crossing of v_s has a detrimental effect on the performance of the ripple filter. This will be illustrated in the next section.

4.8 Unipolar Switching (with Ripple Filter)

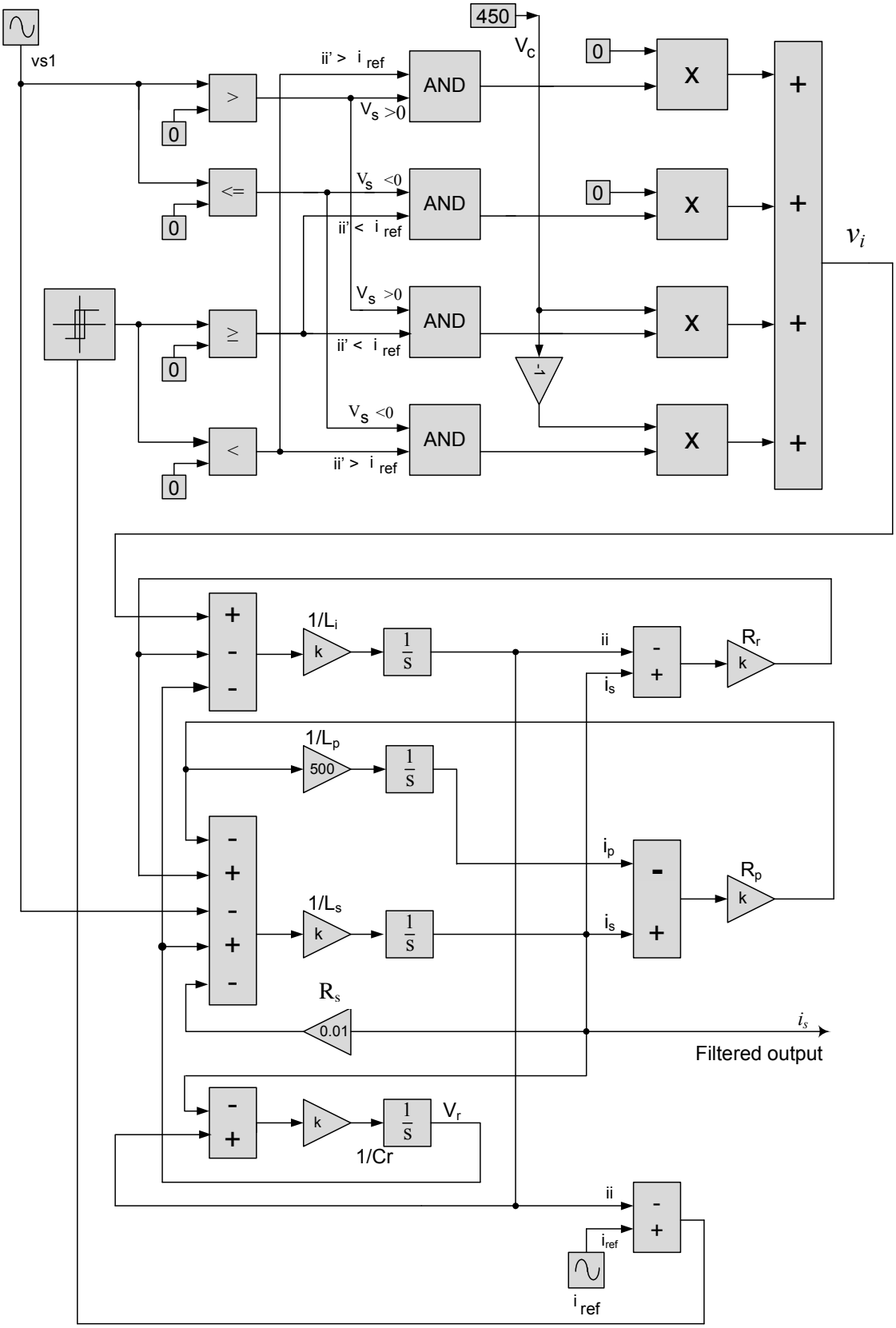


Figure 4.16: Unipolar Switched Inverter Model (with ripple filter)

Figure 4.16 is a block diagram of the Simulink® model of the unipolar switched inverter including the ripple filter. Figures 4.17 and 4.18 show the predicted and experimental waveform for current i_s. Both of these waveforms illustrate the unacceptable distortion which characterises unipolar switched inverters. Since distortion in the injected current waveform occurs near the AC supply voltage zero crossing and there is no such distortion present in the case of bipolar switching, it is worthwhile looking at the possibility of a mixed-mode switching system. If bipolar switching was restricted to a small time interval near the zero crossing of v_s, the efficiency advantage of unipolar switching could be retained while maintaining distortion well within acceptable limits.

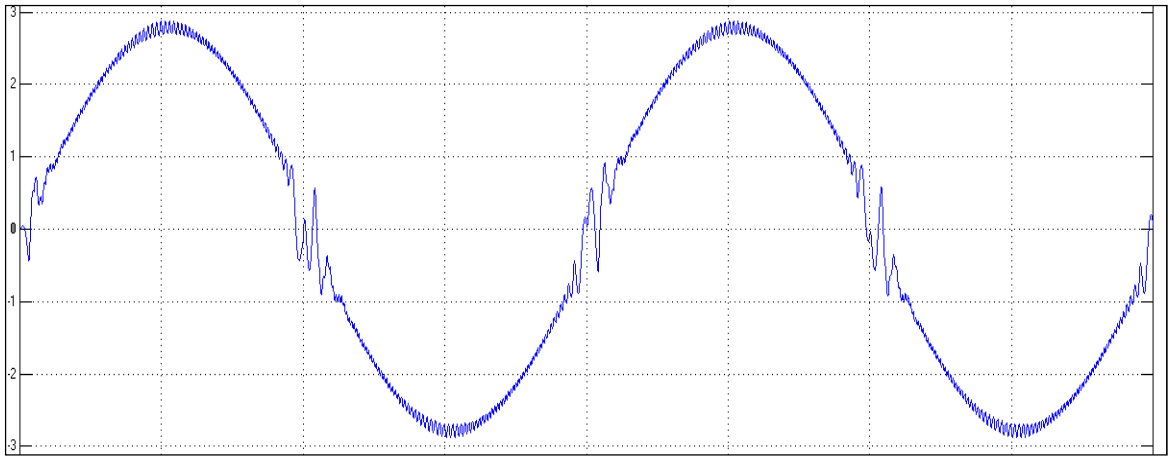


Figure 4.17: Theoretical Filtered Unipolar Operation, (I_i = 2A)
L_i=10mH, L_p=2mH, C_r=2µF, R_p=47Ω

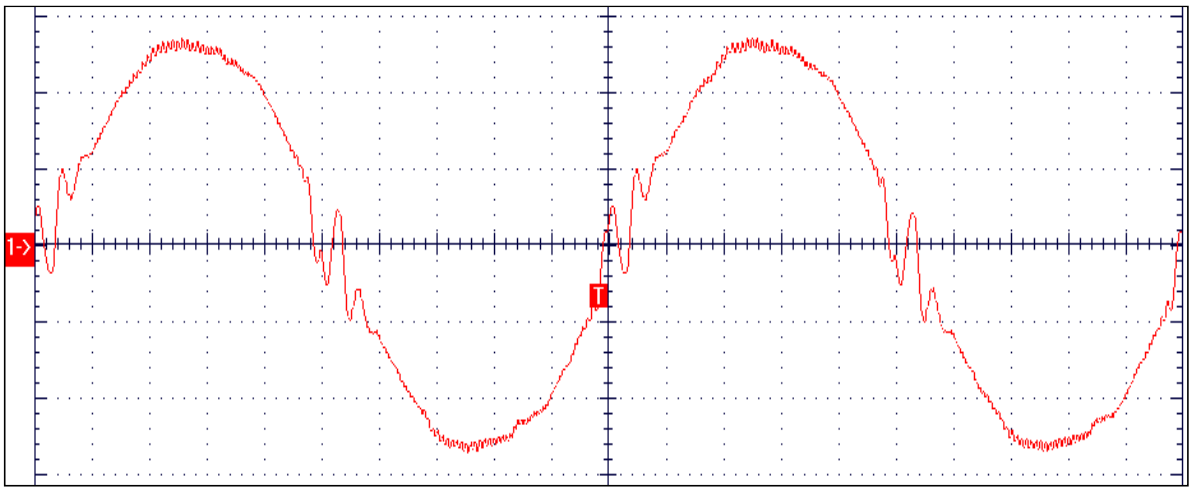


Figure 4.18 Experimental Filtered Unipolar Operation (I_i = 2A)
L_i=10mH, L_p=2mH, C_r=2µF, R_p=47Ω

4.9 Mixed Bipolar and Unipolar Switching

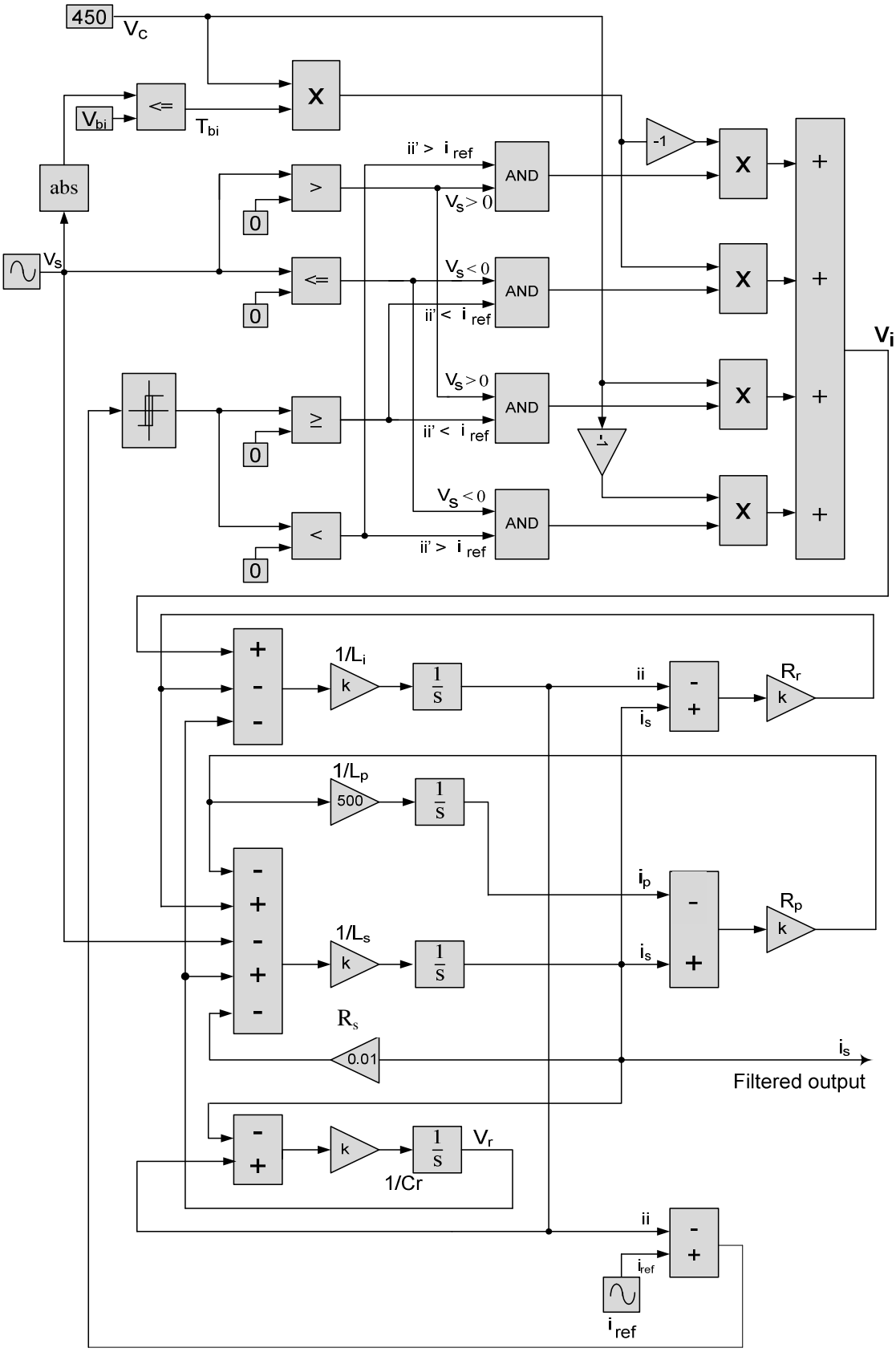


Figure 4.19: Mixed-mode Inverter Block Diagram

The mixed-mode selector block is configured to satisfy the rules of logic defined in table 4.3. Typically the value of V_{bi} would be such that bipolar switching is used for only about one-tenth of the power frequency period.

Table 4.3: Mixed-mode Switching Logic

Current Error $(i_i - i_{ref})$	**Value of** v_s	**Inverter output** v_i
$(i_i - i_{ref}) \geq (I_{tol}/2)$	$v_s > V_{bi}$	0
$(i_i - i_{ref}) \leq (-I_{tol}/2)$	$v_s > V_{bi}$	V_c
$(i_i - i_{ref}) \geq (I_{tol}/2)$	$-V_{bi} \geq v_s \leq V_{bi}$	$-V_c$
$(i_i - i_{ref}) \leq (-I_{tol}/2)$	$-V_{bi} \geq v_s \leq V_{bi}$	V_c
$(i_i - i_{ref}) \geq (I_{tol}/2)$	$v_s < -V_{bi}$	$-V_c$
$(i_i - i_{ref}) \leq (-I_{tol}/2)$	$v_s < -V_{bi}$	0
$(-I_{tol}/2) < (i_i - i_{ref}) < (I_{tol}/2)$	any value	No change

Figure 4.20 shows the nature of signal T_{bi} . When it is high the inverter operates in bipolar mode. When it is low the inverter operates in unipolar mode. Since switching, in the unipolar case, practically stops when $|i_{ref}|$ becomes less than $I_{tol}/2$, transition to bipolar switching is designed to take place when $|i_{ref}|$ is near $I_{tol}/2$. This is done by making k in figure 4.20 equal to at least $I_{tol}\widehat{V_s}/2$. Thus the minimum period of bipolar switching is introduced to reduce distortion in the injected current.

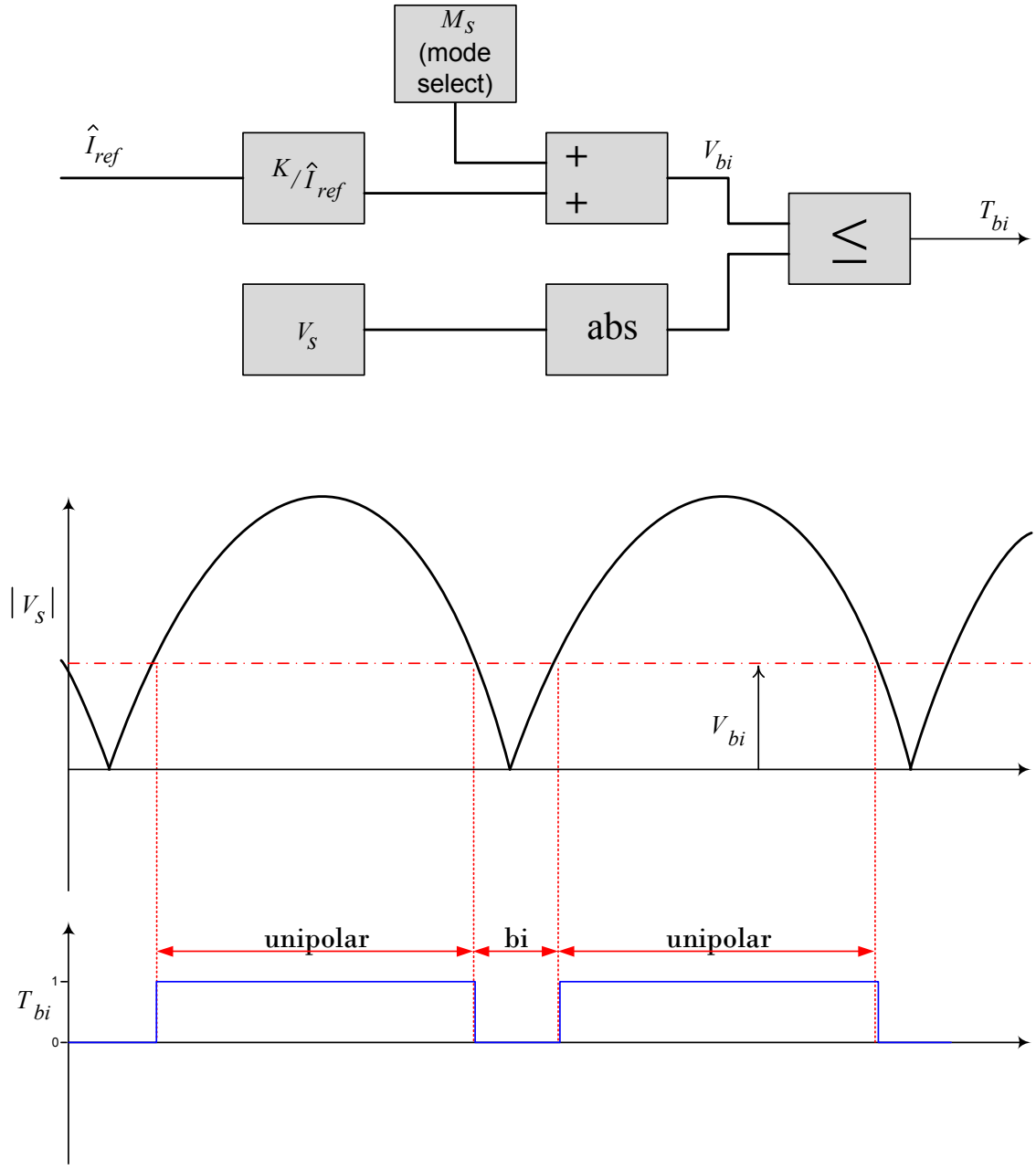


Figure 4.20: Mixed-mode Selector Block Diagram

The mode selector, detailed in figure 4.20 allows the selection of unipolar switching, bipolar switching or mixed mode switching. For unipolar switching, M_s is chosen to be a large enough negative number so that T_{bi} is always true. For bipolar switching, M_s is chosen to be a large enough positive number so that T_{bi} is always false. For mixed-mode switching M_s should be set to zero.

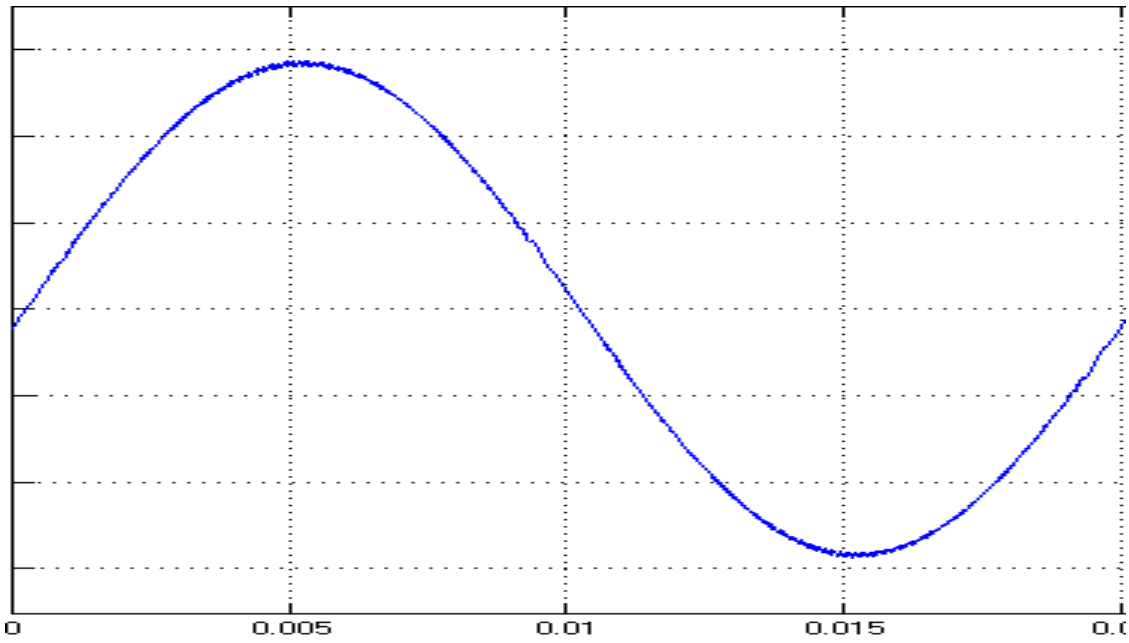


Figure 4.21: Theoretical Mixed-mode Output (no delay)

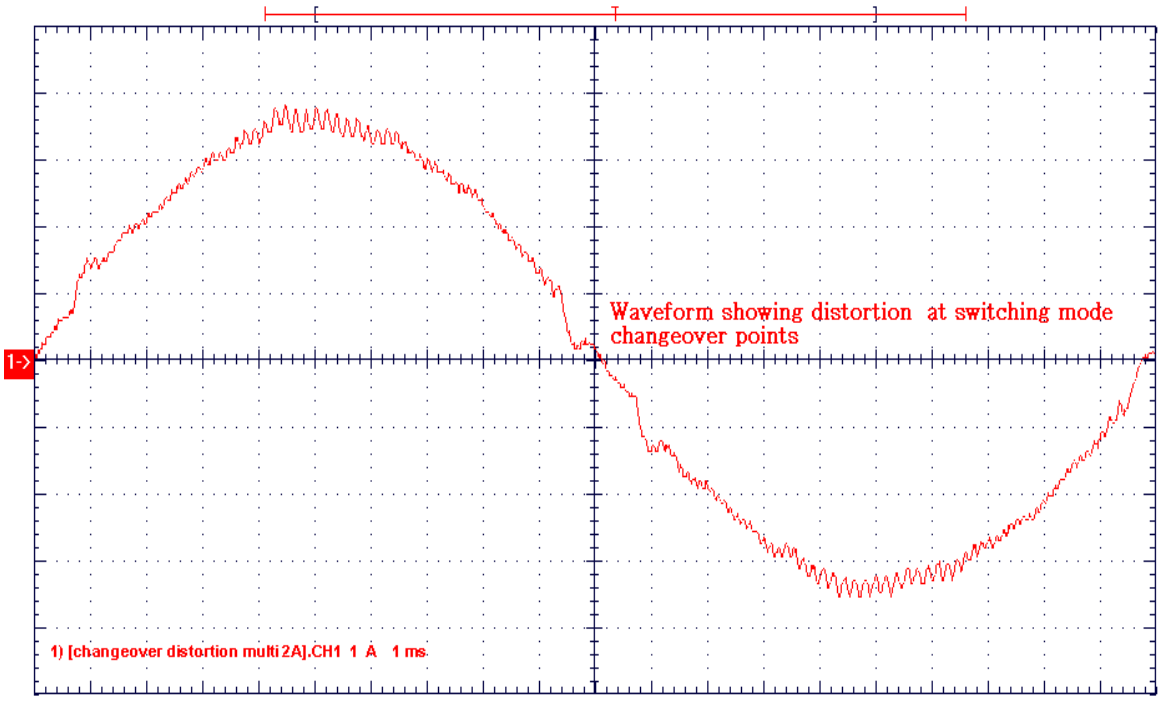


Figure 4.22: Experimental Mixed-mode Output

Figures 4.21 and 4.22 show the theoretical and experimental results for the mixed-mode case. A significant discrepancy is the distortion occurring at the transition between unipolar and bipolar switching and vice versa. The experimental ripple content is also more than expected. It was suspected that a major reason for this would be delayed switching caused by various circuit imperfections and dead-time. Comparison between figure 4.18 and 4.22 confirms that mixed-mode operation has the advantage of reduced distortion near the zero-crossing of the supply voltage.

4.10 The Effect of Delay

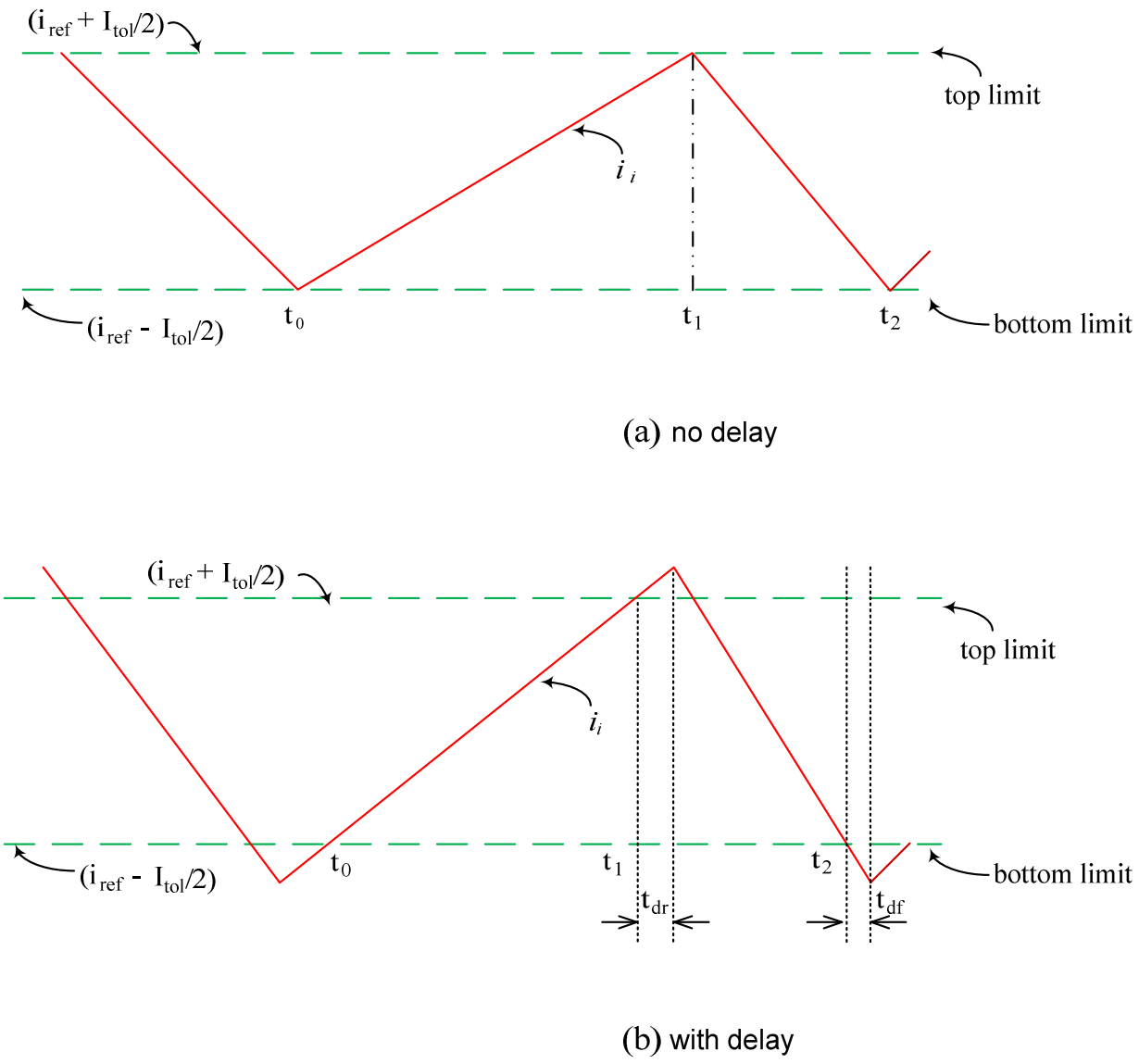


Figure 4.23: Effects of Switching Delay

Refer to figure 4.23 which represents the current (i_i) through the current steering inductor and the top and bottom limits of the tolerance band. Note that the current axis is vertical and the time axis is horizontal. Although the tolerance band limits are shown as horizontal, in practice they will generally have a positive or negative slope. Assuming that slope is zero does not lead to significant error [31].

Figure 4.23(a) shows the case of zero delay. Inverter devices are switched as soon as current i_i reaches one of the tolerance band limits. For example, assuming the inverter is operating at unity power factor and is being unipolar switched, at instant t_1 in figure 4.23(a) transistor T_{A+} will be switched off and straight after that diode D_{A-} will carry current i_i. At instant t_2 transistor T_{A+} will be switched on and current i_i will immediately transfer from D_{A-} to T_{A+}.

Figure 4.22(b) illustrates what happens in the case where there is switching delay. As before current i_i reaches the upper limit of the tolerance band at instant t_1. A finite time t_{dr} elapses before current i_i flows in diode D_{A-} . This finite time, which in practice is of the order of one to a few microseconds, may be due to current sensor delay and signal processing delays such as comparator delays, gate drive delays and transistor turn-off times. Similarly current i_i reaches the lower limit of the tolerance band at t_2 . A finite time t_{df} elapses before current i_i flows in transistor T_{A+}. As before this finite delay will be of the order of one to a few microseconds.

As shown in figure 4.22(b), as a result of delay, instead of current i remaining within the tolerance band, it goes outside the band for a finite amount of time. If there was no delay current i_i changes practically linearly, between $(i_{ref} - I_{tol}/2)$ and $(i_{ref} + I_{tol}/2)$. Therefore the value of current i_i , averaged over one switching cycle is i_{ref}. On the other hand if there is switching delay then current i_i , in the unipolar case, changes linearly between $(i_{ref} - I_{tol}/2) - v_s\, t_{df}/L_i$ and $(i_{ref} + I_{tol}/2) + (V_c - v_s)\, t_{dr}/L_i$. The expressions in the previous sentence are based on the reasonable assumption that the voltage across the ripple filter capacitor (C_r) is very close to the AC supply voltage v_s.

From the previously stated expressions it can be deduced that current i_i , averaged over one hysteretic cycle is given by:

$$i_{\,i(average)} = \; i_{ref} - \frac{v_s(t_{dr}+t_{df})}{2L_i} + \frac{V_c t_{dr}}{2L_i} \qquad 4.26$$

Equation 4.26 is valid for the positive half cycle of the reference current. Equation 4.27 can be arrived at by using similar reasoning to that used for equation 4.26 and is valid for the negative half cycle of the reference current:

$$i_{\,i(average)} = \; i_{ref} - \frac{v_s(t_{dr}+t_{df})}{2L_i} - \frac{V_c t_{dr}}{2L_i} \qquad 4.27$$

Ideally current i_i when averaged over hysteretic cycle must be equal to the current reference i_{ref}. However delayed switching causes two additional components to be part of current i_i. The first is a sinusoidal component which is in phase opposition to v_s and whose peak value is equal to $\widehat{V_s}(t_{dr} + t_{df})/L_i$. The second component is a symmetrical power frequency square wave whose peak value is $V_c\, t_{dr} / L$.

4.11 The Effect of Delay: Bipolar Switching

Figure 4.22(b) is still applicable. In the bipolar case current i_i changes approximately linearly between $(i_{ref} - I_{tol}/2) - (v_c + v_s)t_{df}/L_i$ and $(i_{ref} + I_{tol}/2) + (v_c - v_s)\, t_{dr}/L_i$. Again the expressions in the previous sentence are based on the assumption that the voltage across the ripple filter capacitor is practically equal to the AC supply voltage v_s. From the stated expressions it can be deduced that current i_i averaged over one hysteretic cycle is given by:

$$i_{i(av)} = i_{ref} - \frac{V_c(t_{df} - t_{dr})}{2L_i} - \frac{v_{s(}t_{dr+}t_{df)}}{2L_i} \qquad 4.28$$

Equation 4.28 is valid for the positive half cycle of the reference current. Equation 4.29 can be arrived at by using similar reasoning to that used for equation 4.28 and is valid for the negative half cycle of the reference current.

$$i_{i(av)} = i_{ref} + \frac{V_c(t_{df} - t_{dr})}{2L_i} - \frac{v_{s(}t_{dr+}t_{df)}}{2L_i} \qquad 4.29$$

As in the unipolar case, $i_{i(av)}$ contains two components that are due to switching delay. The first is a sinusoidal component which is identical to the one that appears in the unipolar switching case. The power frequency square wave component is much smaller in the case of bipolar switching. This is because t_{dr} is practically equal to t_{df}.

4.12 Modelling of Switching Delay

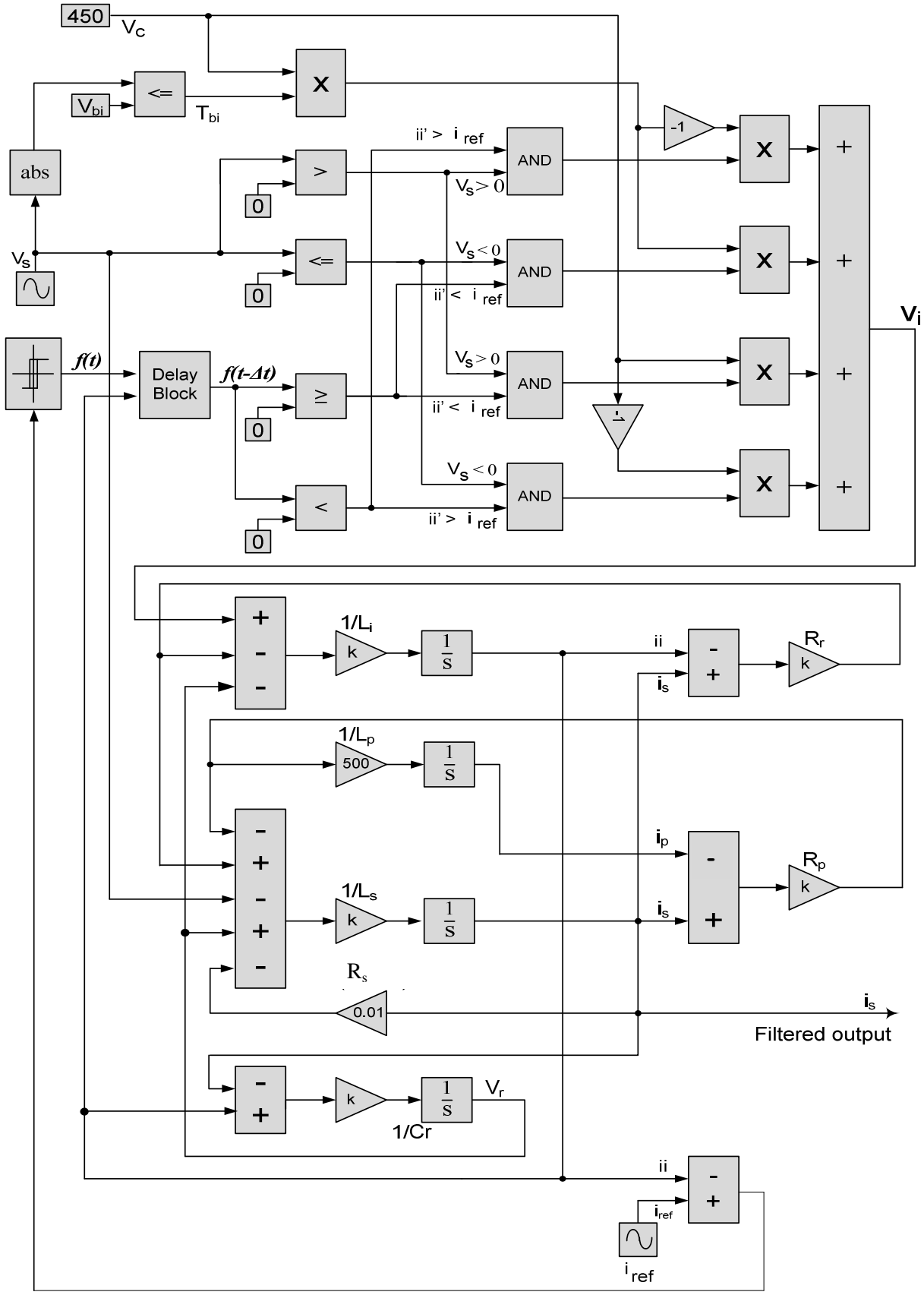


Figure 4.24: Mixed-Mode Inverter Simulink® model with Switching Delay Included

The inverter model, which is shown in figure 4.24, has been modified to incorporate delay. As before the output changes state as soon as current i_i crosses one of the tolerance band boundaries. However the effect of this is delayed according to the logic embedded in the delay block. Details of the delay block are given in figure 4.25. When current $|i_i|$ goes up a pair of transistors carry the current. When current $|i_i|$ comes down a pair of diodes (bipolar case) or a diode and a transistor (unipolar case) carry the current. Delay t_{dr} represents the time interval from the instant current $|i_i|$ as it rises, reaches the boundary of the tolerance band to the time when current i_i transfers from one transistor to a diode (unipolar case) or from a pair of transistors to a pair of diodes (bipolar case). Delay time t_{df} represents the time interval from the instant when current $|i_i|$, as it falls, reaches the boundary of the tolerance band to the time when current i_i has transferred from a diode to a transistor (unipolar case) or from a pair of diodes to a pair of transistors (bipolar case).

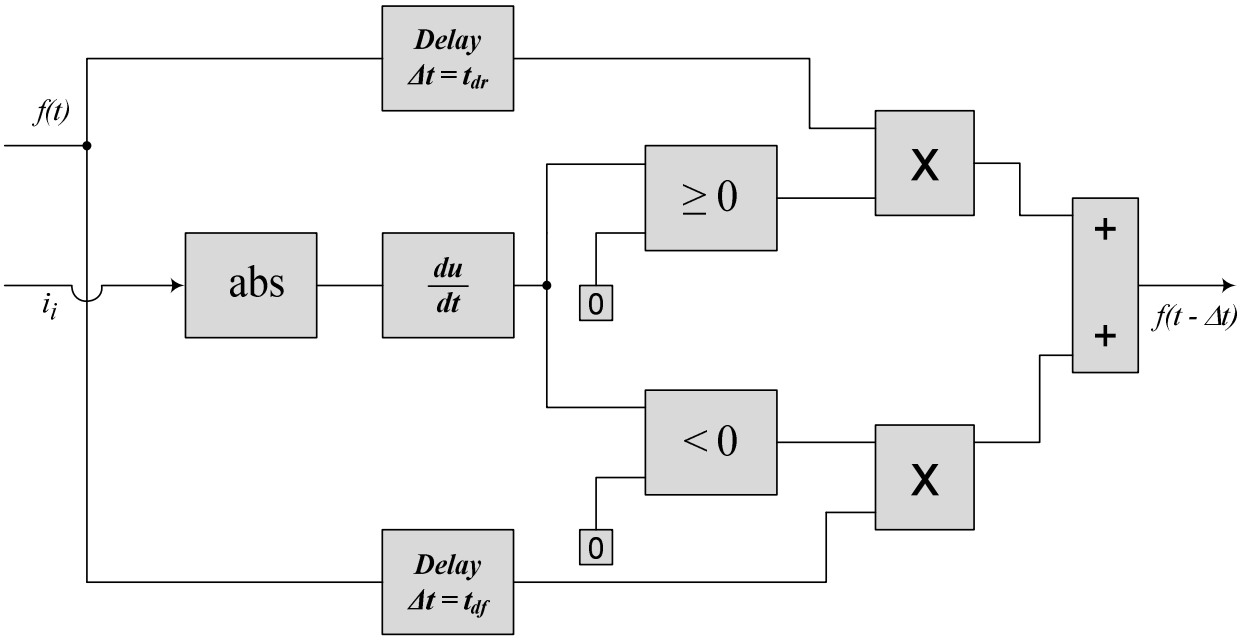


Figure 4.25: Simulink® Block Representing Switching Delay in figure 4.24

4.13 Compensation for the Effect of Delay

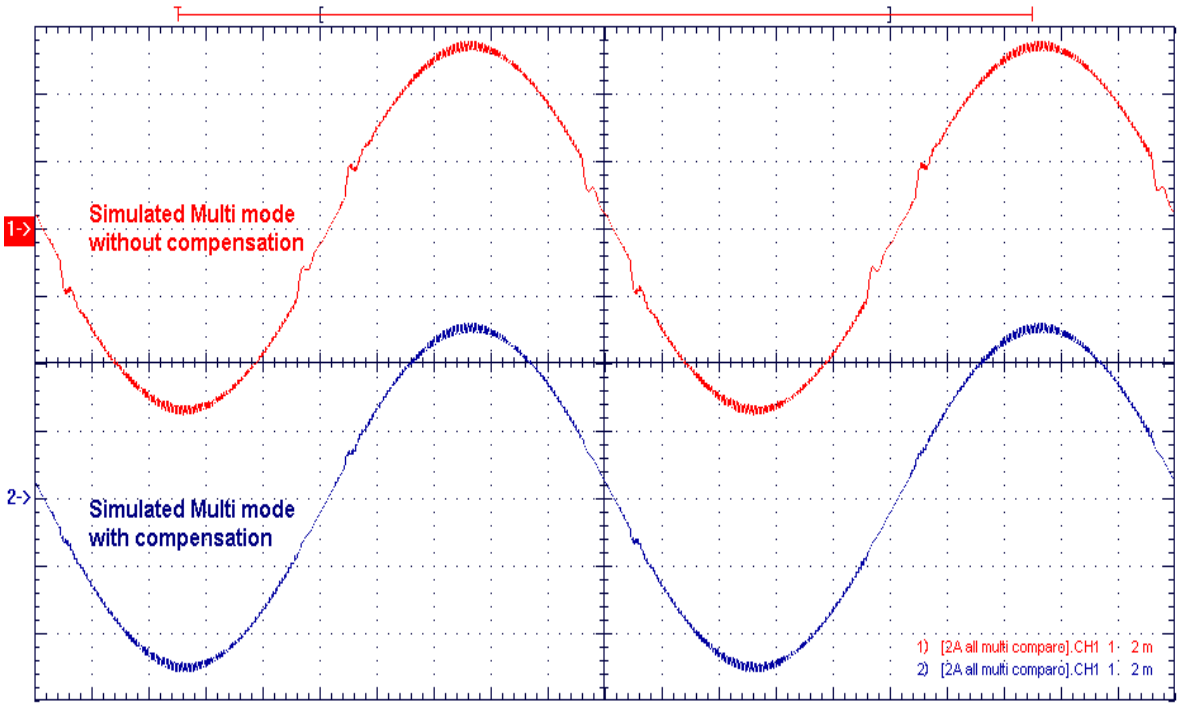


Figure 4.26: Simulated 2A Mixed-mode Operation with Switching Delay of 5µs

Figure 4.26 shows the simulated output waveforms with I_{ref} equal to 2A. The corresponding magnitude spectra are shown in figure 4.27. The odd harmonics, similar to those of a quasi-square wave, as predicted by equations 4.26 and 4.27, are prominent in the unipolar case or in the uncompensated mixed-mode case. The bipolar case is practically free of low frequency harmonics as predicted by equation 4.28 and 4.29.

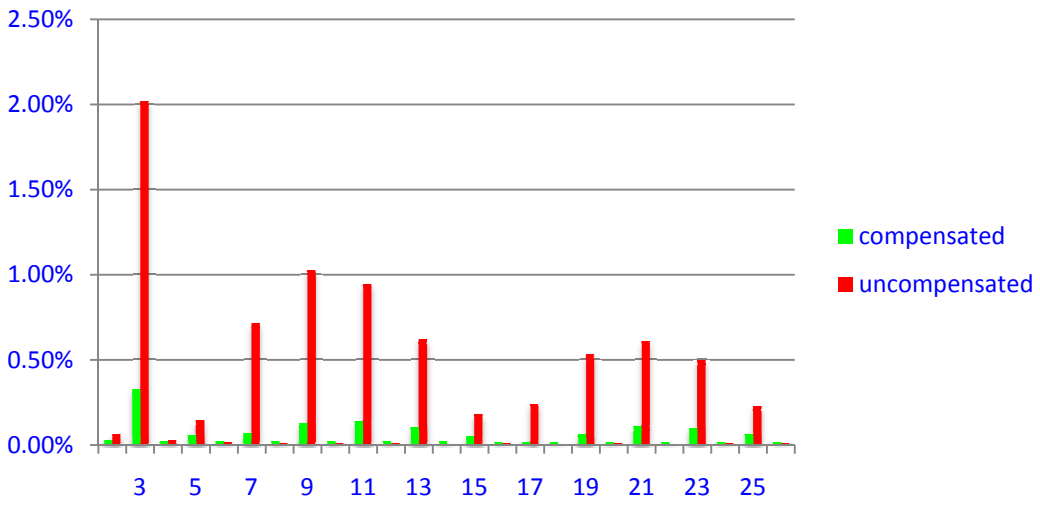


Figure 4.27: Harmonic Content Comparison at 2A with and without Compensation

Figure 4.26 shows that even the mixed mode case is affected by switching delay. In particular switching delay causes ripple filter transients at the time when switching changes from unipolar to bipolar and vice-versa. From the point of view of current $i_{i(av)}$, which is defined as the current through inductor L_i averaged over one hysteretic cycle, the presence of the filter transients is not surprising. Equations 4.26, 4.27, 4.28 and 4.29 predict that there is a step change in current $i_{i(av)}$, of approximately $V_c \cdot t_{dr} / L_i$ every time there is a transition from unipolar switching to bipolar switching and vice-versa.

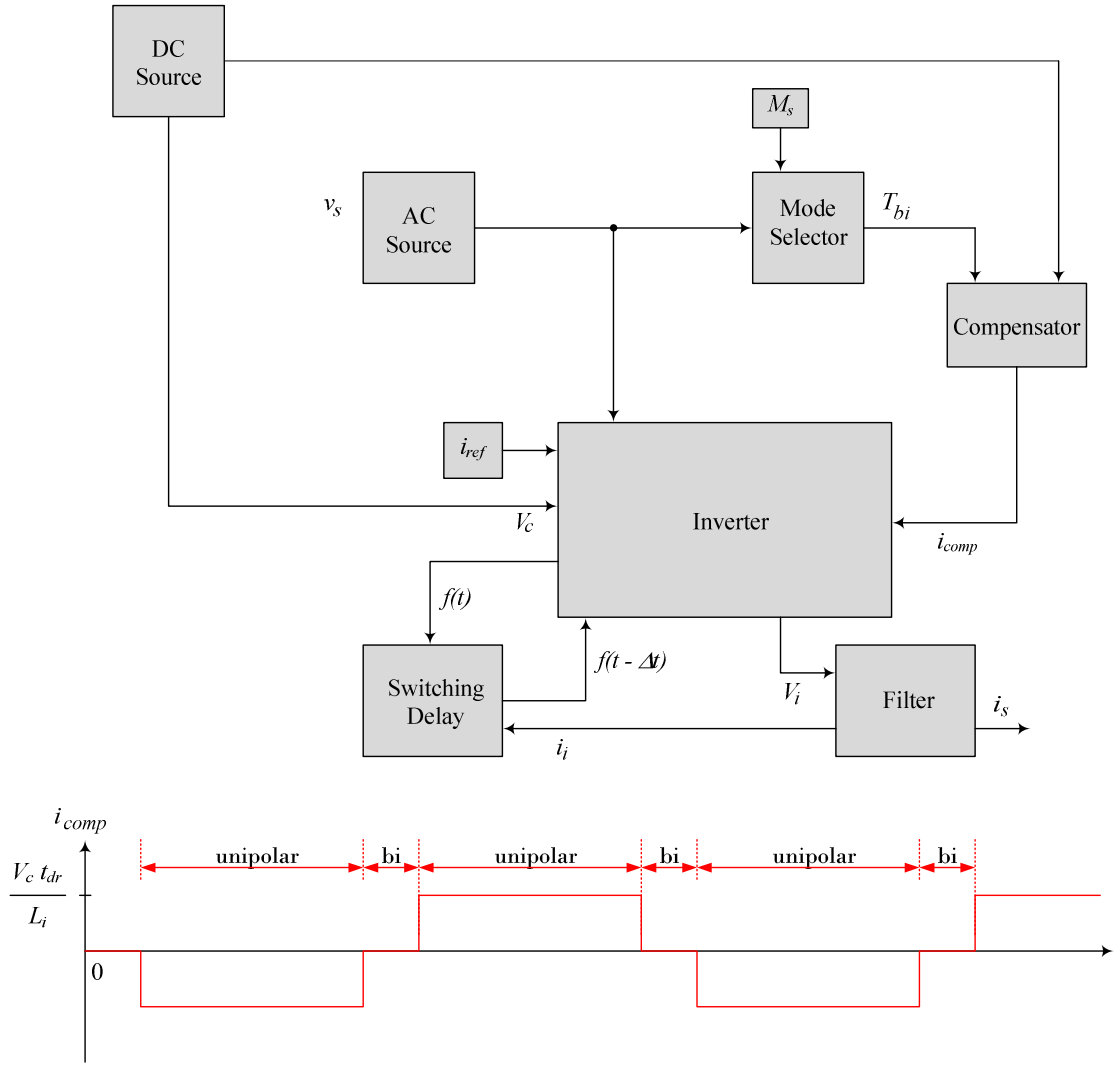


Figure 4.28: Mixed-mode Inverter Block Diagram with Delay and Compensation

It is these step changes that cause the ripple filter transients. A way of eliminating filter transients caused by switching delay is to inject a component of current equal in magnitude to $-(V_c\ t_{dr}/L_i)\ sgn(v_s)$ when the inverter is operating in unipolar mode. As shown in figure 4.28 this additional injected current must be zero when the inverter is operating in bipolar mode. The compensator block which was used as a part of the overall Simulink® model is also shown in figure 4.28.

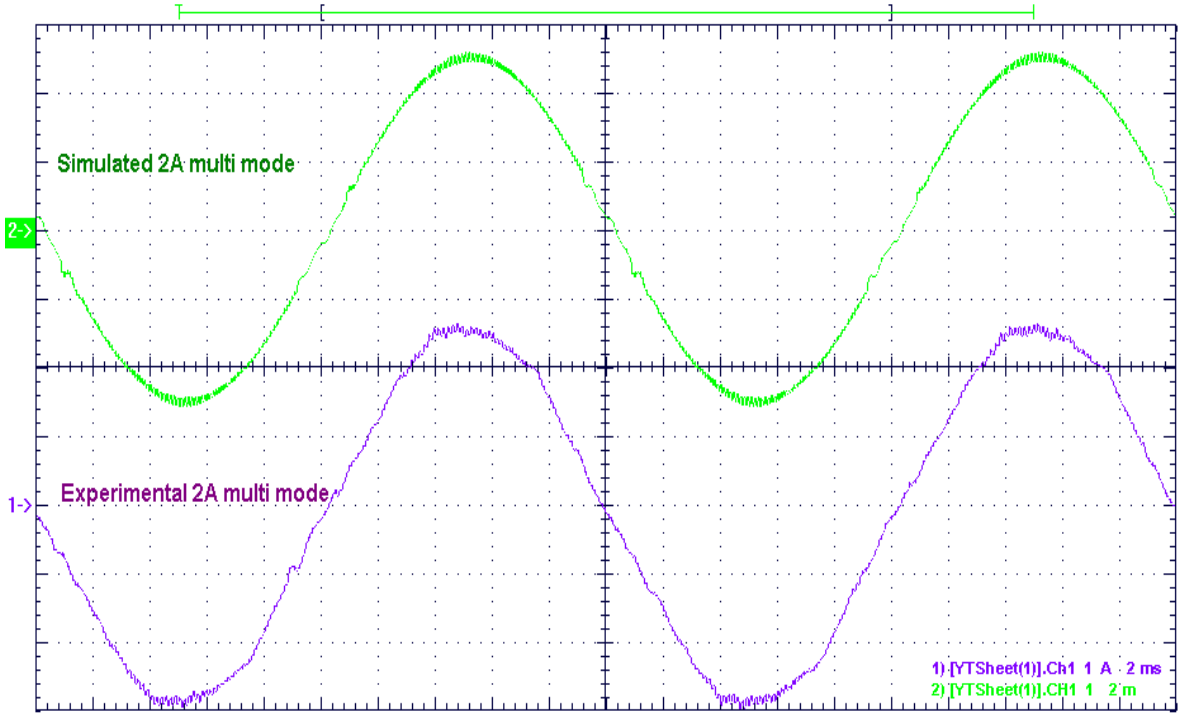


Figure 4.29: Simulated and Experimental Mixed-mode 2A Operation with Delay and Compensation

A comparison of predicted and experimental mixed-mode inverter output waveforms is shown in figure 4.29. Clearly, compensation as described in this section, results in significant improvement in quality of the inverter output current. A delay value of 5µs was used to achieve the simulated waveform shown in figure 4.29 above.

4.14 Thermal Tests

Thermal tests were carried out to practically illustrate reduced inverter losses in the case of unipolar and mixed-mode switching. For fair and meaningful comparison all tests were carried out with DC bus voltage equal to 410V, AC supply voltage 247V and the reference current I_{ref} equal to 2.5A. The tolerance band was adjusted so that in all the tests that were carried out the switching frequency averaged over one mains frequency cycle was 10 kHz. For practical implementation details refer appendix A.6.

For the purpose of the test the power electronic modules used for the inverter were mounted on a single heat-sink. The heat-sink was naturally cooled to achieve reasonable temperature change. The rated value of the thermal resistance to ambient for the heat-sink was 0.29ºC/W [42]. This was verified by dissipating a known amount of DC power through the modules and measuring the steady state temperature increases of the heat-sink above ambient. The temperature was obtained from a thermocouple inserted into a specially drilled hole inside the heat-sink.

Results of the tests are given in table 4.4. Mixed-mode operation is clearly advantageous when compared to bipolar mode of operation. There is practically no sacrifice in efficiency in going from unipolar switching to mixed-mode switching. It is expected that at lower current levels (less than 1A), where the relative period of bipolar mode present in the mixed-mode operation is higher, the efficiency advantage is reduced.

Table 4.4: Thermal Test Results

Switching Topology	DC Bus Voltage	AC Supply Voltage	Inverter Output Current (A)	Steady State Heat-Sink Temperature (ºC)	Ambient Temperature (ºC)	Power loss through Heat-Sink (W)
Unipolar (10kHz Average)	410	247	2.5	37.7	25.2	43.07
Unipolar (10kHz Average)	410	247	2.5	36.7	24.3	42.75
Unipolar (10kHz Average)	410	247	2.5	35.4	22.8	43.32
Bipolar (10kHz Average)	410	247	2.5	42.3	25.3	58.63
Bipolar (10kHz Average)	410	247	2.5	42.6	25.7	58.39
Bipolar (10kHz Average)	410	247	2.5	42.35	25.8	58.46
Mixed-mode (10kHz Average)	410	247	2.5	35.3	22.8	43.15

4.15 Summary

This chapter has been a detailed comparison between unipolar and bipolar switched current controlled single-phase transformerless grid connected inverters. A ripple filter is a necessary system element to reduce switching frequency current harmonics to within acceptable levels.

It has been found that while unipolar switching has the advantage of reduced losses, it suffers from current distortion near the AC mains voltage zero crossing. In addition switching delay introduces low frequency harmonic content in the inverter output current, whose relative magnitudes are similar to those of a mains frequency square wave in phase with the AC supply voltage.

On the other hand, it has been confirmed both by simulation and by experimentation that bipolar switching does not have the two disadvantages mentioned above. However it does suffer higher switching losses.

A hybrid inverter switching strategy has been developed and practically implemented that has the higher efficiency advantage of unipolar switching and the better waveform quality of bipolar switching. This has been achieved by using unipolar switching for more than eighty percent of the time. For a short fraction of the 50Hz cycle, typically about 1ms from the zero crossing of the AC supply voltage, bipolar switching is used. This is to ensure that switching frequency remains high and consequently distortion near the zero crossing of the AC supply voltage is practically eliminated. It was found that switching delay caused ripple filter transients to occur at transition points between bipolar and unipolar switching. A compensation technique has been adopted which results in smoother transitions.

Chapter 5 DC Bus Voltage Control

5.1 Introduction

The previous chapter dealt with inverter current control which is the innermost control loop of the PV system. The reference current for that control loop has to correlate with the level of insolation since there is no significant energy storage between the output of the solar panels and the input of the inverter. A rise in insolation level must automatically result in a proportionate rise in the active component of the reference current. As shown in figure 5.1, the active component of the current reference, $k_h\, i_{pr}$, is the output of the DC bus voltage controller.

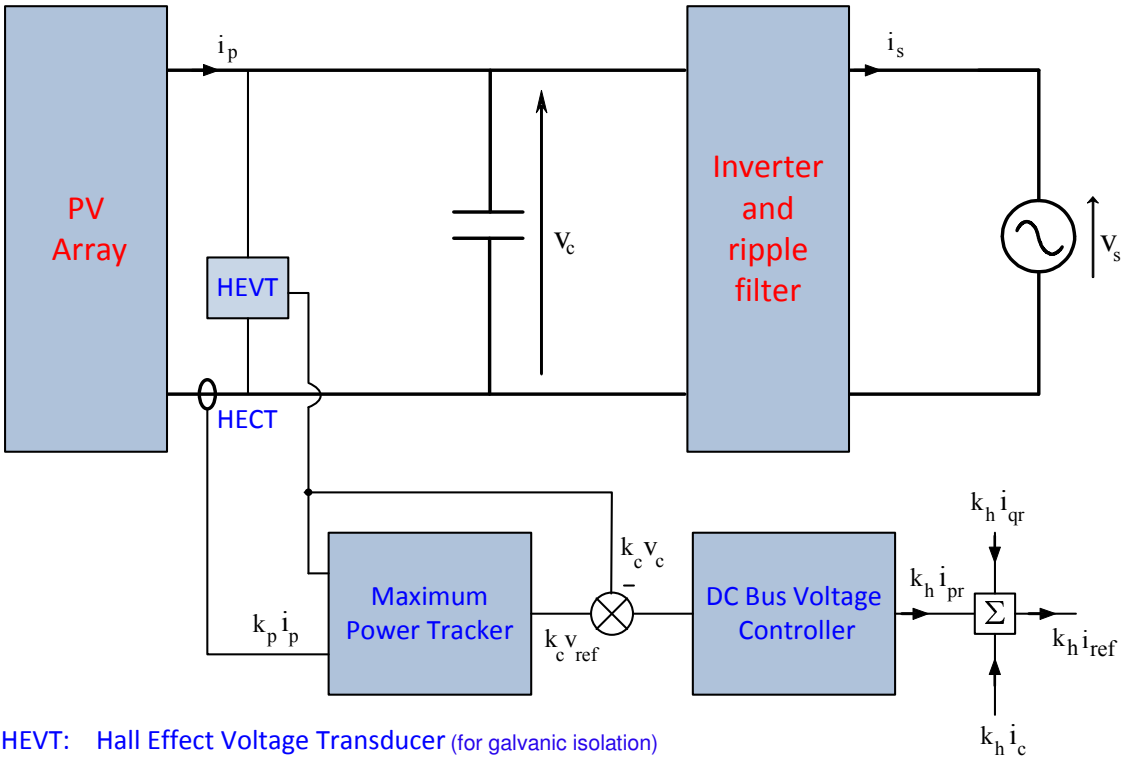


Figure 5.1: PV System Components

An increase in insolation level causes a temporary imbalance between power input from the panels to the DC bus bulk storage capacitor and power output from it to the inverter. This imbalance causes a rise in the DC bus voltage. To restore the DC bus voltage to its reference value the DC bus voltage controller raises the active component of the reference current. This in turn causes power injection into the AC mains to rise, thus restoring power balance for the capacitor. Similarly a decrease in insolation level results in the DC bus voltage controller imposing a lower active component of reference current. As shown in figure 5.1, the other components of the reference current are the DC offset correction current and possibly a reactive component for non-unity power factor operation. The next chapter is devoted to DC offset correction. In this chapter DC offset is assumed to be zero.

To achieve maximum energy extraction from the PV panels, the DC bus voltage has to be made a function of insolation level. This means that as insolation level changes, the reference voltage for the DC bus voltage controller must change accordingly. As is well-known, for any PV array, at a given level of insolation and ambient temperature, there is an optimum voltage at which the PV array should operate if maximum power is to be extracted. The purpose of the maximum power tracker, represented in figure 5.1, is to automatically adjust the voltage reference for the voltage controller so that maximum power is extracted from the PV array.

Details of maximum power tracker implementation are provided in the next section. DC bus voltage controller design and realisation are covered in section 5.3.

5.2 Maximum Power Tracker

The characteristics of the solar array are shown in figure 5.2. A flow chart representing the maximum power algorithm is presented in figure 5.3. At *First run* the maximum power tracker output, $k_c v_{ref}$, is set to a value equal to a preset number of incremental steps(ΔV,4V to minimise disturbance) away from the measured array open-circuit voltage.

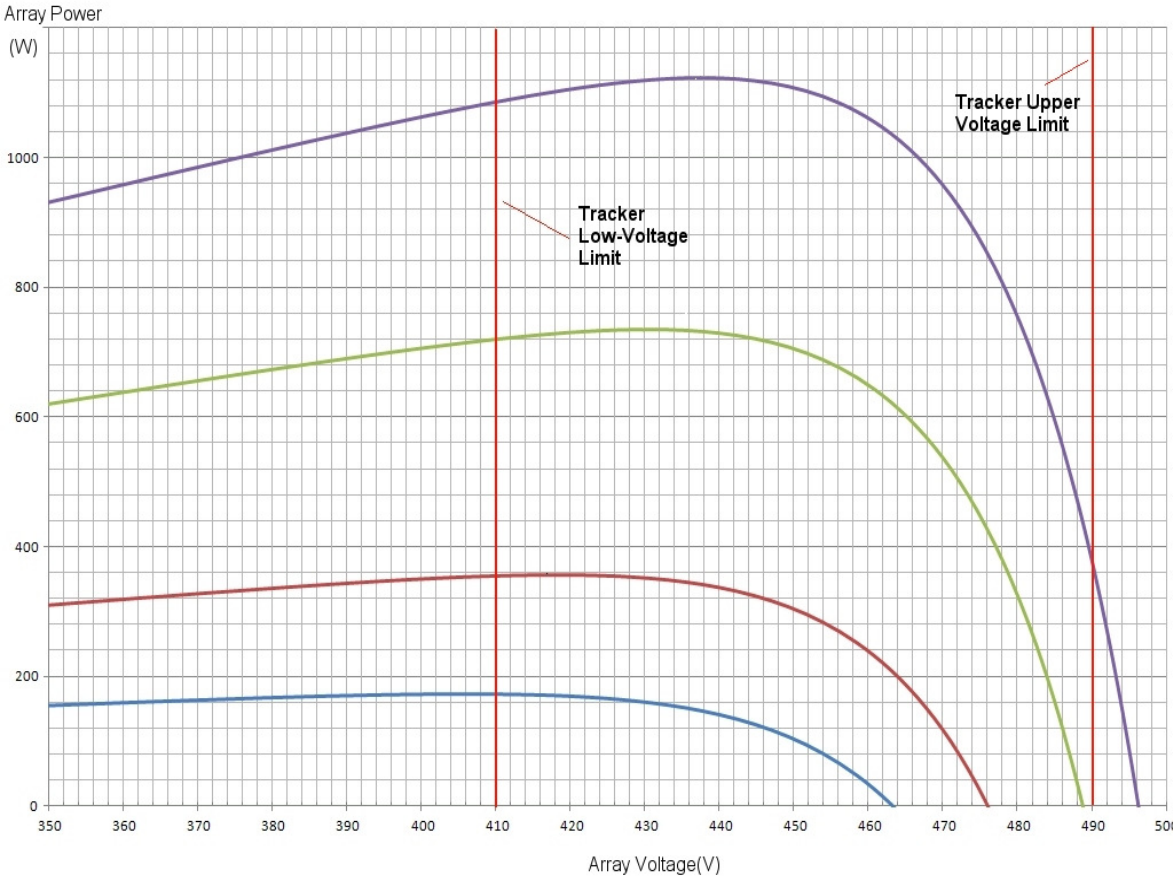


Figure 5.2: PV Array Power versus Insolation Level Curves

The maximum power tracker routine is executed every 30 seconds and the execution time is typically less than a fraction of a second. This gives ample time for the voltage controller to respond to incremental changes imposed by the maximum power tracker. If the previous increment ΔV results in an increase of output power from the array and $k_c v_{ref}$ has not reached either the upper or lower voltage limit as shown in figure 5.2, then the maximum power tracker makes an increment in the same direction of ΔV. If that is not the case, then the increment is made in the opposite direction.

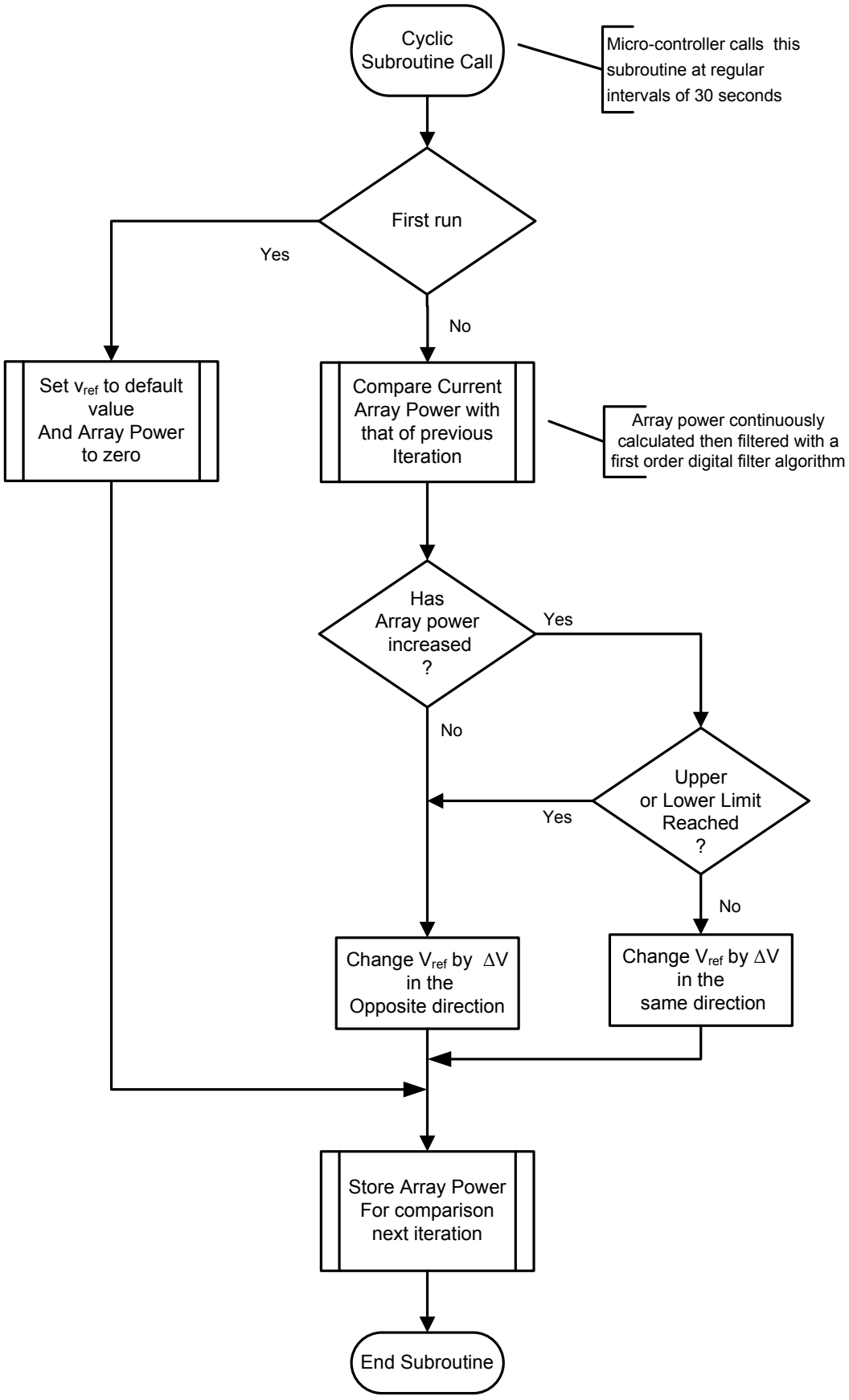


Figure 5.3: PV Array Maximum Power Tracker

5.3 DC Bus voltage Controller

A Simulink® model of the DC bus voltage controller is shown in figure 5.4. The model is based on the following equations:

$$\frac{1}{2}C\frac{dv_c^2}{dt} = P(v_c) - V_s I_{pr} \quad 5.1$$

$$\tau_m \frac{dv_c}{dt} + v_m = k_c v_c \quad 5.2$$

$$k_h I_{pr} = k_p\left(v_m - k_c V_{ref}\right) \quad 5.3$$

Equation 5.1 is based on the assumption that the inverter is 100 percent efficient. It states that the rate of change of energy stored in the DC bus bulk storage capacitor is equal to the difference between DC power output by the solar array and AC power injected into the mains. Inaccuracy due to twice mains frequency voltage ripple was found to be negligible.

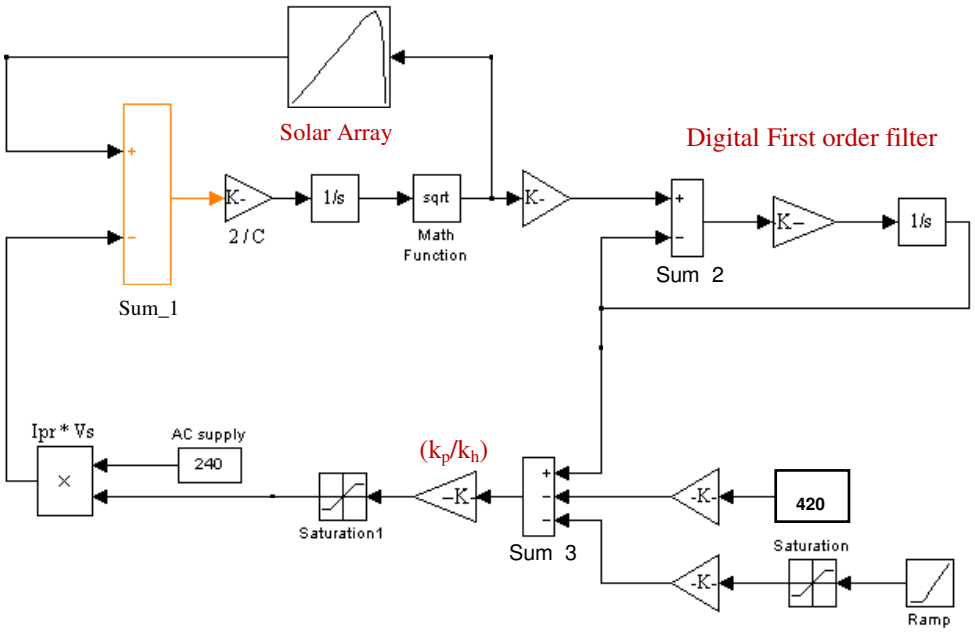


Figure 5.4: DC Bus Voltage Controller Simulink® model

In figure 5.4, equation 5.1 is represented by summer block 'sum_1', gain block '2/C', the 'solar array' block, a square root block and an integrator block. The 'solar array' block is a look-up table which provides the relationship between array power and array voltage for a given insolation level. In other words the 'solar array' block represents one of the curves in figure 5.2. Equation 5.2, which models a first order filter, is represented in figure 5.4 by summer block 'sum_2', a gain block and an integrator. The proportional controller is represented by gain block 'k_p/k_h'. The scaled down error voltage is determined by summer block 'sum_3'. The DC bus reference voltage is modelled in two parts, a constant part shown as '420' in figure 5.4 and a changing part represented by the ramp block and saturation block. These two blocks represent the increment or decrement (ΔV) imposed at the conclusion of every maximum power tracker cycle. Initially (ΔV) was implemented as a step change of approximately 4 volts. However step changes imposed by the maximum power tracker onto the DC bus voltage controller caused oscillations in the injected AC current which were considered unacceptable. The ramp and saturation block represents conversion of the required voltage step (ΔV) into a more gentle change with *dv/dt* selected as 10V/s. This means that incremental changes imposed by the maximum power tracker take 0.4s to fully take effect. For more rapid changes due to thick cloud then the massive drop in insolation level will cause the bus voltage to drop below limits which cause the controller to drop the current reference to zero and wait a preset time before trying to track the MPPT again.

The voltage controller was implemented digitally. Figure 5.5 represents a summary of the control algorithm.

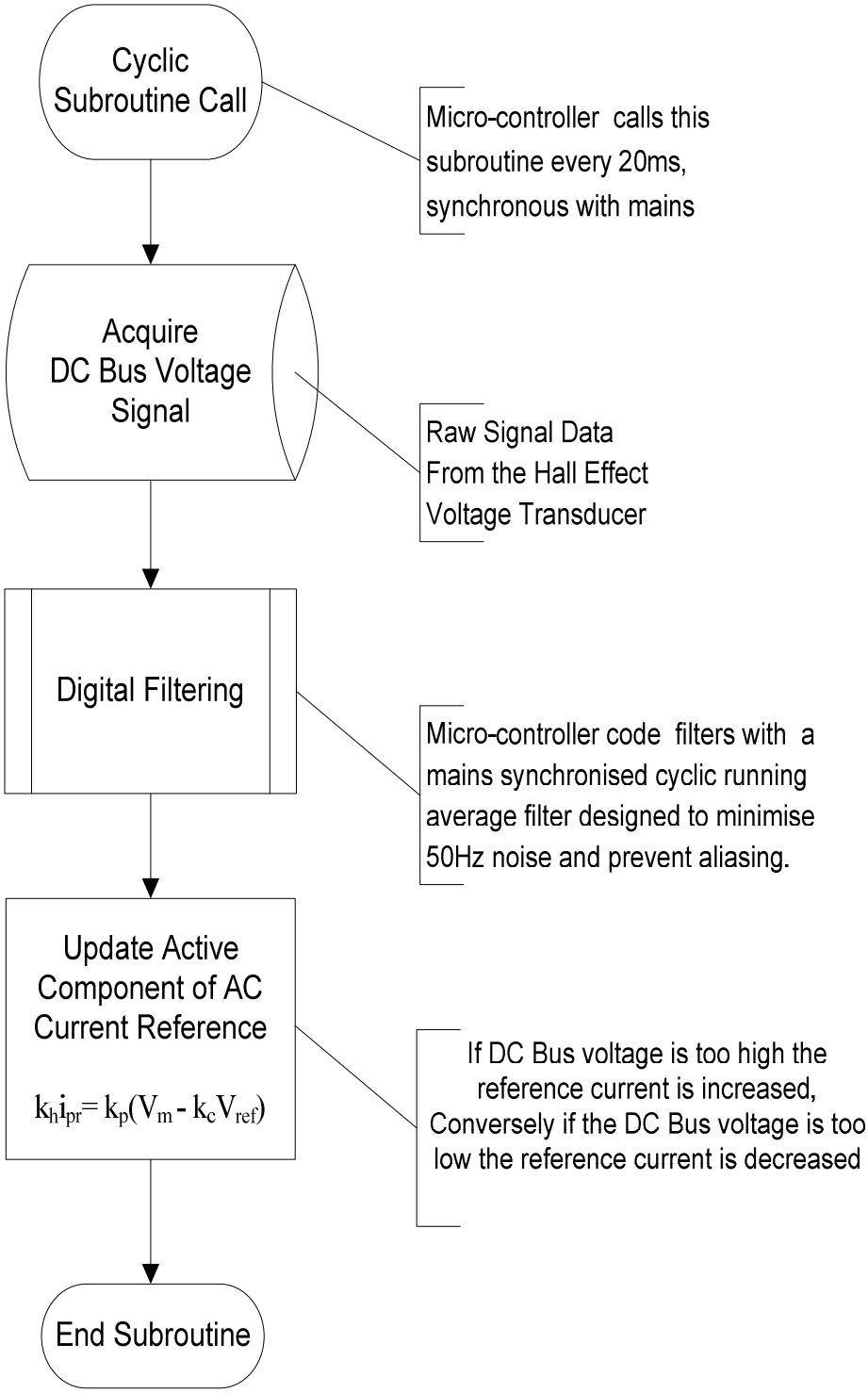


Figure 5.5: DC Bus Voltage Controller

5.4 Dynamic Analysis of the DC Bus Voltage Controller

Equation 5.3 is a non-linear differential equation. This makes the DC bus voltage controller a non-linear system. However, it is possible to carry out linear analysis of the system under small disturbance conditions. This is done by using equations 5.4, 5.5 and 5.6 which are linearised versions of equations 5.1 to 5.3 respectively.

$$CV_c \frac{d\Delta v_c}{dt} = \frac{dP}{dv_c}\Delta v_c - V_s \Delta I_{pr} \tag{5.4}$$

$$\tau_m \frac{d\Delta v_m}{dt} + \Delta v_m = k_c \Delta v_c \tag{5.5}$$

$$k_h \Delta I_{pr} = k_p \Delta v_f \tag{5.6}$$

Δv_c, ΔI_{pr} and Δv_m are small changes relative to the values of V_c, I_{pr} and V_m at a particular operating point. Equation 5.7, which is the system's characteristic equation, has been derived from equations 5.3 to 5.6.

$$\tau_f CV_c s^2 + \left(CV_c - \frac{dP}{dV_c}\ \tau_f\right) s\ + \left(k_c V_s \frac{k_p}{k_h} - \frac{dP}{dV_c}\right) = 0 \tag{5.7}$$

The term $\frac{dP}{dV_c}$ in equation 5.7 represents the possibility of the system going unstable. Referring to figure 5.2, it is clear that irrespective of insolation level, $\frac{dP}{dV_c}$ is negative on the high voltage side of the maximum power point but positive on the other side. There is no danger of instability if the operating voltage is high enough. However there may be occasions when, for a short time operation is on the side of the characteristic where $\frac{dP}{dV_c}$ is greater than zero. From equation 5.7 the following conditions guarantee the controller's stability:

$$k_c V_s \frac{k_p}{k_h} > \frac{dP}{dV_c} \quad 5.8$$

$$C\,V_c > \tau_m \frac{dP}{dV_c} \quad 5.9$$

It was found that for adequate speed of controller response and reasonable steady state error $k_c \frac{k_p}{k_h}$ had to be of the order of 0.5A/V. Therefore inequality 5.8 is easily satisfied since $k_c V_s \frac{k_p}{k_h}$ is equal to 120W/V compared to $\frac{dP}{dV_c}$ which from figure 5.2 is no greater than 4W/V. The value of the filter time constant (τ_f) used for the voltage controller was 0.032s. The DC bus bulk capacitance was 2mF. Equation 5.9 is also easily satisfied since CV_c, with V_c equal to 400V, is 0.8C whereas the maximum value of $\tau_m \frac{dP}{dV_c}$ is equal to 0.128C.

Figures 5.6 and 5.7 illustrate responses of the voltage controller as a result of incremental steps imposed by the maximum power tracker. In both cases the top curve in figure 5.2 is the assumed solar array characteristic. Figure 5.6 is for the case where the pre-disturbance reference voltage is 420V and the maximum power tracker wrongly decrements the reference voltage by 4V. As a result the array voltage drops from 429.9V to 425.7V with practically no oscillations. Similarly active current I_{pr} changes smoothly from 4.96A to 4.86A. In the case of figure 5.7 the pre-disturbance reference voltage is 480V which is higher than the maximum power point voltage. The maximum power tracker decrements the reference voltage by 4V. As illustrated the voltage controller responds smoothly. The bus voltage changes from 485V to 481.5V and the active current changes from 2.45A to 2.89A. Note that in both figures 5.6 and 5.7 that the DC bus voltage is slightly higher than the reference voltage. This is to be expected because the controller is purely proportional. A PI controller was trialled to eliminate this steady state error but led to instability beyond the crest of the array power curve.

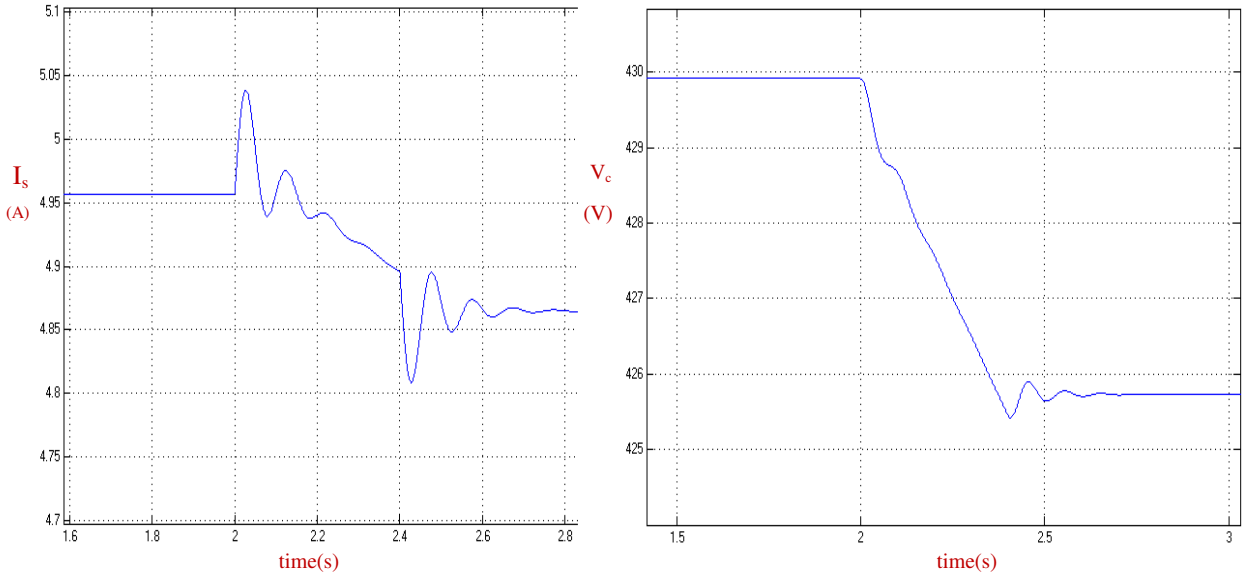


Figure 5.6: DC Bus Voltage Response from 420V to 416V Reference Step

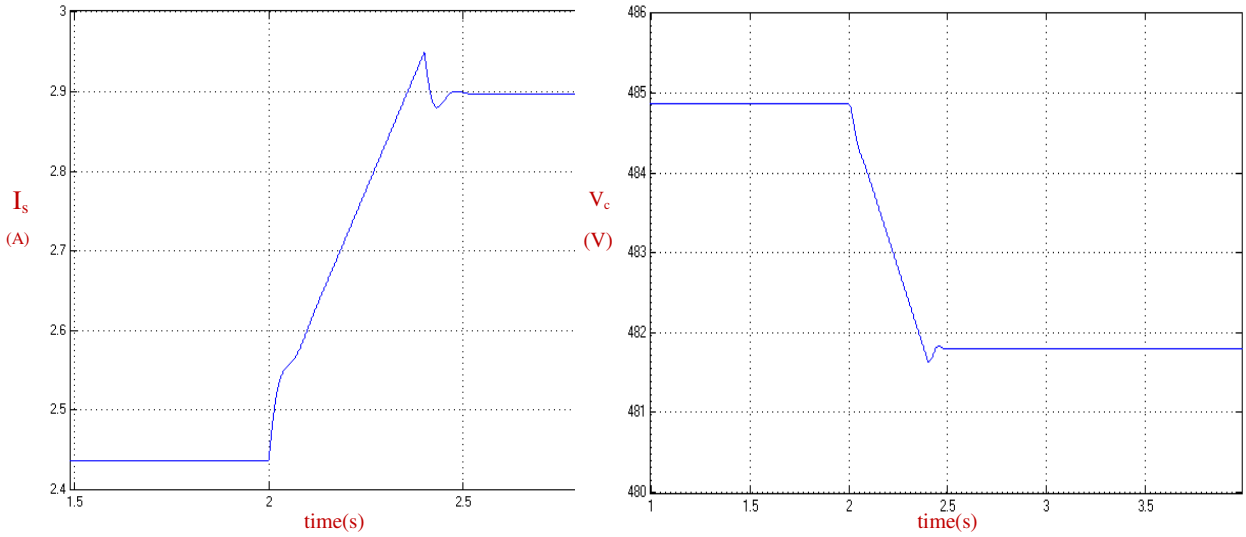


Figure 5.7: DC Bus Voltage Response from 480V to 476V Reference Step

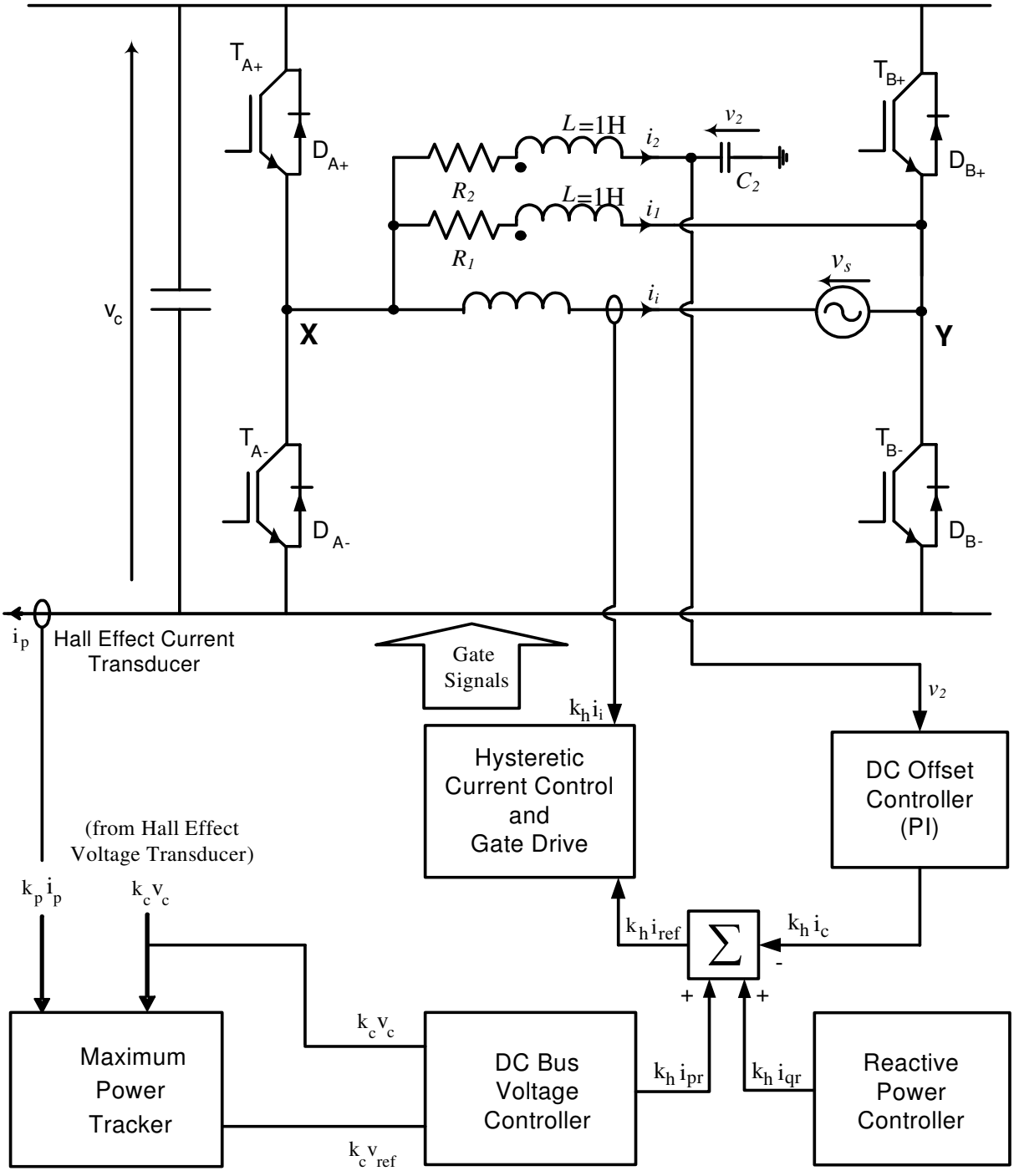
Chapter 6 DC Offset Control

6.1 Introduction

In a typical grid connected PV system DC power from the solar panels is converted to AC by an inverter before injection into the AC network. Ideally the output current of the inverter should be purely AC. But in practice it will contain a small amount of DC. Excessive DC injection into the AC network can result in problems such as corrosion in underground equipment [3], transformer saturation and transformer magnetizing current distortion [4], metering errors and malfunction of protective equipment [5]. For these reasons there are standards that impose limits on DC injection.

As mentioned previously in chapter 3, DC injection could be eliminated by using a power transformer as interface between the output of the inverter and the AC network. But this method has major disadvantages such as added cost, mass, volume and power losses. Alternative solutions to the DC injection problem have been proposed by [3, 10, 11]. Both reference [3] and reference [10] suggest the use of a feedback loop to eliminate the DC offset. In reference [6] a simple mathematical model is developed for the feedback system. It is assumed that the inverter is voltage controlled. No experimental results are reported. In reference [10] a current controlled inverter is considered. It reports some steady state performance test results. However it does not include any mathematical analysis and test results on dynamic performance are not reported. A detailed analysis of the method proposed in reference [10] is presented in section 6.2 of this chapter. Section 6.3 offers an alternative method based on a dual stage RC sensor. For ease of comparison, mathematical models are developed and practical results reported for both alternatives.

6.2 RLLC Based DC Offset Controller



L = winding inductance; M = mutual inductance = $k_m L$; C_2 = filter capacitance

$\tau_f = R_2 C_2$; $k_h i_c = k_e(-v_i + v_2)$; $v_i = \frac{-1}{\tau_i}\int_0^t v_2 dt + v_{i(0)}$; $i_{sr} = (i_{pr}^2 + i_{qr}^2)^{0.5}$

Figure 6.1: RLLC DC Offset Controller

The DC offset controller being considered is shown in figure 6.1 and it is based on the same concepts as those suggested in reference [10]. In particular the DC offset sensor being used is realised using a pair of mutually coupled inductors and an RC filter circuit. For this reason it has been called an RLLC DC offset sensor. The 1:1 mutually coupled inductor pair is bifilar wound to minimise leakage flux. The purpose of the mutually coupled inductor pair is to minimise the 50Hz voltage component in v_2. If R_1 and leakage flux were equal to zero then v_2 will ideally be proportional to the DC offset current and will not contain any 50Hz component. In practice R_1 and leakage flux are both finite and there will be some 50Hz component in v_2. It is important to minimise that component because it interferes with operation of both the DC offset controller and the inverter current controller. For example the 50Hz part of voltage v_2 may add a quadrature component to the reference current, which if it is large enough, will interfere with the power factor of the inverter.

As shown in figure 6.1, v_2 is the input to the DC offset PI controller whose output, $k_h i_c$, is added to the inverter reference current. The integrator element ensures that at steady-state $k_h i_c$ will assume a value which results in a zero DC offset current.

6.2.1 Mathematical Model

Symbols for currents and voltages are defined in figure 6.1. Upper case symbols used for currents and voltages represent their Laplace transforms. It has been assumed that the current controlled inverter is effectively a unity gain amplifier. In other words, ideally, its output current instantaneously follows the effective current reference (i_{ref}) which is equal to ($i_{sr} - i_c$). The voltage at the output terminals of the inverter has been approximated as, $v_s + (i_o - i_c)R$, where R is the resistance experienced by i_i as it flows from X to Y (figure 6.1).

Uncompensated DC Offset current i_o is due to circuit component imperfections. Current (i_o – i_c) is the offset component of current i_i.

The preceding assumptions and explanations lead to:

$$(sL + R_1)I_1 + sM\,I_2 + I_c R = V_s + I_o R \qquad 6.1$$

$$sM\,I_1 + (sL + R_2)\,I_2 + I_c R + V_2 = V_s + I_o R \qquad 6.2$$

since $k_h I_c = - k_e v_i + k_e V_2$

equations (6.2) and (6.3) respectively become:

$$(sL + R_1)I_1 + sM\,I_2 + kV_2 - kV_i = V_s + I_o R \qquad 6.3$$

$$sM\,I_1 + (sL + R_2)\,I_2 + (k+1)V_2 - kV_i = V_s + I_o R \qquad 6.4$$

where $K = Rk_e / k_h$

$$\begin{pmatrix} sL+R_1 & sM & K & -K \\ sM & sL+R_2 & K+1 & -K \\ 0 & -1 & sC_2 & 0 \\ 0 & 0 & 1 & s\tau_i \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ V_2 \\ V_i \end{pmatrix} = \begin{pmatrix} V_s + I_0 R \\ V_s + I_0 R \\ 0 \\ \tau_i v_i(0) \end{pmatrix} \qquad 6.5$$

Equation (6.5) is a mathematical representation of the DC offset control system. Equations (6.3) and (6.4) are expressed as the first two rows of matrix equation (6.5). The third row is the relationship between the voltage and current of capacitor C_2. The last row expresses the relationship between v_i, the integral component of the PI controller output, and v_2, which is the input to the integrator.

With the DC offset controller operating, a compensating current i_c is generated which, at steady state, ideally cancels i_o. The model represented by equation (6.1) can be used for both dynamic and steady state analysis. The two steady state issues that are most relevant are the steady-state behaviour of (i_o-i_c) and the 50Hz component in v_2. Because of the integral action of the PI controller, it can be deduced that if at steady state current i_o is constant or slowly changing then (i_o-i_c) will be zero. The 50Hz component in v_2 gives rise to a 50Hz component in $k_h i_c$ which must be minimised because of its adverse effect on the operation of the controller and the inverter.

Equation (6.6) is a transfer function that has been derived from equation (6.5) and it can be used to evaluate the 50Hz component of $k_h I_c$.

$$k_h I_c = \frac{k_e[\ \tau_p \tau_i (1 - k_m)s^2 + \tau_i s + \tau_p (1 - k_m)s + 1]V_s}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0} \qquad 6.6$$

where $k_h i_c = k_e(-v_i + v_2)$

$s = j\omega = j100\pi$ rad/s

$b_0 = k_e R / k_h = K$

$b_1 = \tau_p(1 - k_m)K + \tau_i(K + 1)$

$b_2 = \tau_i \tau_p (1 - k_m)K + \tau_i \tau_p + \tau_i \tau_f$

$b_3 = \tau_p \tau_f \tau_i (1 + R_1 / R_2)$

$b_4 = \tau_i \tau_f \tau_p^2 (1 - k_m^2) R_1 / R_2$

and V_s = rms value of AC supply voltage.

Aspects of dynamic performance that are of prime interest are stability and turn-on transients. At turn-on all control and gate drive circuits are energised and allowed to stabilise before inverter operation is enabled. This means that unless special measures are

implemented, when the inverter starts to operate the output of the PI controller is not necessarily zero. In the worst case the PI controller output could be at its designed saturation limit. This means that turn on transients can be partly due to the initial integrator capacitor voltage $v_i(0)$. Equation (6.7) is a transfer function that has been derived from equation (6.5) and it allows the effect of $v_i(0)$ on the transient response of the compensating current to be determined.

$$k_h I_c = \frac{(f_3 s^3 + f_2 s^2 + f_1 s^1 + 1)\tau_i k_e v_i(0)}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0} \qquad 6.7$$

where: $f_1 = \tau_p + \tau_f$

$$f_2 = \tau_p \tau_f (R_1 / R_2 + 1)$$

$$f_3 = \tau_f \tau_p^2 (1 - k_m^2) R_1 / R_2$$

Current i_o will also cause a transient component in the compensating current i_c. Equation (6.8) allows this transient component to be determined.

$$k_h I_c = \frac{[\tau_i \tau_p (1 - k_m) s^2 + \tau_i s + \tau_p (1 - k_m) s + 1] k_e R I_o}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0} \qquad 6.8$$

Stability assessment can be carried out by applying the Hurwitz criterion to the system's characteristic equation which is the denominator of equation (6.7) or (6.8). Since k_m is very close to 1, the system can be reduced to third order. Also as will be shown in the next section R_1/R_2 is much smaller than 1. Therefore the following must be satisfied in order to guarantee stability.

$$\tau_i > \frac{\tau_f \tau_p K}{(\tau_f + \tau_p)(K + 1)} \qquad 6.9$$

6.2.2 Controller Design

The mathematical model presented in section 6.2.1 was used to help with the design and evaluation of a DC offset controller based on the proposed RLLC DC offset sensor. For maximum effectiveness of the mutually coupled inductor pair, k_m must be close to 1 and τ_p must be large. Bifilar winding of the inductor pair maximises k_m. Larger values of τ_p can be achieved by using a core with large cross-sectional area and copper winding window area. If k_m is close to 1 (> 0.97), loop gain k is small and $s = j100\pi$, it can be shown by using equation (6.6) that:

$$k_h I_c \approx \frac{-k_e V_s}{(100\pi)^2 \tau_p \tau_f} \qquad 6.10$$

The following were the design steps:

(a) An available core, with cross-sectional area 50mmx30mm was used for the mutually coupled inductor pair. The core window was filled with two identical windings. The number of turns was chosen such that each can support voltage v_s without saturating the core. A value of about 0.5 second was achieved for τ_p. The winding resistance was approximately 2.0 Ω.

(b) Equation (6.10) was used to deduce τ_f. The PI controller gain k_e was chosen to be 0.5. Supply voltage V_s was taken to be 240V and a value of 10mV was used for $k_h i_c$. This was considered reasonable since, given that the Hall Effect sensor constant k_h was equal to 1.25V/A, the 10mV contributes to an equivalent of 8mA of 50Hz to the inverter current controller reference. This has negligible effect on the current controller because it is designed to operate at much higher currents. Also the phase shift between the 10mV signal and voltage v_s is almost 180 degrees which means that the inverter power factor is unaffected. Based on the above considerations equation

(6.10) returned a value of 0.22 seconds for τ_f . A 220kΩ resistor(R_2) and two 0.47uF capacitors(C_2) were used for practical realization.

(c) To ensure sufficient damping, it was decided to make τ_i equal to twice the value which results in marginal stability of the system as defined by inequality 6.9. To come up with the desired value of τ_i, an estimate of resistance R was required. Resistance R consists of two series connected parts. One part is external to the AC network and is essentially the resistance of the current ripple filter inductor shown in figure 6.1. The other part is the Thevenin resistance looking back into the AC supply terminals. A value for the first part of R is easily determined. It is not easy to determine a value for the second part. However, a reasonable upper limit for that part may be arrived at from knowledge of the AC supply characteristics such as supply capacity, voltage regulation, X/R ratio and fault level. According to inequality 6.9, the use of an upper limit for R leads to higher values for τ_i. This is a conservative approach because a higher value of τ_i implies a more stable system. Based on the above considerations a value of 0.12 seconds was arrived at for τ_i.

(d) There is some flexibility in the choice of the PI controller proportional gain k_e However for the same sensor performance (governed by equation (6.10)) and the same dynamic performance, lower values of k_e results in lower values of τ_i and τ_f which means smaller capacitors are needed for practical implementation. An excessively low value of k_e may lead to implementation problems for the PI controller. A value of 0.5 was considered to be a reasonable compromise. The analogue circuit used for implementation of the PI controller was based on a design described in Frohr [44]. Details are given in appendix A.10.

6.2.3 Test Results

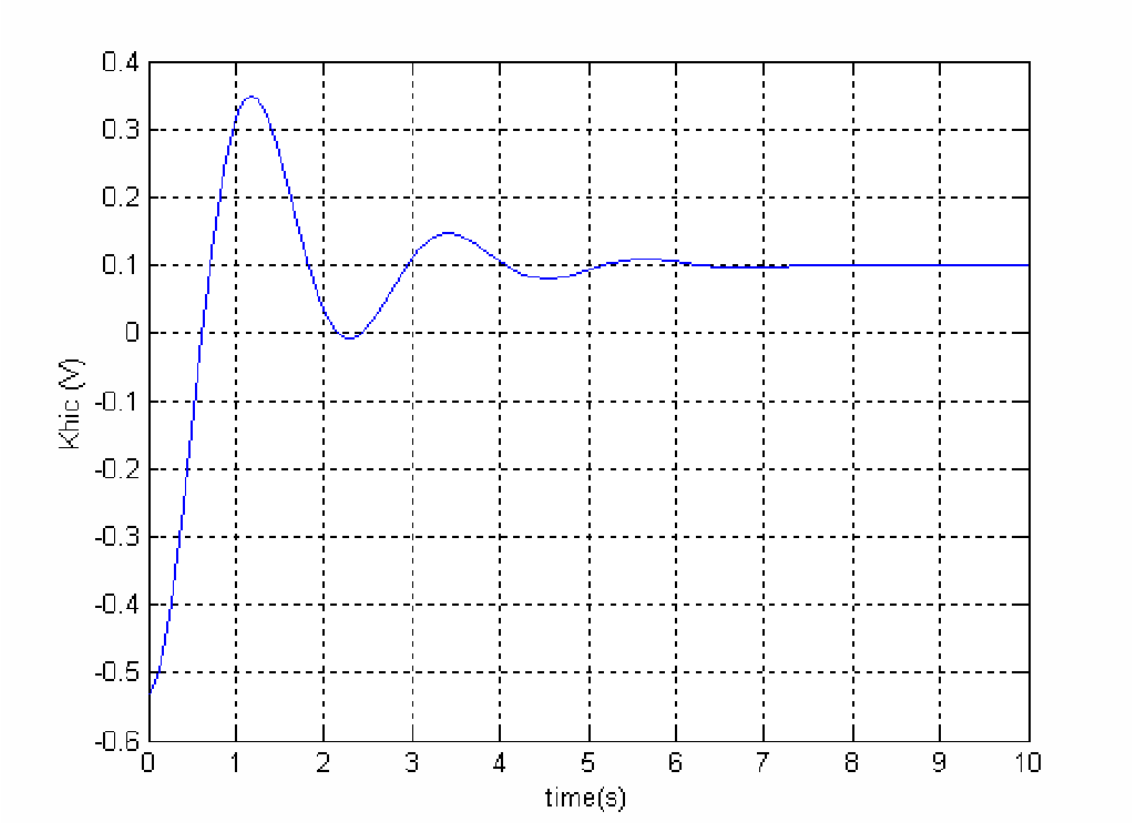


Figure 6.2: Measured Compensating Current Signal

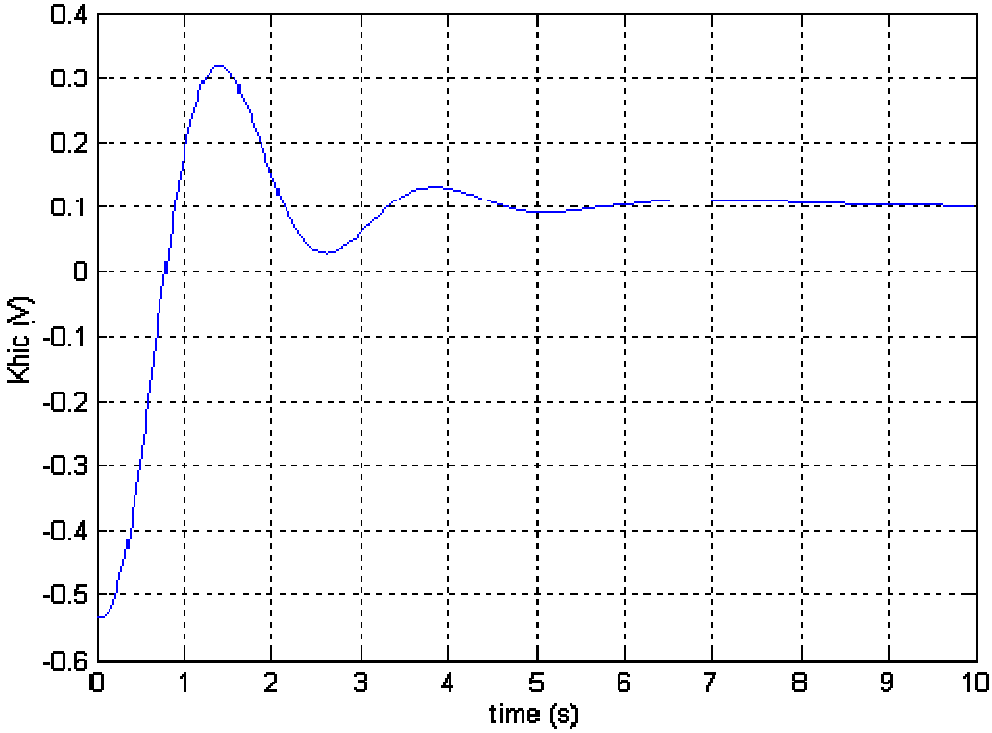


Figure 6.3: Predicted Compensating Current Signal

Without the DC offset controller and with I_i equal to 1A, the measured DC offset current was 30mA. With the DC offset controller in operation, the measured DC offset current was less than 2mA. In theory this should have been zero. The non-zero value is most likely due to integrator imperfections such as the integrator input offset range within which integration does not occur.

Figure 6.2 is a plot of the measured behaviour of the scaled compensating current $k_h i_c$ as result of inverter turn-on. Prior to the start of inverter operation the DC offset controller was operating, but effectively in open loop. Because of that, at the start of inverter operation, the PI controller's output was saturated at the chosen limit which was set to about 0.5V. This limit represents the maximum available DC offset compensating current. There is good agreement between the measured response of figure 6.2 and the theoretical response shown in figure 6.3 which is based on equations (6.7) and (6.8). The steady state value of the response is non-zero because a compensating signal is generated by the controller to cancel the DC offset observed on open loop. The settling time is of the order of 7 seconds. The fundamental reasons for this relatively slow response are the large values of τ_p and τ_f and the small value of loop gain K. The slow rate of response is not considered to be a serious problem because once the inverter is operating any disturbance that requires a response from the DC offset controller is unlikely to be fast changing.

Discussion of Results

The results presented in this section are considered to be very satisfactory since the DC offset controller manages to keep the DC offset well within the limits specified by Australian Standard AS 4777.2-2005[1]. A major problem with the RLLC sensor however is the size of the inductor core and the amount of copper needed by the two windings for effective filtering of the 50Hz signal. There is also significant additional power losses associated with a relatively large core. Design equations for inductors show that as core area and winding window area decrease the winding resistance increases much more rapidly than its inductance. For example, for the primary side of a 230V/24V transformer with package dimensions 20x20x15mm, τ_p was measured as approximately 5ms and winding resistance was 14kΩ. The mathematical model shows that with two such windings used as mutually coupled inductor pairs, the DC offset sensor would behave effectively as a first order filter with time constant R_2C_2. Due to the need for a large core and a significant amount of copper for the mutually coupled windings to be effective, the proposed RLLC DC offset sensor is not considered to be a practical solution to the problem of sensing the DC offset current injected by a grid-connected inverter into the AC network.

6.3 Dual-Stage RC Based Analog DC Offset Controller

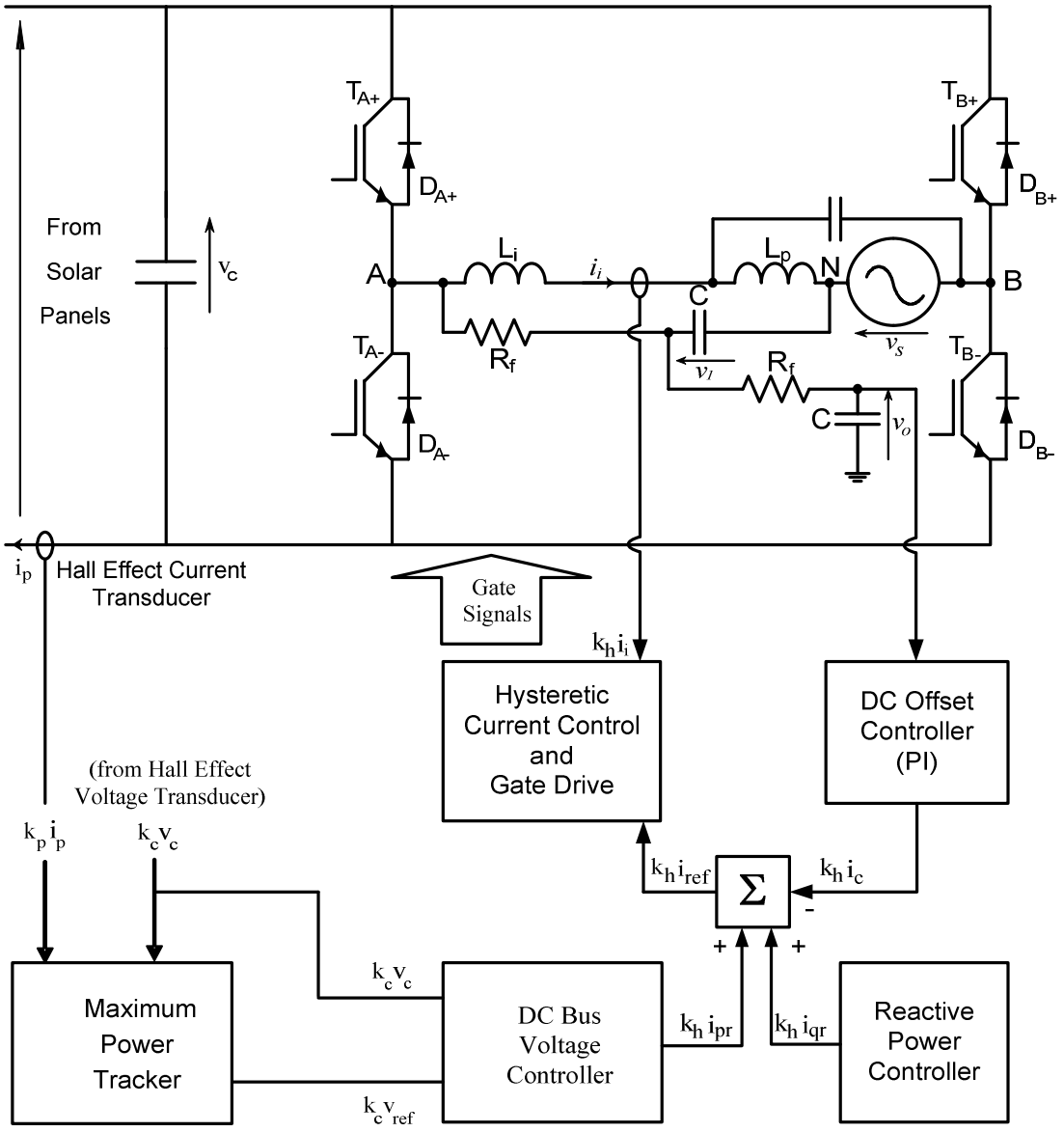


Figure 6.4: Dual-Stage RC Analogue DC Offset Controller

DC offset is monitored by sensing the voltage across the ripple filter inductors $(L_i + L_p)$ as shown in figure 6.4. The DC signal is extracted by using simple two-stage RC filtering. An analogue PI controller sends correction signal $k_h i_c$ to the summer circuit. Ideally this entirely eliminates the DC offset although in practice a small DC offset remains, but this is well within the limits imposed by standards such as Australian Standard AS4777.2 or the United Kingdom's ER G83/1-1.

6.3.1 Mathematical Model

Refer to figure 6.5 which is a block diagram representation of the DC offset sensor. The input to the DC offset sensor (v_f) is the voltage across the ripple filter inductors. This voltage is assumed to be made up of two components. There is a fast changing component labelled as v_L and a slow changing component equal to $(i_o\text{-}i_c)R$. The fast changing component would essentially be a mains frequency sinusoidal signal equal to $L\omega i_s$.

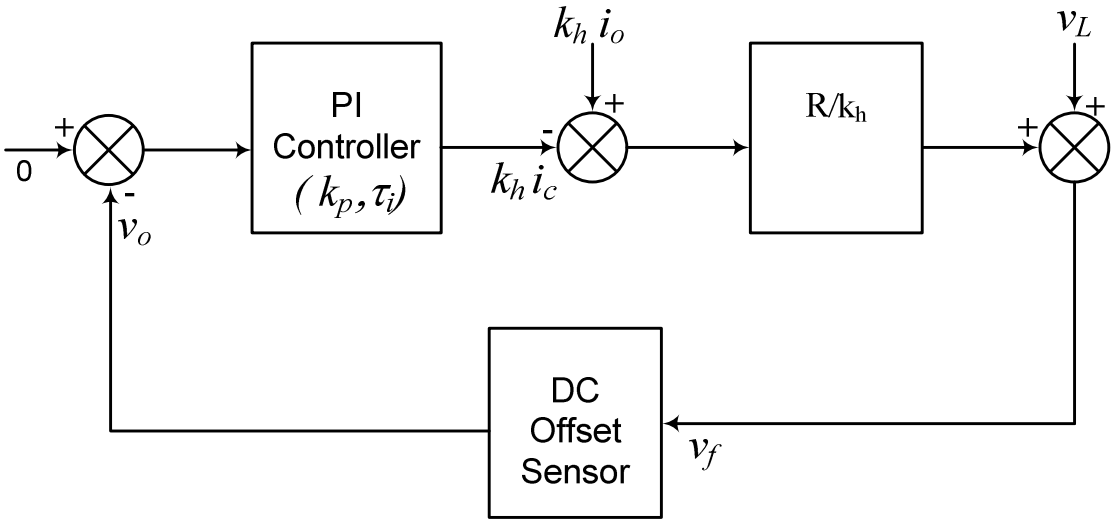


Figure 6.5: DC Offset Sensor Block Diagram

One part of the slow changing component is due to an unwanted DC offset current i_o which may be present because of circuit imperfections. The other part is due to the compensating current i_c which is proportional to the output signal from the DC offset control loop. The reasonable assumption made in figure 6.5 is that the slow changing component of inverter current contributes only a resistive voltage to the input of the DC offset sensor. Similarly it is assumed that the fast changing component of the inverter current contributes only an inductive voltage to the input of the DC offset sensor. If i_o is constant at steady state, the PI controller makes i_c equal to i_o thus ensuring the inverter output current is free of DC.

Referring to figures 6.4 and 6.5, for the second stage of the two-stage RC filter we have:

$$\tau_f \frac{dv_0}{dt} + v_0 = v_1 \qquad 6.11$$

where $\tau_f = R_f C$

Since node *N* in figure 6.4 is the neutral and a MEN (multiple earthed neutral) is assumed, the current input into the first stage of the two-stage RC filter is given by:

$$\frac{v_f - v_1}{R_f} = C\frac{dv_0}{dt} + C\frac{dv_1}{dt} \qquad 6.12$$

which may be written as:

$$\tau_f \frac{dv_0}{dt} + \tau_f \frac{dv_1}{dt} + v_1 = v_f \qquad 6.13$$

In figure 6.5, voltage v_o is the input to the PI controller. The relationship between v_o and the output of the integral element is given by:

$$-\tau_i \frac{dv_i}{dt} + k_p v_o = 0 \qquad 6.14$$

where τ_i = PI controller integration time constant and k_p = proportional gain

The output of the PI controller ($k_h i_c$) is given by:

$$k_h i_c = k_p v_o + v_i \qquad 6.15$$

From figure 6.5:

$$v_f = v_L + (i_o - i_c)R \qquad 6.16$$

Combining equations (6.11 to 6.16) and taking the Laplace transform results in equation (6.17).

The constant k in equation (6.17) is equal to $R\,k_p / k_h$.

$$\begin{pmatrix} s\tau_f + 1 & s\tau_f + k & k/k_p \\ -1 & s\tau_f + 1 & 0 \\ 0 & k_p & s\tau_i \end{pmatrix} \begin{pmatrix} V_1 \\ V_0 \\ V_i \end{pmatrix} = \begin{pmatrix} V_L + I_0 R \\ 0 \\ \tau_i v_i(0) \end{pmatrix} \qquad 6.17$$

In arriving at equation (6.17) coupling between the DC offset control loop and the other three control loops have been ignored. This assumption of negligible coupling is justified in section 6.5 with theoretical and experimental results.

The innermost loop of the inverter control system is the hysteretic current controller. As mentioned before, to the other loops the current control loop effectively appears as an amplifier with a pure gain. But the value of this gain is dependent on the magnitude of the mains voltage. Changes in the mains voltage magnitude may be regarded as disturbances in the current control loop. Slow changes in the AC voltage magnitude results in modulation of the mains frequency input signal v_L to the DC offset controller and has no effect on it. The value of the mains voltage magnitude may change suddenly by a few percent as a result of planned or unplanned disturbances on the AC network. The effect of such changes on the DC offset sensor may be assessed by treating these as mains frequency signals that appear suddenly as a disturbance and that are represented by v_L as shown in figure 6.5.

6.3.2 Controller Design

The designer of the DC-Offset sensor has to choose values for τ_f, τ_i and k_p to meet design specifications. It is assumed that the choice of values for R and k_h is based on criteria other than specifications for the DC-Offset controller. This is definitely true for the Hall Effect constant k_h which is chosen to maximize current sensor sensitivity. Resistance R could be just the inherent series resistance of the ripple filter inductors. However if it is found that the inherent resistance is too small for proper operation of the DC-Offset control loop, additional resistance may be added but at the expense of increased power losses.

The two main criteria specified for the DC-Offset controller were:

(a) A maximum value of the mains frequency component in its output signal.

(b) A sufficiently damped output response.

These two design criteria are now considered in detail.

Steady State Response

The first criterion is essentially about the steady state response of the controller output signal $k_h I_c$ to the mains frequency disturbance input v_L. Equation (6.18), derived from equations (6.15 and 6.17) by using Cramer's rule, is a transfer function describing the response.

$$k_h I_c = \frac{-k_p[\tau_i s + 1]V_L}{\tau_i \tau_f^2 s^3 + 3\,\tau_i \tau_f s^2 + (k+1)\tau_i s + k} \qquad 6.18$$

The steady state response is obtained from equation (6.18) by setting $s = j2\pi f$.

At 50Hz we have : $$k_h I_c \approx \frac{-k_p V_L}{(100\pi)^2 \tau_f^2} \qquad 6.19$$

Equation (6.19) was used to deduce τ_f. The PI controller gain k_p was chosen to be 0.4. The power frequency voltage across the filter inductor v_L was taken to be 25V, which corresponds to the inductors carrying rated inverter output current. A value of 10mV was used for $k_h I_c$. This was considered reasonable since, given that the Hall Effect sensor constant k_h is equal to 1.25V/A, the 10mV contributes an equivalent of only 8mA to the current controller reference. Based on the above, equation (6.19) returned a value of 0.10 seconds for τ_f.

Controller Stability

The output signal of the DC offset control loop, in general, is made up of a transient part and a steady state part. The steady state part is essentially made up of a mains frequency component as detailed above and a DC component equal and opposite to the unwanted DC offset current i_o as shown in figure 6.5. The transient part of controller's output is in response to sudden disturbances. These disturbances, as stated before, may be due to either planned or unplanned events. Examples of planned events that may result in sudden disturbances are system turn-on and switching operations in the AC network such as on-load tap changing giving rise to relatively sudden changes in the AC supply voltage. There are three disturbance input signals that appear explicitly in the proposed model as described by equation (6.17). These are integrator initial condition $v_i(o)$, unwanted DC offset i_o and sensor ac voltage input v_L. Each one of these may result in a transient response. Unless special measures are implemented at the instant of energisation of the inverter, the integral component of the DC offset PI controller may be non-zero. If that is the case there will be a transient component in the controller's output which is given by equation (6.20).

$$k_h I_c = \frac{-k[\tau_f^2 s^2 + 3\tau_f s + (k+1)]v_i(0)}{\tau_i \tau_f^2 s^3 + 3\,\tau_i \tau_f s^2 + (k+1)\tau_i s + k} \qquad 6.20$$

The proposed DC offset controller may be implemented digitally or by means of an analogue controller. If it is implemented digitally it is easy to ensure that $v_i(0)$ is equal to zero at the instant of inverter energisation.

Current i_o, if it is present at the instant of inverter energisation, will also cause a transient component in the compensating current i_c. Equation (6.21) allows this component to be determined.

$$k_h I_c = \frac{-k_p[\tau_i s + 1](R\frac{I_0}{s})}{\tau_i \tau_f^2 s^3 + 3\,\tau_i \tau_f s^2 + (k+1)\tau_i s + k} \qquad 6.21$$

The response to sudden changes, in v_L , as would occur if there was a change in supply voltage v_s , can be determined using:

$$k_h I_c = \frac{-k_p[\tau_i s + 1]V_L(s)}{\tau_i \tau_f^2 s^3 + 3\,\tau_i \tau_f s^2 + (k+1)\tau_i s + k} \qquad 6.22$$

A necessary condition for acceptable operation of the DC offset control loop is its stability. Stability assessment can be carried out by applying the Hurwitz criterion to the system's characteristic equation which is the denominator of equations (6.20), (6.21) and (6.22). Inequality (6.23) must be satisfied to guarantee stability.

$$\tau_i > \frac{\tau_f k}{3(k+1)} \qquad 6.23$$

To ensure sufficient damping, integration time τ_i must be sufficiently greater than the right hand side of inequality (6.23). Values of all the DC offset controller design parameters are given in Table 6.1. The table shows how those values relate to design equation (6.19) and inequality (6.23).

Table 6.1: DC Offset Controller Design Parameters

Design variable	Chosen value	Comments
Current Sensor constant (k_h)	**1.25 V/A**	• Determined by number of turns used with the Hall-Effect sensor. • Inadequate sensitivity if value too low • Maximum value limited by DC rail voltage
AC component in DC offset controller output signal ($k_h i_c$)	**10mV**	• Represents the undesirable 50Hz component in the output of the DC offset sensor. • Chosen limit dictates the value of the filter time constant τ_f given by equation 6.19. • If chosen limit is too small, τ_f becomes too large making the filter harder to implement
Filter resistance(R_f) and Filter capacitance(C)	**220kΩ** **0.47uF**	• $R_f C$ or τ_f is dictated by equation 6.19 • R_f cannot be made larger than a few hundred kΩ because of the effect of noise and stray impedances
Series resistance (R)	**0.38Ω**	• Can consist of just the inductors' resistance or additional series resistance may be added. • Choice of R dictated by efficiency considerations.
PI controller gain (k_p)	**0.4**	• For a given degree of stability, increasing k_p will mean increasing τ_i, making integrator implementation difficult • Too low a value of k_p leads to sluggish controller response.
PI controller Integration time (τ_i)	**100ms**	• For the chosen value of k, defined as $k_p R / k_h$, inequality (6.23) predicts a τ_i value of 23ms for marginal stability • A value of τ_i sufficiently higher than 23ms was chosen to ensure adequate damping.

6.3.3 Test Results

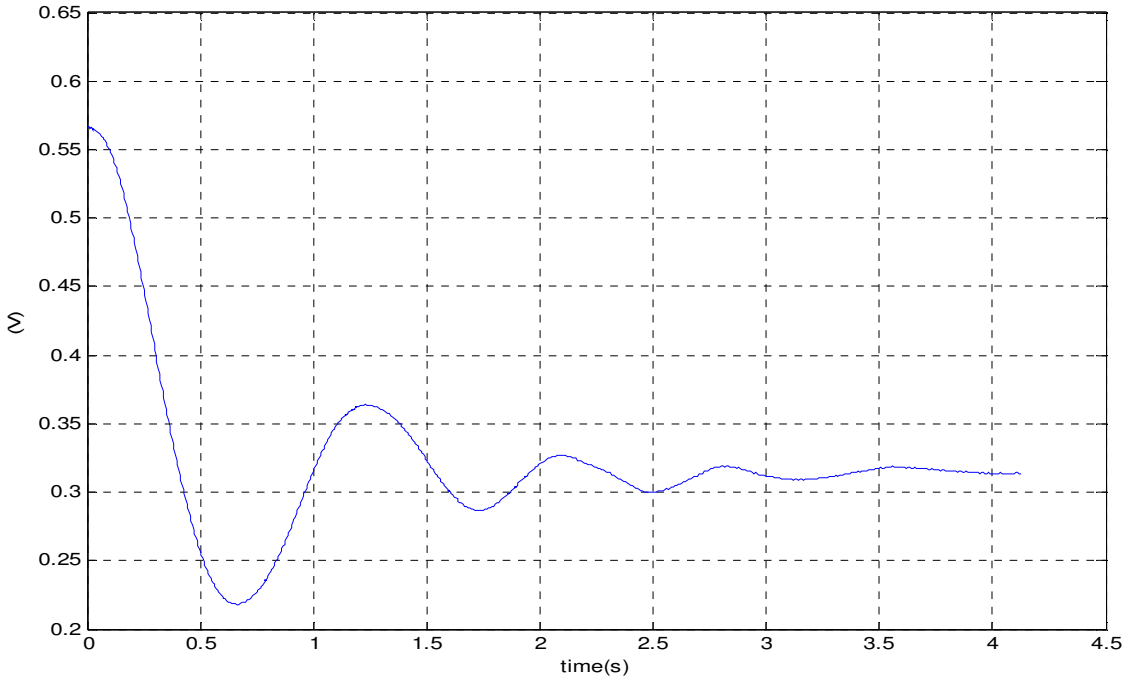


Figure 6.6: Measured Transient Response of PI Controller Output

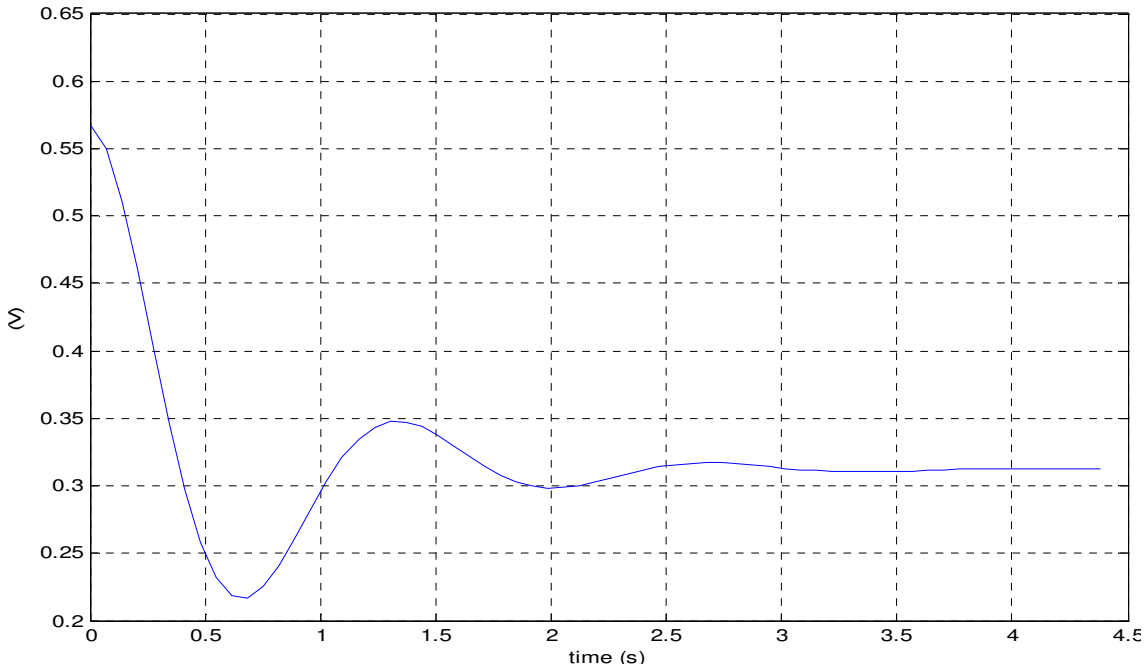


Figure 6.7: Simulated Transient Response of PI Controller Output

To verify the proposed design of the DC offset controller, the predictions of equations (6.20 and 6.21) and inequality (6.23) were compared with test results. Using the chosen value for τ_f of 0.1s and the estimated value of 0.07 for *k,* inequality (6.23) predicts marginal stability of the DC offset control loop when τ_i is equal to 23ms. With all controller

parameters held constant and τ_i varied, the measured value of τ_i at the onset of instability was found to be 20ms. A design value of 100ms was chosen to avoid instability. A higher value would improve stability but would result in sluggish responses.

Figure 6.6 shows a measured transient response. The inverter was first left to run with the DC offset controller not operating. This was done by grounding the output to the DC offset controller. The controller was then activated by removing the short. The transient response of the integrator capacitor consists of the voltage changing from its initial value to the steady-state value required for elimination of any DC offset. Prediction of the controller response, which was carried out using equations (6.20) and (6.21), is shown in figure 6.7. There is in reasonable agreement between the predicted response and the measured response shown in figure 6.6. Transients such as the one shown in figure 6.8 are easily avoided if a digital DC offset controller is used.

The analogue PI controller performs very satisfactorily and its component count and cost are very low. However, digital implementation of the controller has advantages such as ease of adjustment of controller parameters and better control of integrator initial conditions at inverter start-up.

6.4 Dual-Stage RC Based Digital DC Offset Controller

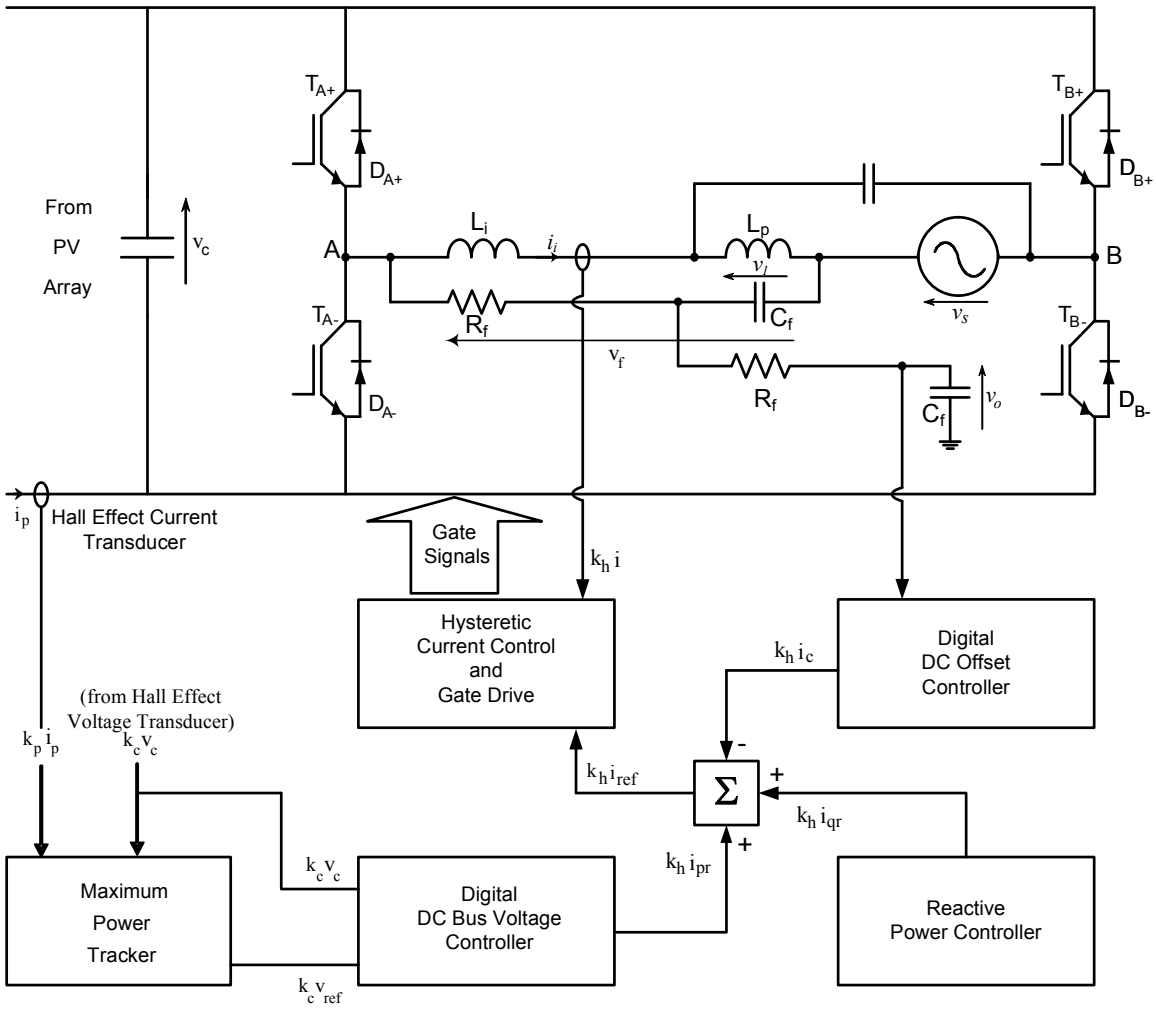


Figure 6.8: Dual-Stage RC Digital DC Offset Controller

A grid-connected photovoltaic system is shown in figure 6.8. It is essentially the same as figure 6.4 except for the digital implementation of the DC offset controller.

As in the analogue case (figure 6.5), the sinusoidal source v_L represents the 50Hz component of v_f which is the input to the two-stage RC-filter. The step input (I_o), when multiplied by R, is the component of input signal representing a sudden change in DC offset current injected by the inverter.

That is:

$$\tau \frac{dv_1}{dt} + v_1 + i_c R = v_L + i_o R \qquad 6.24$$

where $i_c R$ is the output of the digital controller.

Equation 6.25 relates to the second stage of the dual stage RC filter

$$\tau \frac{dv_o}{dt} + v_o - v_1 = 0 \qquad 6.25$$

The output signal from the dual stage RC filter was fed into the analogue to digital converter input of the digital controller. Filter time constant τ had to be high enough to make the 50Hz component of v_o low compared to its highest prospective DC value. A smaller 50Hz component allows better A to D converter resolution to be selected while lowering the risk of saturation. Measurements indicated that the digital controller was affected by operation of the inverter. For satisfactory operation, further low pass filtering was necessary within the digital controller. The digital filter is represented in the Simulink® model of figure 6.9 by the first order filter with time constant τ_d . In other words:

$$\tau_d \frac{dv_z}{dt} + v_z - v_o = 0 \qquad 6.26$$

To simplify the design process the last stage of the digital controller was chosen to be a piecewise constant rate integrator. The integration rate, $k_z v_z$, as shown in figure 6.9, was selected based on the following conditions:

$$200\text{mV/s} = k_{d2} \quad \text{if} \quad |v_z| > 20\text{mV} \qquad 6.27$$

$$5\text{mV/s} = k_{d1} \quad \text{if} \quad 0.5\text{mV} \leq |v_z| \leq 20\text{mV} \qquad 6.28$$

$$0\text{mV/s} \qquad \text{if} \qquad |v_z| < 0.5\text{mV} \tag{6.29}$$

The piecewise constant rate integrator may be modelled by the following equation:

$$k_h i_c = \int_0^t k_z v_z \, dt \quad or \quad k_z v_z = k_h \frac{di_c}{dt} \tag{6.30}$$

Note that equation 6.30 is a non-linear differential equation since, in accordance with inequalities 6.27, 6.28 and 6.29, k_z is a function of v_z. That is k_z =

$$k_{d2} / v_z \qquad \text{if} \qquad |v_z| > 20\text{mV} \tag{6.31}$$

$$k_{d1} / v_z \qquad \text{if} \quad 0.5\text{mV} \leq |v_z| \leq 20\text{mV} \tag{6.32}$$

$$0\text{mV/s} \qquad \text{if} \qquad |v_z| < 0.5\text{mV} \tag{6.33}$$

As will be discussed in the next section, the reason for using different rates of integration is to achieve quick responses while maintaining stability.

6.4.1 Mathematical Model

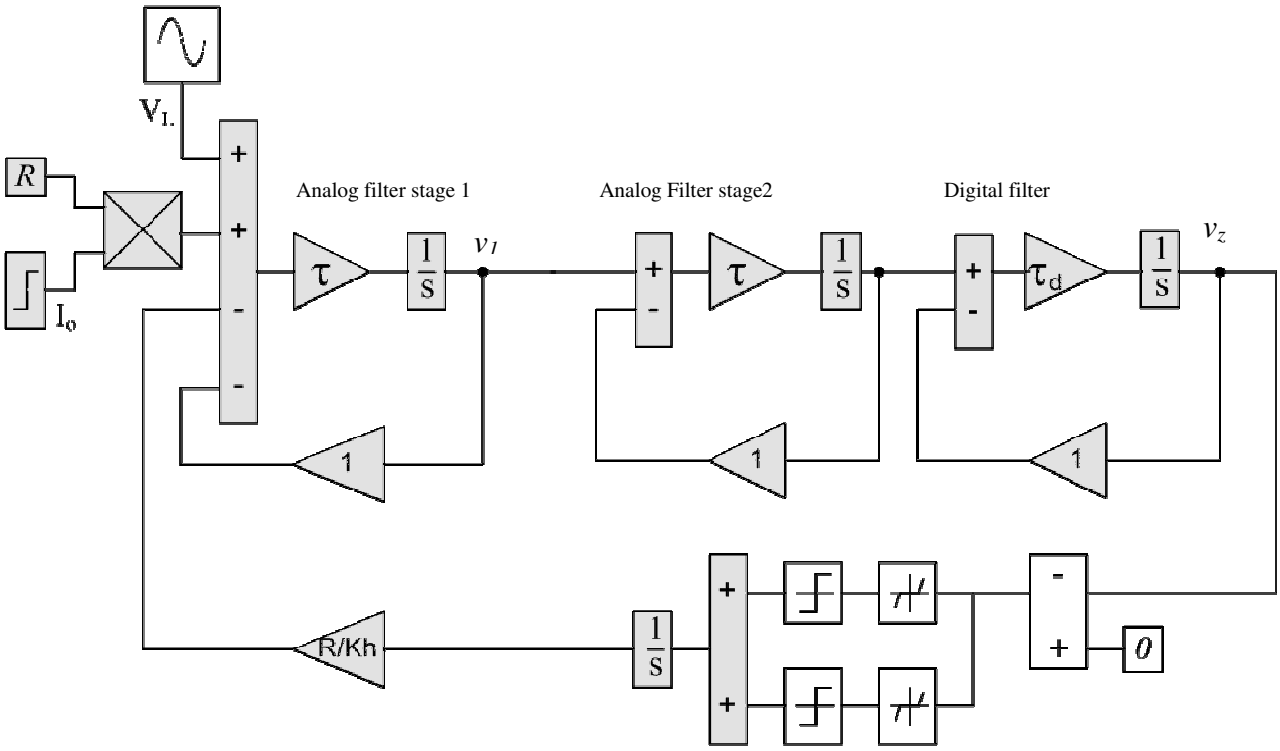


Figure 6.9: Digital DC Offset Controller Simulink Model

A Simulink® model of the DC offset controller, which was digitally implemented, is shown in figure 6.9. As the sampling rate used by the digital controller was approximately 200 times faster than the fastest loop discrete analysis is not required. Three stages of filtering of the sensed DC offset signal are shown. The additional stage of filtering with the digital system is to avoid aliasing. The controller is essentially a variable gain integral controller. A linearised model of the controller was derived. This led to the following characteristic equation:

$$\tau_d \tau^2 s^4 + (2\tau\tau_d + \tau^2)s^3 + (2\tau + \tau_d)s^2 + s + k = 0 \qquad 6.34$$

By analysing the equation it was found that stability of the DC offset controller is satisfactory only if the loop gain *k* falls within a certain range of values.

6.4.2 Controller Design

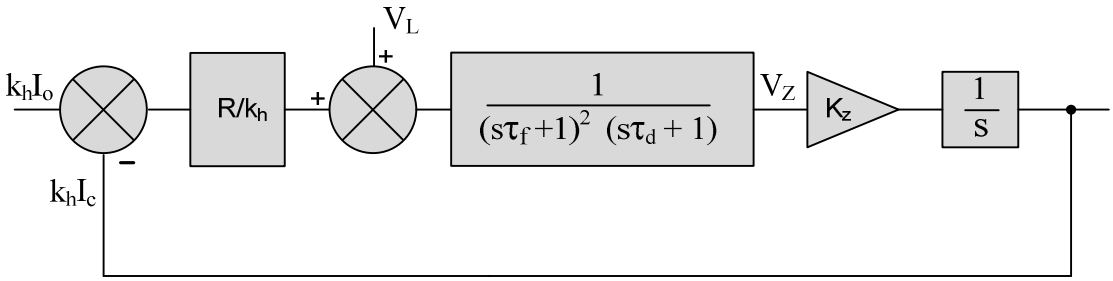


Figure 6.10: Controller Block Diagram

The above block diagram is based on equations 6.24, 6.25, 6.26 and 6.30. Filter time constant τ_f was chosen to ensure that the AC component in filter output voltage v_o was limited to 25mV. The filter time constant was calculated to be 0.1s and was implemented with a 220kΩ and 0.47uF capacitor. It was important to impose this limit so that most of the input range of A to D converter was made available for the DC offset, which, in the worst case, could be as high as 100mA. The A to D converter range chosen was +/-100mV. As mentioned before, in addition to filtering using the dual RC filter, a first order digital filter with a time constant equal to 0.25s was found to be necessary for satisfactory operation. Both the dual RC filter and the digital filter are represented as linear transfer functions in the block diagram of figure 6.10.

The integrator gain , k_z ,may be represented by a describing function N, Raven[44]. The describing function of a nonlinear element is equal to the phasor representing the fundamental component of the output divided by the phasor representing its input, which is assumed to be sinusoidal. In this case the describing function is given by:

$$N = 0 \quad \text{for} \quad 0 < V_z < 0.0005V$$

$$= \frac{4k_{d1}(1-(0.0005/V_z)^2)^{1/2}}{\pi V_z} \quad \text{for} \quad 0.0005V < V_z < 0.02V$$

$$= \frac{4k_{d2}(1-(0.02/V_z)^2)^{0.5}}{\pi V_z} - \frac{4k_{d1}(1-(0.0005/V_z)^2)^{0.5}}{\pi V_z} \quad \text{for} \quad V_z > 0.02V \qquad 6.35$$

In practice, as will be shown, k_{d1} is much smaller than k_{d2}. Therefore inequality 6.35 may be simplified to:

$$= \frac{4k_{d2}(1-(0.02/V_z)^2)^{0.5}}{\pi V_z} \qquad \text{for} \quad V_z > 0.02V \tag{6.36}$$

The block diagram of figure 6.10 leads to the following characteristic equation:

$$\tau_d\tau_f^2 s^4 + \left(2\tau_f\tau_d + \hat{0}_f^2\right)s^3 + \left(2\tau_f + \tau_d\right)s^2 + s + \frac{Rk_z}{k_h} \tag{6.37}$$

By replacing s by $j\omega$ and by equating imaginary parts to zero, a frequency of oscillation can be calculated. This is the limit cycle frequency achieved by the system if Rk_z/k_h is large enough for the system to be unstable. In this case:

Limit cycle frequency = ω_c

$$= \frac{1}{\left(2\tau_f\tau_d + \tau_f^2\right)^{0.5}} \tag{6.38}$$

By equating the real parts of equation 6.37 to zero, the critical value(k_c) of Rk_z/k_h can be evaluated. That is:

$$k_c = \left(2\tau_f + \tau_d\right)\omega_c^2 - \tau_d\tau_f^2\omega_c^4 \tag{6.39}$$

The choice of integration rates, that is k_{d1} and k_{d2}, determines how stable the system is. Expressions for critical values of integration rates (k_{dc}) can be derived by combination of equations 6.35 and 6.39. That is:

Rk_{dc}/k_h = *critical integration rate* * R/k_h

$$= \frac{\pi k_c V_z}{4(1-(0.0005/V_z)^2)^{1/2}} \qquad \text{for} \quad 0.0005 < V_z < 0.02$$

$$= \frac{\pi k_c V_z}{4(1-(0.02/V_z)^2)^{0.5}} \qquad \text{for} \quad V_z > 0.02 \tag{6.40}$$

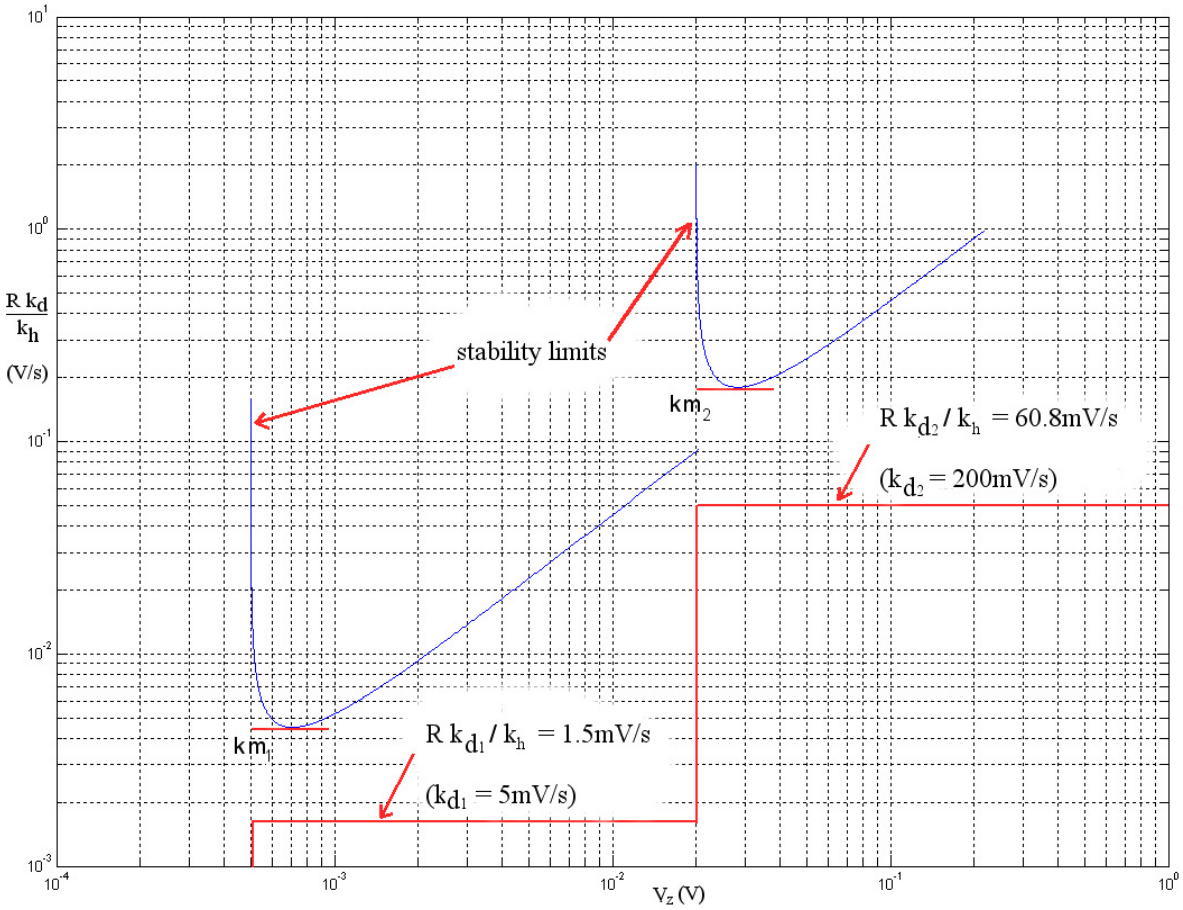


Figure 6.11: Integrator Gain Characteristic

Figure 6.11 is the graphical representation of equation 6.40. The graph can be used as a design tool for the DC offset controller. It brings out the following properties of the control system:

(a) Without the two dead-bands, the boundary between the stable and unstable regions will be a straight line of gradient $\pi k_c/4$ going through the origin. This means that the system will be unstable irrespective of the choice of integration rate.

(b) The choice of a relatively large dead-band, such as ±0.02V in the present case, allows stable operation with integration rates up to a maximum value labelled as k_{2m} in figure 6.11. Limit cycling occurs if an integration rate higher than k_{2m} is chosen. The frequency of the limit cycle is given by equation 6.38 and the amplitude is given by the intersection between the horizontal line representing the integration rate and the stability curve of figure 6.11.

(c) Whilst the choice of a relatively large dead-band allows fast responses without loss

of stability, control action is lost when the variable to be controlled is inside the dead-band. To solve this problem a second dead-band can be introduced. In the present case the size of the second dead-band is ±0.0005V.

(d) The width of the second dead-band should be small enough so that no control action is needed once the control variable settles within the band.

In the present case the design procedure was:

(1) Choose τ_f to ensure that less than 20mV of 50Hz appears at the input of the A to D converter.

(2) Choose τ_d so that the digital signal representing the DC offset is sufficiently filtered.

(3) Choose the size of the smaller dead-band so that it is well-within the allowable DC offset voltage limit. (This is the maximum allowable DC offset current limit times the circuit resistance R). In this case a dead-band of ±0.5mV was chosen. This corresponds to a current of ±0.2mA which is well within AS4777.2 specifications. A tighter dead-band could be chosen but this would be at the expense of longer response times.

(4) Choose the size of the larger dead-band. In this case the choice was 20mV.

(5) Based on values of τ_f, τ_d and the chosen size of the two dead-bands, produce a graph similar to figure 6.9. Use the graph to select integration rates k_{d1} and k_{d2}. These should be, respectively fractions of k_{m1} and k_{m2}. The closer k_{d1} and k_{d2} are to the critical values, the more oscillatory the system will become. To avoid oscillations k_{d1} was set to less than $0.5k_{m1}$ and similarly k_{d2} was set to less than $0.5k_{m2}$. Note that the values of k_{d1} and k_{d2} determine the response rate. If this is found to be too slow, the size of one or both dead-bands could be increased.

6.4.3 Test Results

Both the linearised model and the Simulink® model predict instability if the controller loop-gain is above a particular value, figure 6.12 confirms this prediction. Figure 6.12 shows the controller response to the removal of an artificially injected DC offset current. The artificial injection was implemented in software by initially forcing $k_h i_c$ to be such that the measured offset current was about 90mA, at time zero the artificial injection was suddenly removed. Figure 6.13 shows that a stable response results if the controller gain is low enough. Figures 6.14 and 6.15 are the corresponding simulation results.

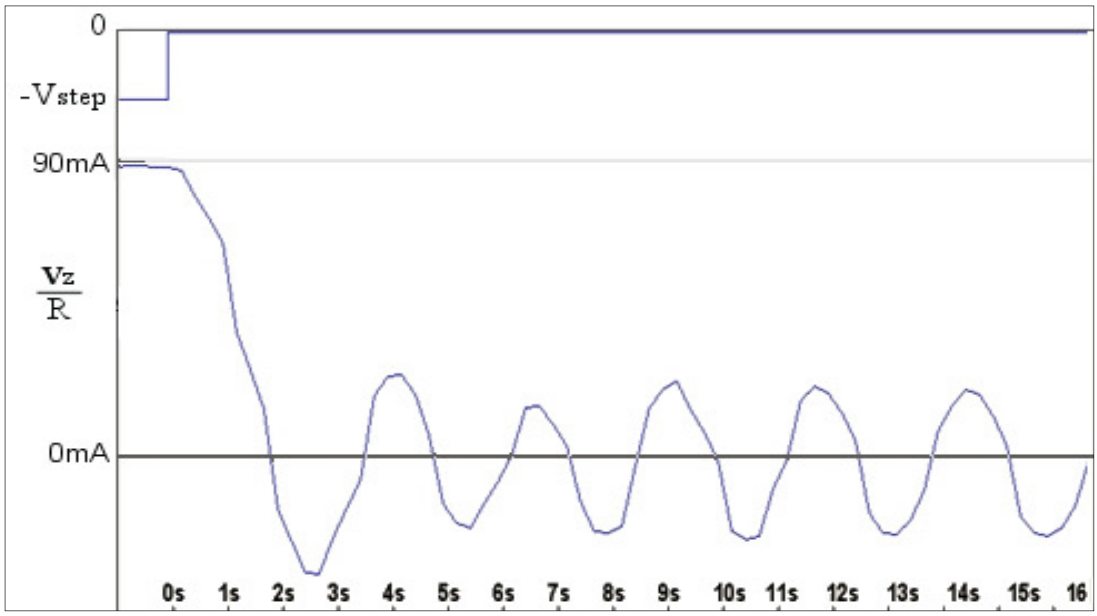


Figure 6.12: Measured DC Offset Controller Step Response (unstable)

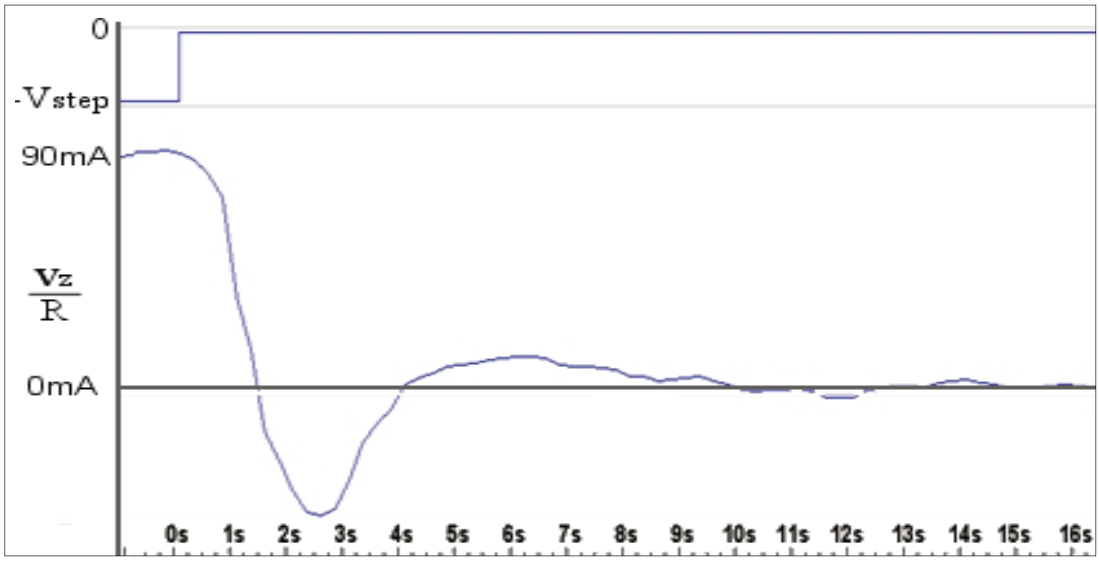


Figure 6.13: Measured DC Offset Controller Step Response (stable)

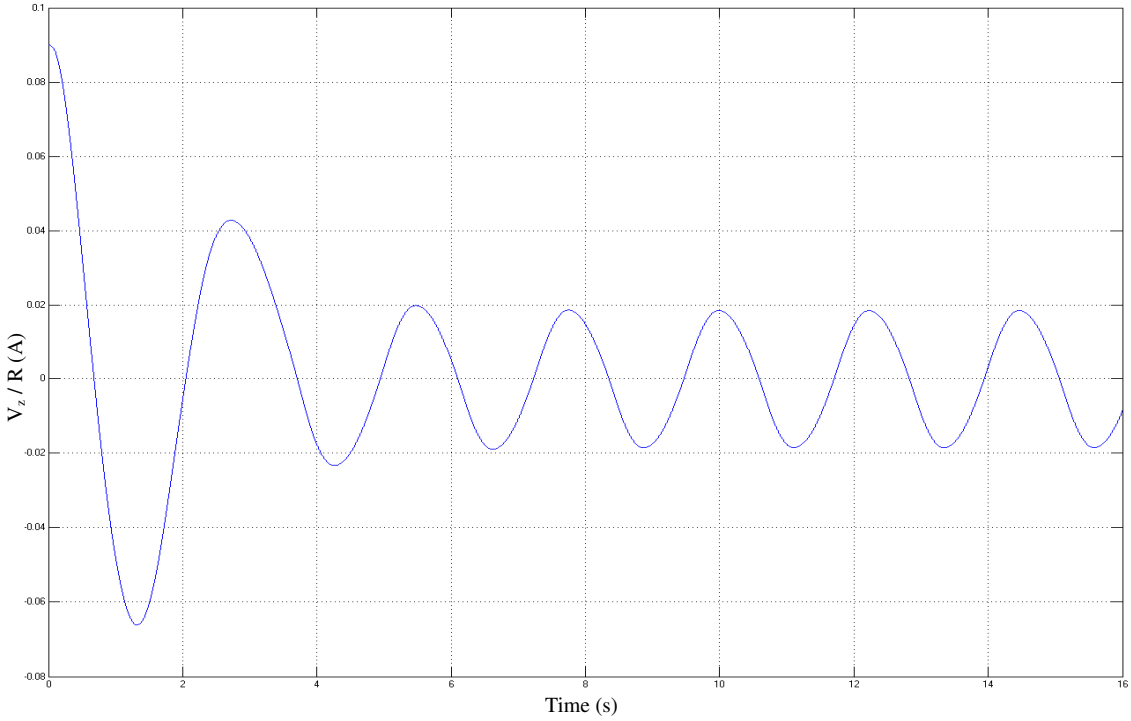


Figure 6.14: Simulated DC Offset Controller Step Response (unstable; k_{d1}=0.2V; k_{d2} =0.2V)

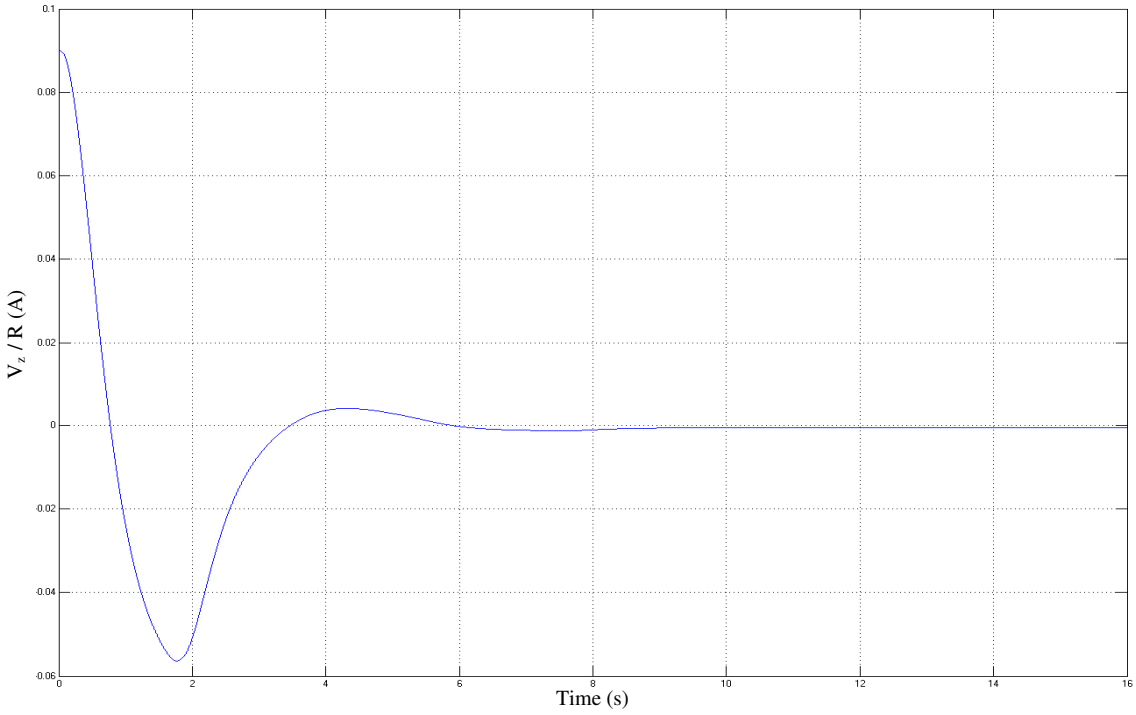


Figure 6.15: Simulated DC Offset Controller Step Response (stable; k_{d1}=0.2V; k_{d2} = 0.005V)

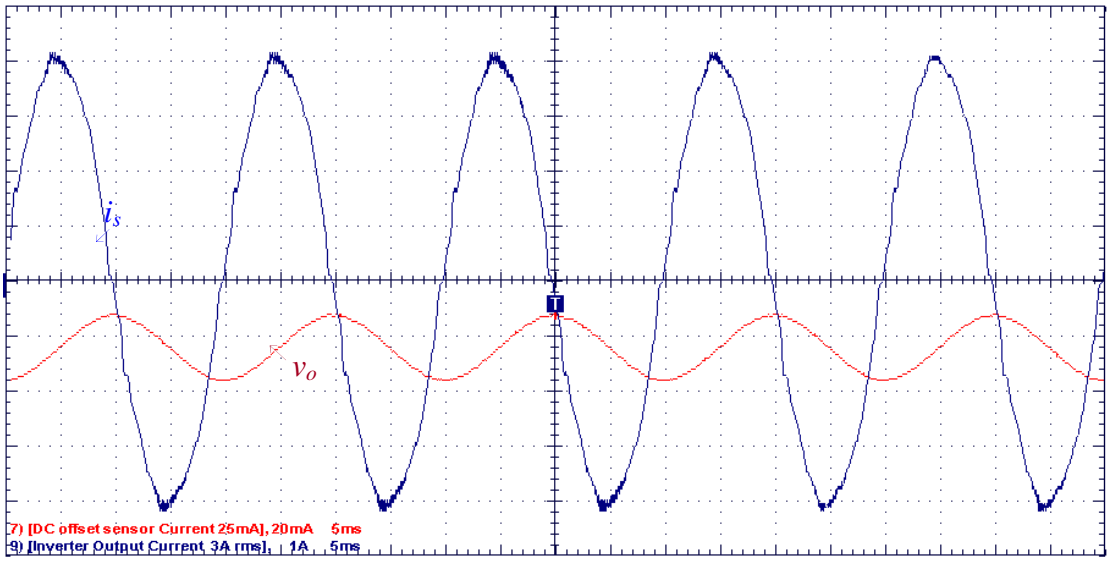


Figure 6.16: DC Offset Sensor output at 3A with 25mA DC Offset (DC offset controller disabled)

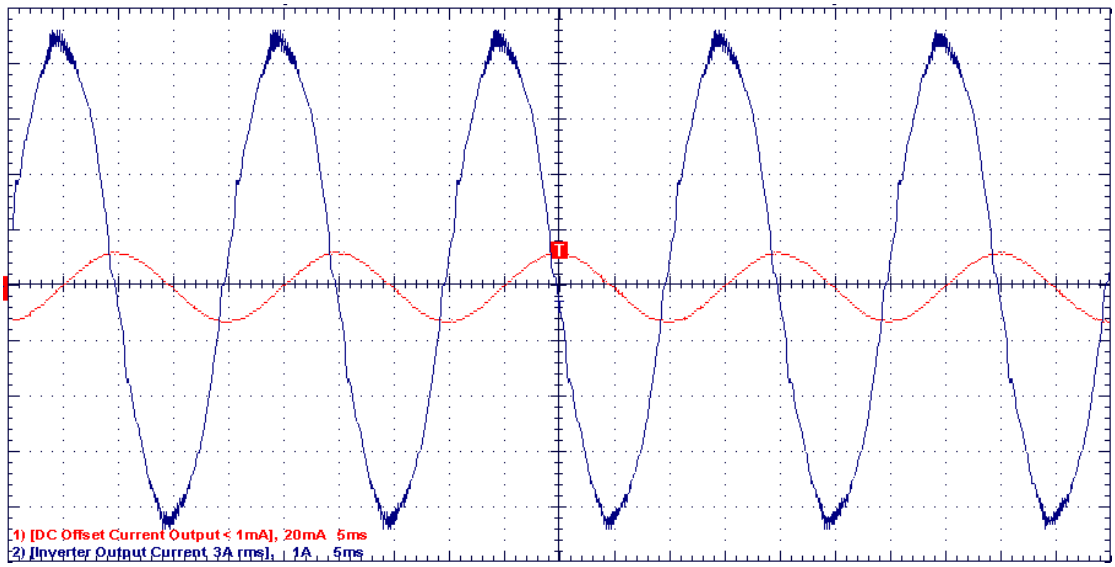


Figure 6.17: DC Offset Sensor output at 3A with <1mA DC Offset (DC offset controller active)

The experimental results of figures 6.16 and 6.17 show the output of the DC offset sensor with the control loop disabled (~25mA offset) and enabled(<1mA offset). DC offset measurements were carried out using a Fluke 87 multimeter on DC mA scale. The values from the multimeter agree well with the Wavestar® cyclic mean figures of 21mA(loop disabled) and 0.49mA(loop enabled). As mentioned before the high 50Hz ripple component present in the sensor waveform required additional filtering to be implemented in the digital control loop to avoid aliasing. The analogue PI controller system allowed this ripple to pass through to the current controller without disturbance to normal operation.

6.5 DC Offset and Bus Voltage Controller Interaction

The mathematical models of the DC offset controllers presented in this chapter ignore any possible interactions with other control loops in the system. It can be argued that there is very little interaction between the operation of the DC offset control loop and the DC bus voltage control loop. The fundamental reason behind this is that the DC bus voltage control loop is driven by the imbalance between DC power from the DC bus and AC power injected into the AC network and that the action of the DC offset controller has practically no effect on that power balance. That is except for resistive losses, there is no active power associated with the injection of a DC offset current into the AC network. Moreover, the resistive losses are, in practice, very small. The reduction or elimination of DC offset current in i_s will therefore only produce minor reactions from the DC bus voltage control loop which will result in negligible increases in reference current i_{ref}. The assumption of no interaction between the DC offset controller and the DC bus voltage control loop is therefore justified. Results are presented later in this section verifying that the above assumptions.

Any possibility of interaction between the DC offset controller and the maximum power tracker would be through the DC bus bulk storage capacitor voltage v_{dc}. But operation of the DC offset controller has no effect on v_{dc}. Therefore the assumption of no interaction between the DC offset controller and the maximum power tracker is justified.

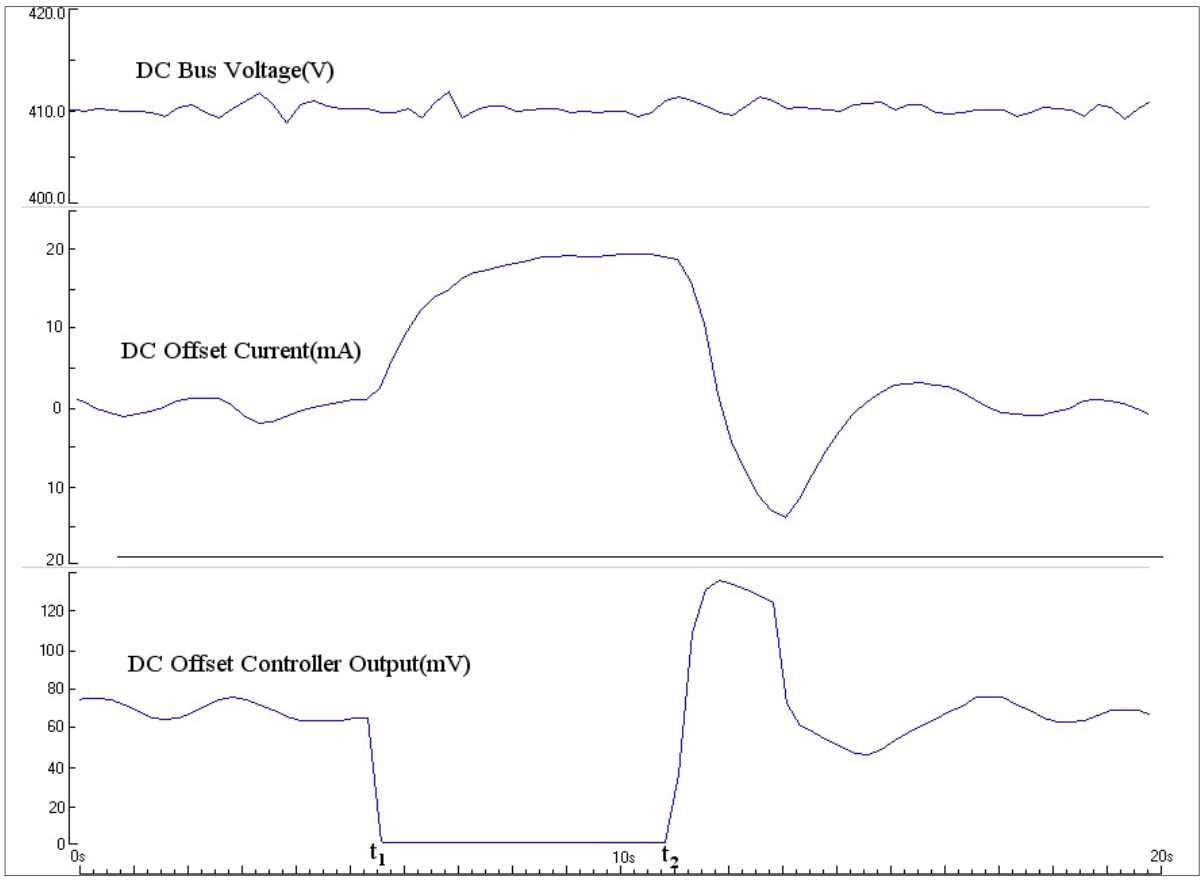


Figure 6.18: Non-Interaction between DC Offset and DC Bus Control Loops

Figure 6.18 illustrates the absence of interaction between the DC bus voltage control loop and the DC-Offset control loop. The DC-Offset control loop is opened by forcing the controller output to zero at time t_1. The loop is closed again at time t_2. The DC offset current signal, which has been extracted from the output of the DC offset sensor by additional filtering, responds accordingly. It increases as a result of the DC offset loop being opened and returns to zero after a transient period upon closure of the loop. Clearly, the DC bus voltage, also shown in figure 6.18, is unaffected by operation of the DC offset control loop.

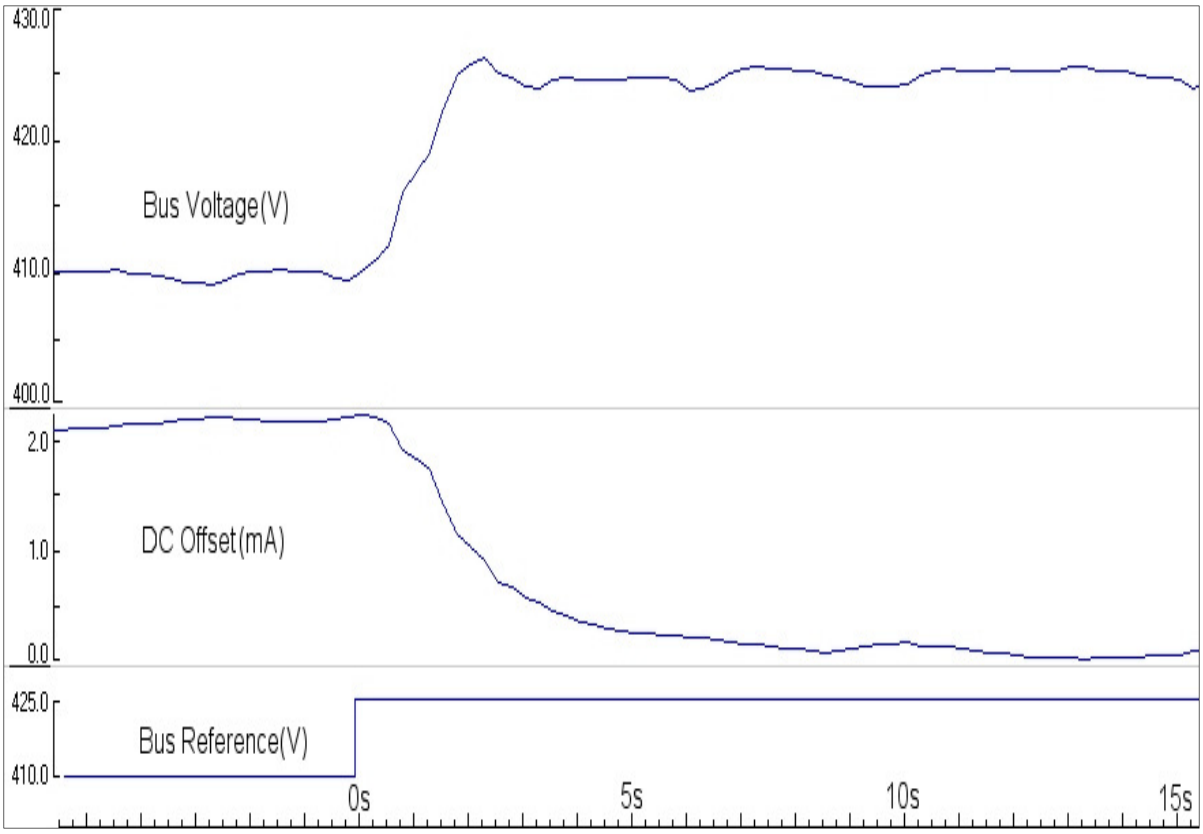


Figure 6.19 Apparent coupling between Bus Voltage and DC Offset Loops (DC offset loop disabled)

While the aim of the previous test was to assess the effect of operation of the DC offset controller on v_{dc} , the effect of operation of the DC bus controller on the DC offset level was also investigated. With the DC offset control loop disabled a reference step to the DC bus voltage was applied and the results recorded. The test results are shown in figure 6.19 above. Having clearly stated before that there is no coupling between the control loops, reference to figure 6.19 would appear to somewhat contradict these earlier statements. However it should be noted that the results of figure 6.19 merely indicate that there is a relationship between the level of DC offset from the controller and the inverter current output. This was verified with the DC offset compensation loop disabled and monitoring the steady state DC offset level achieved at various output current levels, the results of which are given in table 6.2.

Table 6.2: DC Offset Currents at Various Inverter Output Levels

Inverter AC Output Current current(A rms)	Inverter DC offset with control loop open current(mA)	Inverter DC offset with control loop closed current (mA)
1.0 A	30mA	1.02mA
2.0A	13mA	0.86mA
3.0A	-8.1mA	0.52mA
4.0A	-22mA	0.61mA

It was found that without a closed DC offset control loop the level of DC offset current was a function of inverter output. As shown in table 6.2, the DC offset controller operates to ensure that the DC offset current remains within acceptable limits irrespective of the level of inverter output current.

6.6 Summary

This chapter has focussed on the dynamic performance of two methods of elimination of DC injection by single-phase transformerless grid-connected inverters. The first method was proposed by Sharma[10,46] but no design or performance analysis were reported. The conclusion based on analysis and tests carried out as part of this thesis project is that whilst the proposed method is effective, it is costly, bulky and it represents a significant decrease in energy efficiency. The reason for this is the requirement for a relatively large inductor core.

The alternative DC offset sensor proposed here is effectively a dual stage RC filter. Both analogue and digital DC offset controllers based on the proposed sensor have been assessed. Mathematical models for the controllers have been derived. Design procedures based on the models have been proposed, implemented, tested and validated. It has been impossible to compare the dynamic performance of this technique as to the author's knowledge there is no published research on this aspect of DC offset controllers. The steady state response of this technique is better than that given in [11] and no actual figures are given in [10,46]

Chapter 7 Conclusions

An inverter is typically the interface between the AC network and renewable energy converters such as photovoltaic or wind systems. This project has been about newly proposed techniques that would result in cost, efficiency and output quality improvement of such inverters.

7.1 DC Offset Control

A major reduction in cost, mass and volume is arrived at by elimination of the power transformer between the inverter and the AC network. The presence of the transformer , however, is a safeguard against the injection of DC into the AC mains. Without the transformer, DC injection may become a problem. A major objective of this project was to ensure DC injection remains below acceptable levels in the case of the transformerless single-phase grid-connected inverters. While the concept of using DC offset PI controllers to ensure injected DC offset current remain at zero had previously been proposed, no publication was found on quantitative analysis of their dynamic performance.

Two DC offset controllers, using different DC offset sensors, were investigated. The first one, termed the RLLC sensor, was based on a 1:1 mutually coupled inductor pair and an RC filter. While this sensor had been previously proposed, no analysis of its performance had been carried out. As part of this project, a design procedure for the RLLC based DC offset controller was developed. Also a mathematical model was produced to assess its dynamic performance. The mathematical model was validated by laboratory tests. While the performance of the RLLC based DC offset controller was found to be satisfactory, its major drawback was cost, size and power loss of the 1:1 mutually coupled inductor. It was

found that the length of the inductor time constant needed to meet reasonable design specifications was relatively long. This meant a substantial amount of copper, of the order of 0.75kg and a large core area of the order of 1500mm^2, was needed. Core loss was of the order of 5W. It was concluded that the RLLC based DC offset controller was not a practical solution.

The second DC offset controller was based on a dual stage RC sensor. This allowed reduction of AC in the output of the sensor to negligible levels while maintaining good speed of response. Both the analogue and the digital versions gave satisfactory performance with DC injection sustained below 1mA, well within the limits imposed by standards such as Australian Standard AS 4777.2 or United Kingdom's ER G83/1.

7.2 Reduction in Current Distortion

A detailed comparison of unipolar and bipolar inverter switching was carried out from the inverter output current distortion point of view. Important factors that had to be taken into consideration were:

- Range of switching frequencies
- Distortion near the peak of the AC supply voltage waveform;
- Distortion near the zero-crossing of the AC supply voltage waveform;
- The effect of switching delay
- Response of the ripple filter; and
- Switching power loss

It has been confirmed by detailed theoretical analysis and by laboratory tests that bipolar switching has the following advantages:

1) Well defined range of switching frequencies, in the case of hysteretic current control, making ripple filter design relatively straight forward.
2) From the point of view of distortion, excellent performance near the zero crossing of the voltage waveform.
3) No additional low frequency distortion caused by switching delay.

Disadvantages of bipolar switching are:

1) Higher switching power losses;
2) Increased ripple frequency distortion near the peak of the AC supply voltage caused by switching delay.

Detailed analysis and laboratory tests confirmed that unipolar switching has the following advantages:

1) Lower switching power loss; and
2) Ripple content near the peak of the AC supply voltage waveform is less affected by switching delay compared to bipolar switching.

Disadvantages of unipolar switching are:

1) The lower end of the switching frequency range, in the case of hysteretic current control, is not well defined and consequently the range of ripple frequencies present in the output current to be filtered is broader than in the case of bipolar switching.
2) Heavy ‘ringing’ at the ripple filter resonant frequency near the zero crossing of the AC supply voltage waveform; and
3) Additional low frequency distortion due to switching delay.

An important outcome of this research project is mixed-mode inverter switching. It has been demonstrated both by theoretical analysis and by laboratory tests that the mixed-mode switching combined the best features of bipolar and unipolar switching. The bipolar interval of mixed-mode switching is centred around the zero crossing of the AC supply voltage. The size of the bipolar interval that is required to practically eliminate distortion and ringing near the supply voltage zero crossing depends on the level of current demand relative to the tolerance band. For example for an inverter output current that is three times the tolerance band size, the required bipolar interval is nine degrees on either side of the AC voltage zero crossing. Since the size of the bipolar interval is normally small, typically two milliseconds or so, mixed-mode switching retains the lower switching loss advantage of unipolar operation. For example under nominally identical operating conditions with a DC bus voltage of 410V, AC supply voltage 247V and inverter output current 2.5A rms, measured inverter power loss was respectively 43.0W, 58.5W and 43.2W(table 4.4) for unipolar, bipolar and mixed-mode switching.

Mixed-mode switching avoids the ripple filter ringing and current distortion problem suffered by unipolar switched inverters. Mixed-mode switching also retains the unipolar operation advantage of lower ripple current magnitude near the peak of the AC supply waveform. Ripple filter design for mixed-mode switching is as straight forward as that for bipolar switching. This positive outcome is as a result of using bipolar switching for only a few degrees either side of the AC supply waveform zero crossing to replace unipolar switching. In mixed-mode switching, within every half cycle of the inverter output current waveform there are two transition events, one from bipolar switching to unipolar and one from unipolar switching to bipolar switching. Each one of these transitions represents a sudden disturbance to the ripple filter. It has been found that in the presence of switching delays of around 5μs that the magnitude of the ringing at transition events could be high

enough to be a problem. A compensation technique has been developed to minimise the disturbance due to the ripple filter at the transition events. Fundamentally the disturbance at transition events is due to differences in the averaged inverter output current waveforms for unipolar and bipolar switching methods. The compensation technique adds an offset compensation signal to the unipolar reference. The compensation signal in the respective unipolar and bipolar reference waveforms allow for smoother transition from unipolar to bipolar switching and vice versa, thus reducing the impact on the ripple filter and reducing distortion of the current waveform at these transition events.

7.3 Summary

A transformerless single-phase grid connected inverter system has been investigated, designed and tested. Its innovative features are:

a) Mixed-mode switching to make the most of the desirable features of unipolar and bipolar switching. In particular the switching power loss advantage of unipolar switching and the low current distortion feature of bipolar switching are retained.

b) A compensation technique that allows practically disturbance free transition from unipolar switching to bipolar switching and vice versa. This compensation technique also eliminates low frequency harmonics caused by switching delay.

c) A DC offset controller that maintains DC injection below 1mA. Both analogue and digital versions have been successfully designed and implemented. Comprehensive dynamic analysis of both versions has been carried out.

d) Use of digital potentiometers for implementation of the hysteretic current controller thus avoiding the need for high precision analogue or fast digital multiplication.

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Appendix A

A.1: System Overview

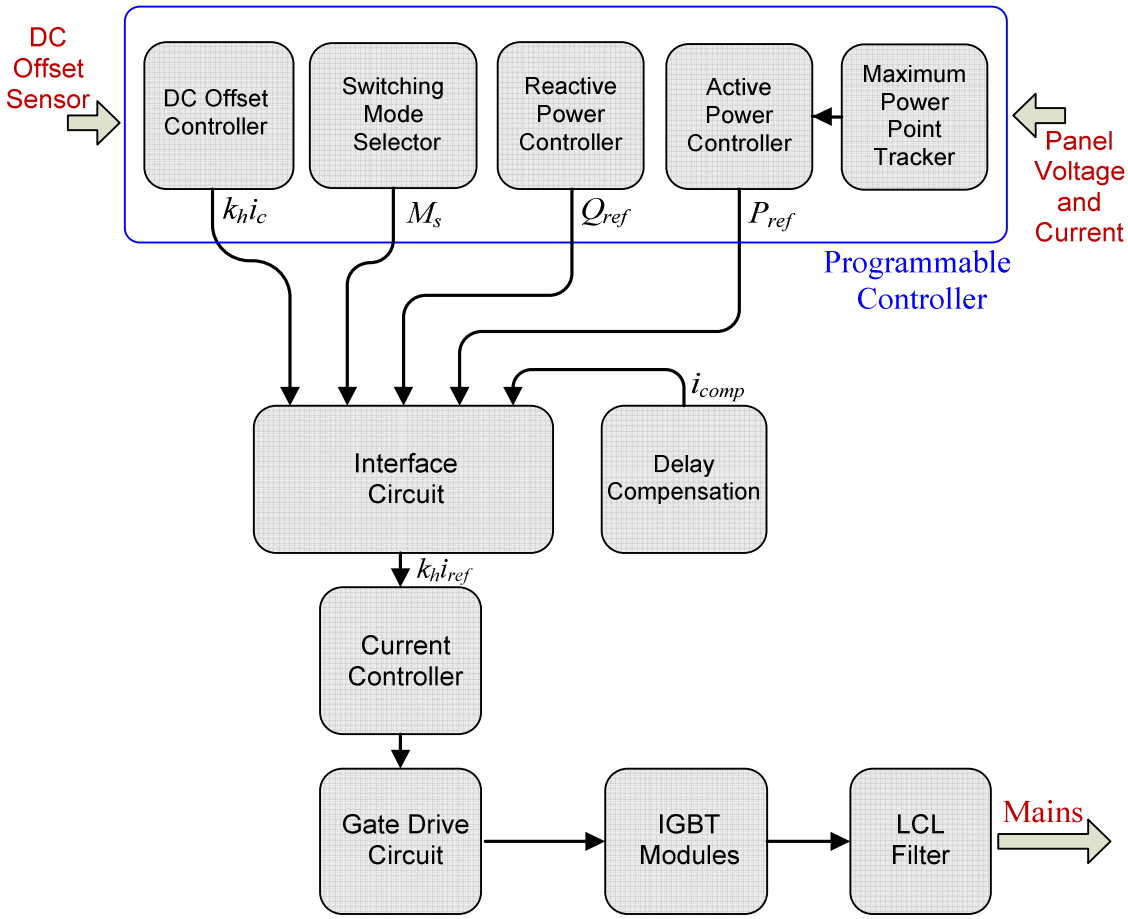


Figure A.1: System Overview Block Diagram

This appendix provides a description of the hardware used to implement the inverter. As shown in figure A.1 the software platform used was the Siemens CPU244XP programmable controller. This industrial controller was chosen because of its compliance to European Community (CE) EMC Directive 89/336/EEC and noise immunity under EN61000--6—21, ease of programming and ease of interfacing with other hardware. Software developed as part of this project consisted of the DC offset controller (chapter 6), the inverter current controller switching mode selector (chapter 4) and the maximum power tracker (chapter 5). While a reactive power controller was not developed, the inverter had reactive power injection capability (as illustrated by figure A.2). Apart from the programmable controller, figure A.1 represents other hardware modules which are described in detail in the following pages.

A.2: Illustration of Inverter Non-Unity Power Factor Operation

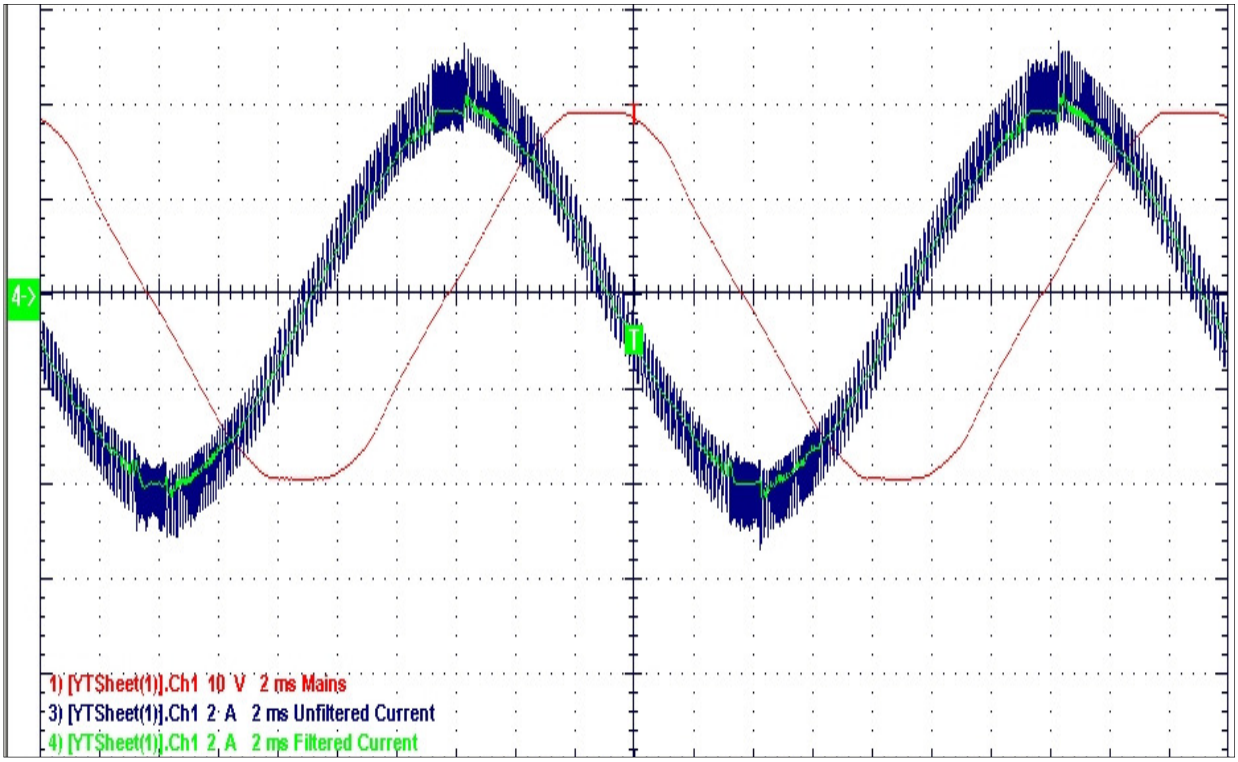


Figure A.2: Inverter Output Current Leading supply voltage by 81°

A.3: Zero Phase-Shift Filter

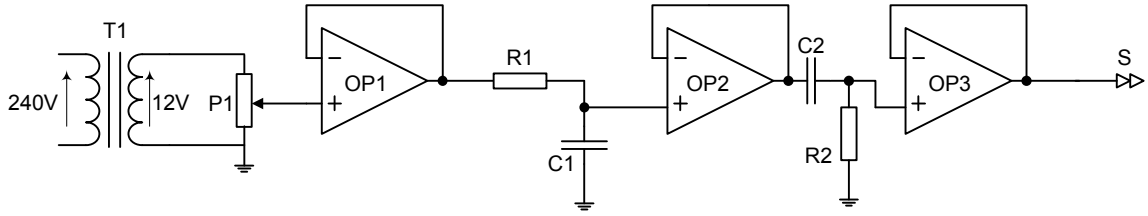


Figure A.3: Zero Phase-Shift Filter Circuit

An AC signal synchronised with the AC supply voltage is needed for the generation of the reference current $\boldsymbol{i_{ref}}$ which, as shown in figure A.1, is the input to the current controller. Reference current $\boldsymbol{i_{ref}}$ is the output of the zero-phase shift filter shown in figure A.3. A 240V/12V 50Hz miniature transformer is used to obtain a reference signal (approximately 5V rms) in phase with the supply voltage. Because of the undesirable presence of harmonics, the signal is filtered. As shown in figure A.3, the overall transfer function for the two stage filter is:

$$\frac{jff_o}{(jf + f_o)^2}$$

where R = $\mathbf{R_1} = \mathbf{R_2}$ and C = $\mathbf{C_1} + \mathbf{C_2}$ have been chosen so that f_o = 50Hz. This implies that the filter has the desirable effect of practically zero phase-shift at 50Hz while having significant attenuation at higher harmonic frequencies.

A.4: Zero Phase-shift Filter Effectiveness

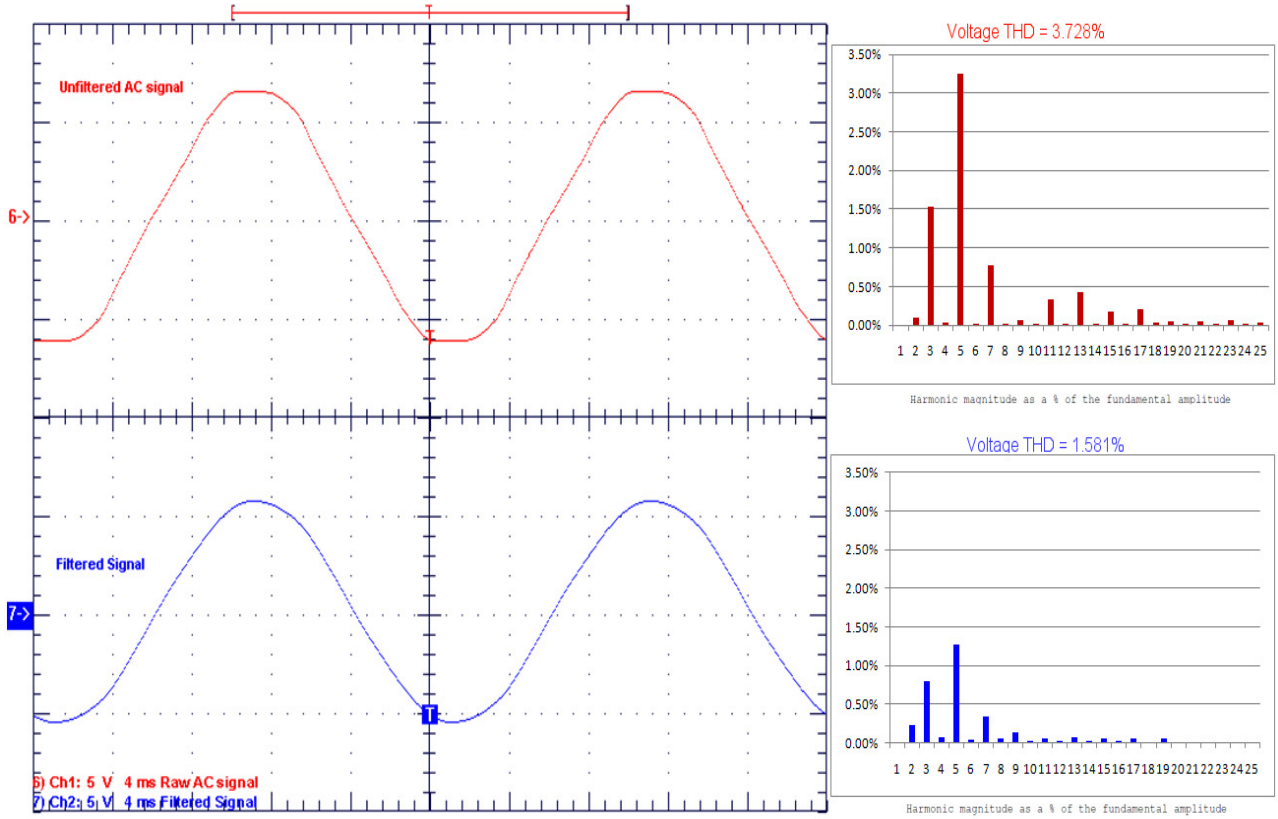


Figure A.4: Zero Phase-shift Filter Effect

Figure A.4 shows that the output of the filter is significantly less distorted when compared to the raw AC signal. A significant reduction in the total harmonic distortion (THD), and higher frequency harmonics as shown in the respective waveform spectra, was also achieved.

A.5: Active and Reactive Components of $k_h i_{ref}$

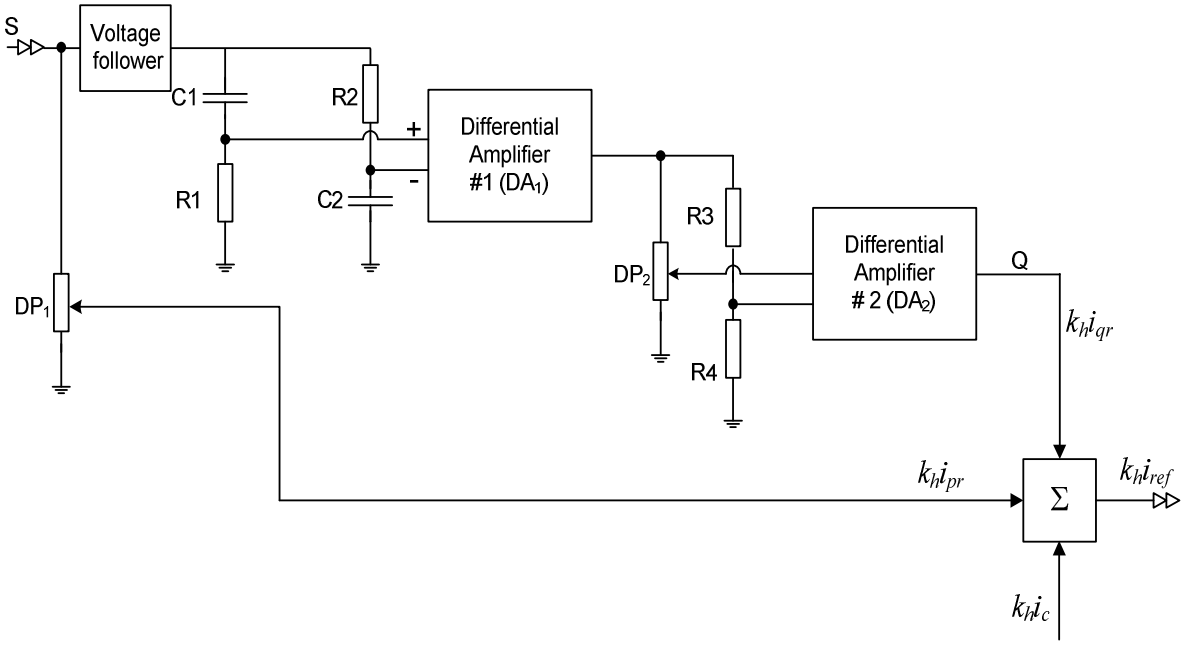


Figure A.5: Active and Reactive Component of $k_h i_{ref}$

The 5V output (S) from the zero phase-shift filter circuit is used to generate the current reference signal $k_h i_{ref}$ as shown in figure A.5. Digital potentiometer DP_1 is used to generate the active component of $k_h i_{ref}$. As described in chapter 5 the digital potentiometer **DP_1** is adjusted according to the output of the DC bus voltage controller to maintain active power balance.

To create a signal for the reactive component of $k_h i_{ref}$, signal S from the zero phase-shift filter is phase shifted by 90^o. The 90^o phase shifter is realised by components **R_1, C_1, R_2, C_2** and differential amplifier **DA_1**. The output of **DA_1** is of nominally fixed magnitude. Digital potentiometer **DP_2**, and the voltage divider made up of **R_3** and **R_4** and differential amplifier **DA_2** allows the 90^o phase shifted signal to be adjusted from 0 to a maximum value of 4V leading or lagging. Digital potentiometer **DP_2** is adjusted via software within the programmable controller. The reactive component of $k_h i_{ref}$ is maximum and lagging when **DP_2** is at the zero position. When the output terminal of **DP_2** is in its middle position the reactive component of $k_h i_{ref}$ is zero. The reactive component of $k_h i_{ref}$ is maximum and leading when **DP_2** is at its maximum position. As described in chapters 5 and 6, the summer circuit combines active and reactive power references with DC offset Control to produce the reference current signal $k_h i_{ref}$.

A.6: Bipolar Current Controller

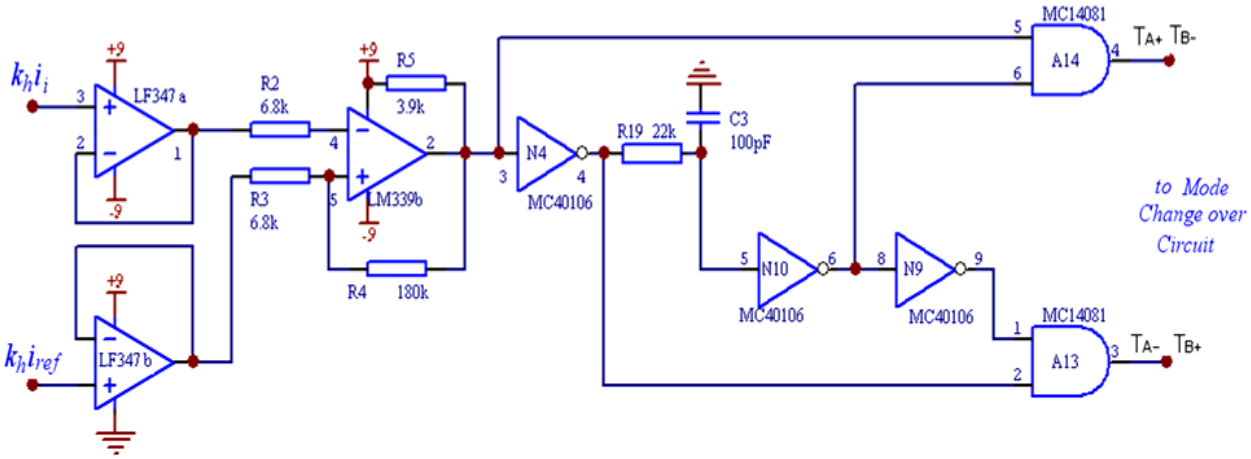


Figure A.6: Current Controller (bipolar)

Figure A.6 shows the current controller used for the bipolar switching mode. The inverter current signal $k_h i_i$ and the reference signal $k_h i_{ref}$ are compared by the comparator (LM339b). The comparator circuit incorporates an inbuilt hysteresis band given by:

$$V_{band} \simeq \pm 9R_3 / (R_3 + R_4)$$

Since k_h was 1.25V/A, this corresponds to a nominal tolerance band of ±0.3A. However, in practice, as can be seen for example in figure A.2, the tolerance band appears wider due to the effects of delay in controller circuit. The output of the comparator goes high when $k_h i_i$ goes lower than $k_h(i_{ref} - I_{tol}/2)$. This results in transistors T_{A+} and T_{B-} of the inverter being turned on and T_{A-} and T_{B+} being turned off. The output of the comparator goes low when $k_h i_i$ goes higher than $k_h(i_{ref} + I_{tol}/2)$. This results in inverter transistors T_{A-} and T_{B+} being turned on and T_{A+} and T_{B-} being turned off. Components R_{19}, C_3, inverting buffers N_{10} and N_9, and AND gates A_{13} and A_{14} are used to provide the required blanking time when the inverter transistors are switching states. While turn-off happens without intentional delay, turn-on is delayed by an amount determined by the product of the resistance of R_{19} and capacitance of C_3. Their values were chosen to give a blanking time of 2.2µs.

A.7: Unipolar Control Circuit

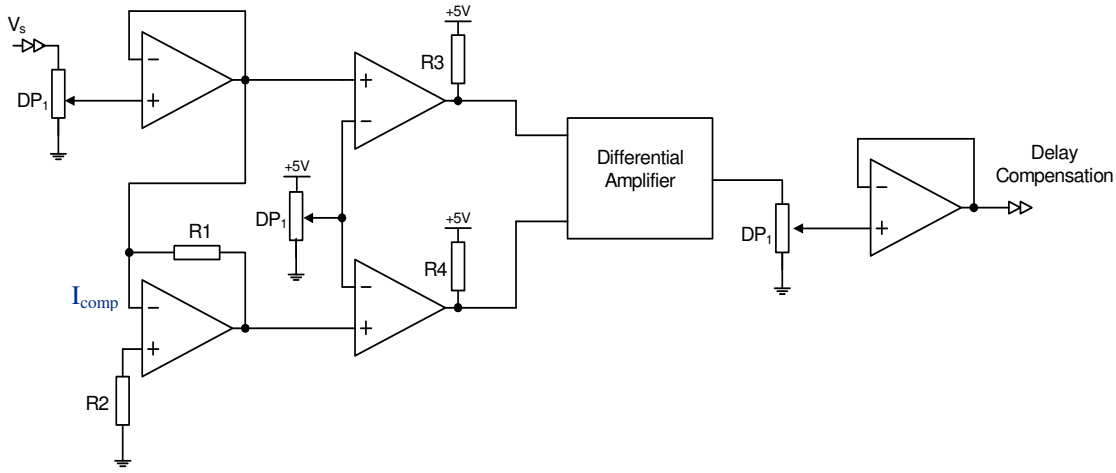


Figure A.7: Current Controller Circuit (Unipolar)

Figure A.7 shows the current controller for unipolar switching. The bottom section which is used to control inverter transistors $\mathbf{T_{A+}}$ and $\mathbf{T_{A-}}$ is identical to the previously described bipolar controller shown in figure A.4.

The top section is used to control inverter transistors $\mathbf{T_{B+}}$ and $\mathbf{T_{B-}}$. The aim is to have $\mathbf{T_{B+}}$ on during the positive half cycle of the AC supply voltage and $\mathbf{T_{B-}}$ on during the negative half cycle. The output of the comparator (**LM339a**) is high during the positive half cycle and low during the negative half cycle. This results in $\mathbf{T_{B+}}$ being on during the positive half cycle and $\mathbf{T_{B-}}$ being on during the negative half cycle. Components $\mathbf{R_7}$, $\mathbf{C_1}$, inverting buffer $\mathbf{N_1}$, and AND gates $\mathbf{A_1}$ and $\mathbf{A_5}$ are used to provide a blanking time of 2μs when the transistors change states.

A.8: Multi-Mode Controller Schematic

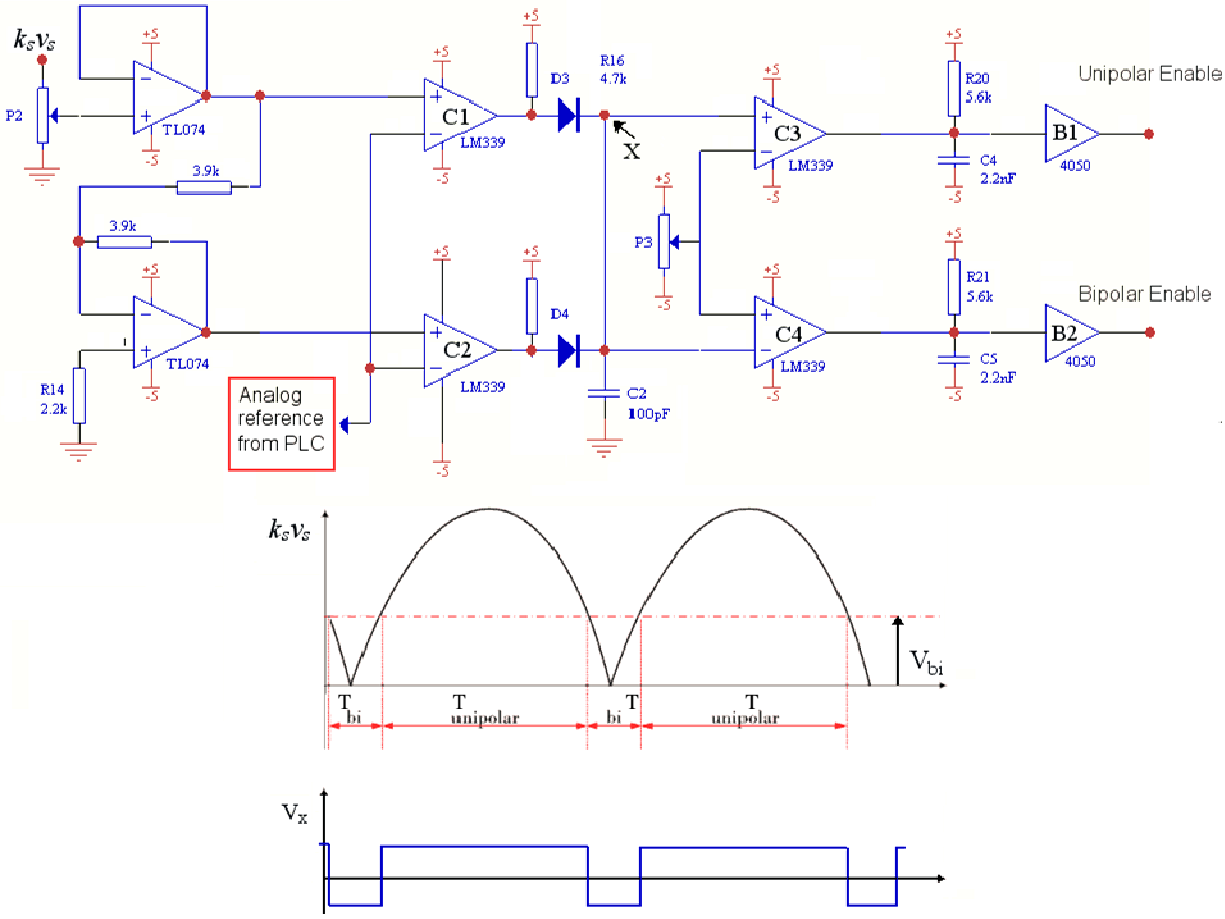


Figure A.8: Mode Control Circuit

As elaborated in chapter 4 the inverter is capable of operating in three modes. That is in: bipolar mode, unipolar mode and multi-mode. Mode control is carried out by the circuit in figure A.8. The programmable controller outputs an analogue signal V_{bi} which determines the mode of operation. Comparator $\mathbf{C_1}$ compares $\mathbf{V_{bi}}$ with the AC supply voltage signal $k_s v_s$ whereas comparator $\mathbf{C_2}$ compares $-k_s v_s$ with $\mathbf{V_{bi}}$. If $\mathbf{V_{bi}}$ is made higher than the peak value of $k_s v_s$, then the outputs of the comparators are both low and constant. Potentiometer **P3** is adjusted to provide a positive voltage of about 1V at the inputs of comparators **C3** and **C4**. Therefore when $\mathbf{V_{bi}}$ is greater than the peak value of $k_a v_s$, the output of the non-inverting buffer $\mathbf{B_1}$ is high whereas the output of non-inverting buffer $\mathbf{B_2}$ is low. This means that if $\mathbf{V_{bi}}$ is greater than the peak value of $k_a v_s$ purely bipolar operation results.

If $\mathbf{V_{bi}}$ is made negative, then the outputs of comparators $\mathbf{C_1}$ and $\mathbf{C_2}$ are both high and constant. This causes $\mathbf{V_x}$ to be equal to the positive supply rail voltage, resulting in the output of the non-inverting buffer $\mathbf{B_1}$ to be low and the output of non-inverting buffer $\mathbf{B_2}$ to be high. This means that if $\mathbf{V_{bi}}$ is less than zero then purely unipolar operation results.

If $\mathbf{V_{bi}}$ falls between zero and the peak value of $k_a v_s$ then multi-mode operation is the result. That is, as shown in figure A.8, for time interval T_{bi} , centred around the zero crossing of the AC supply voltage v_s , operation is bipolar. Operation is unipolar for the rest of the time.

Components $\mathbf{R_{20}}$, $\mathbf{C_4}$, $\mathbf{R_{21}}$ and $\mathbf{C_5}$ provide a short blanking time during transition from unipolar operation to bipolar operation and vice-versa. The blanking time is achieved by allowing the outputs of $\mathbf{B_1}$ and $\mathbf{B_2}$ to change instantaneously from high to low, but delaying the reverse transition. The values chosen for the RC circuit resulted in a blanking time of 1.2μs.

A.9: Mode Changeover Circuit

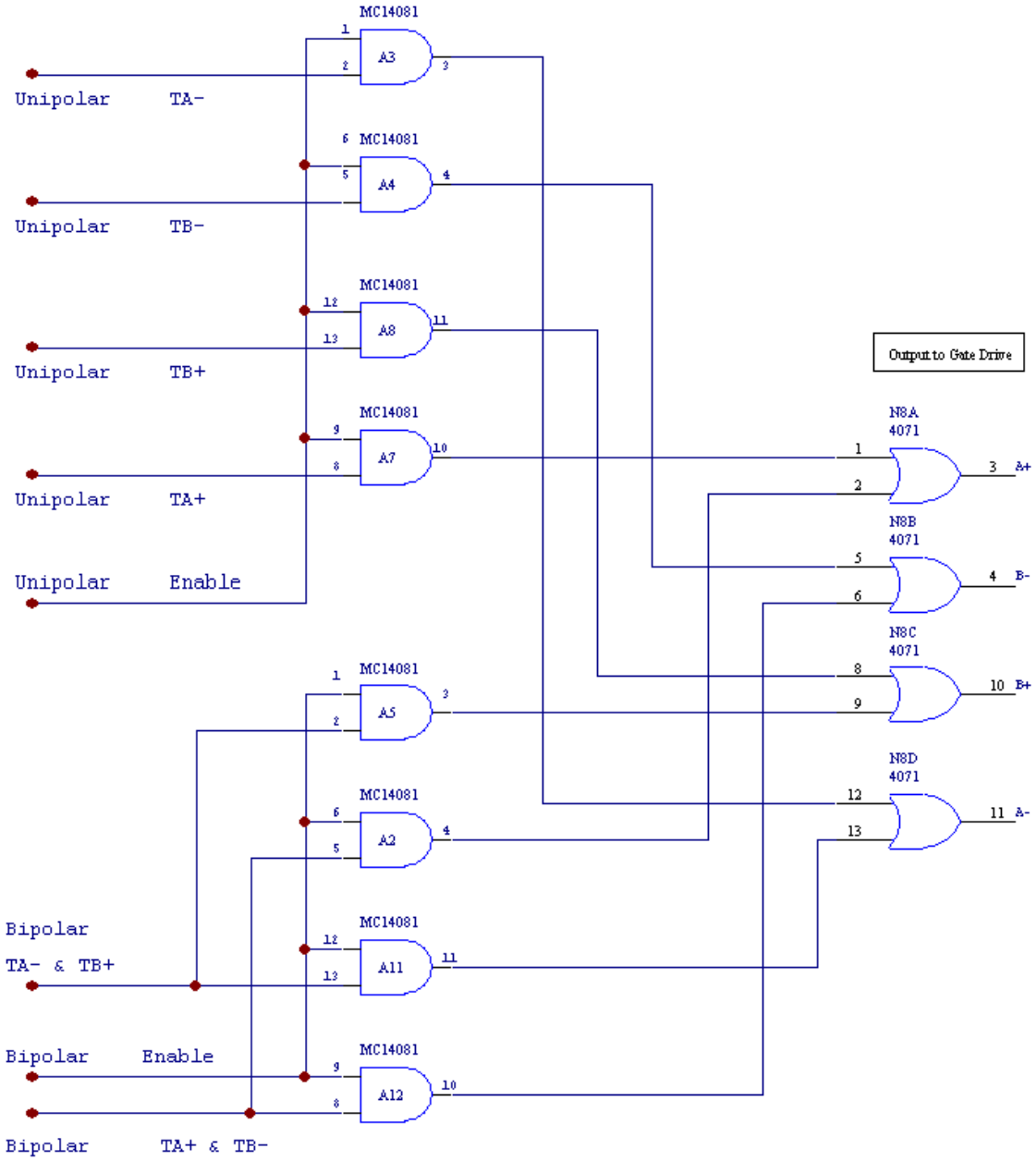


Figure A.9: Mode Changeover Circuit

The output signals from the bipolar current controller (figure A.6), the unipolar current controller (figure A.7) and the mode control circuit (figure A.8) are combined in figure A.9 to generate signals for the gate drive circuit.

A.10: Analogue PI Controller

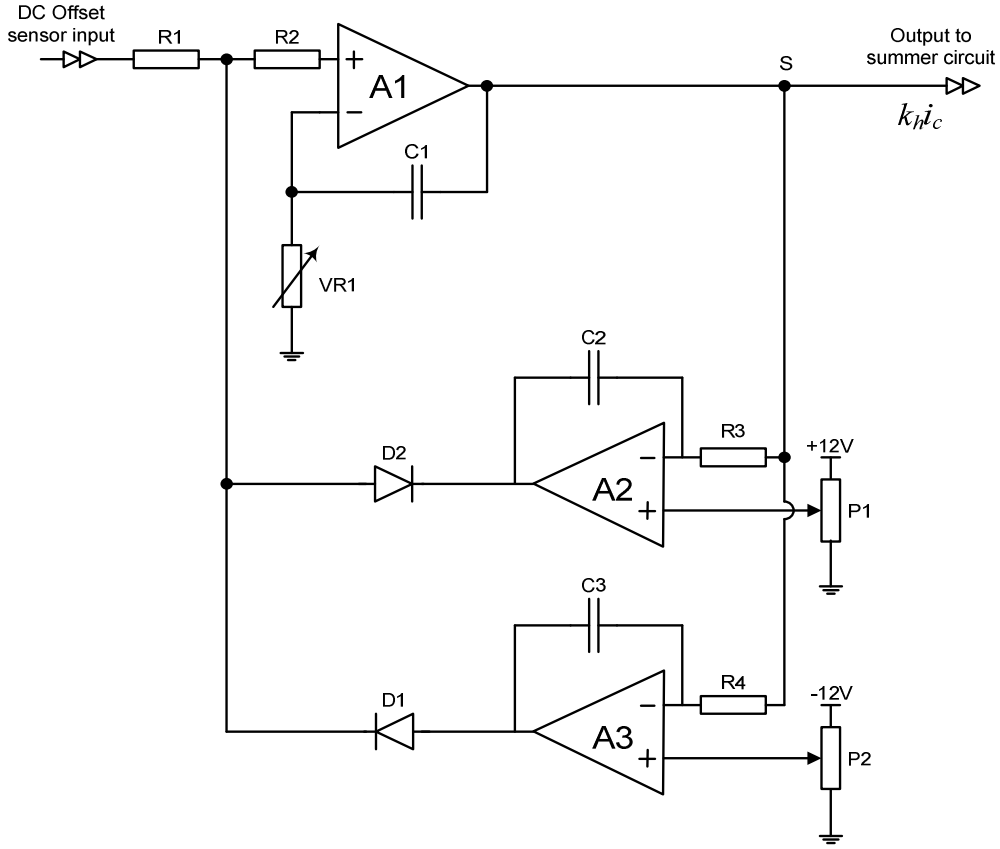


Figure A.10: Analogue PI Controller

The analogue DC offset PI controllers (sections 6.2 and 6.3) were implemented using the circuit in figure A.10. Operational amplifier A_1 is used to implement both the proportional and integral control terms. The transfer function is given by:

$$\frac{(s + {}^{1}/_{\tau_i})}{s} = \frac{(s + {}^{1}/_{RC_1})}{s}$$

where: R = setting of V_{R1}

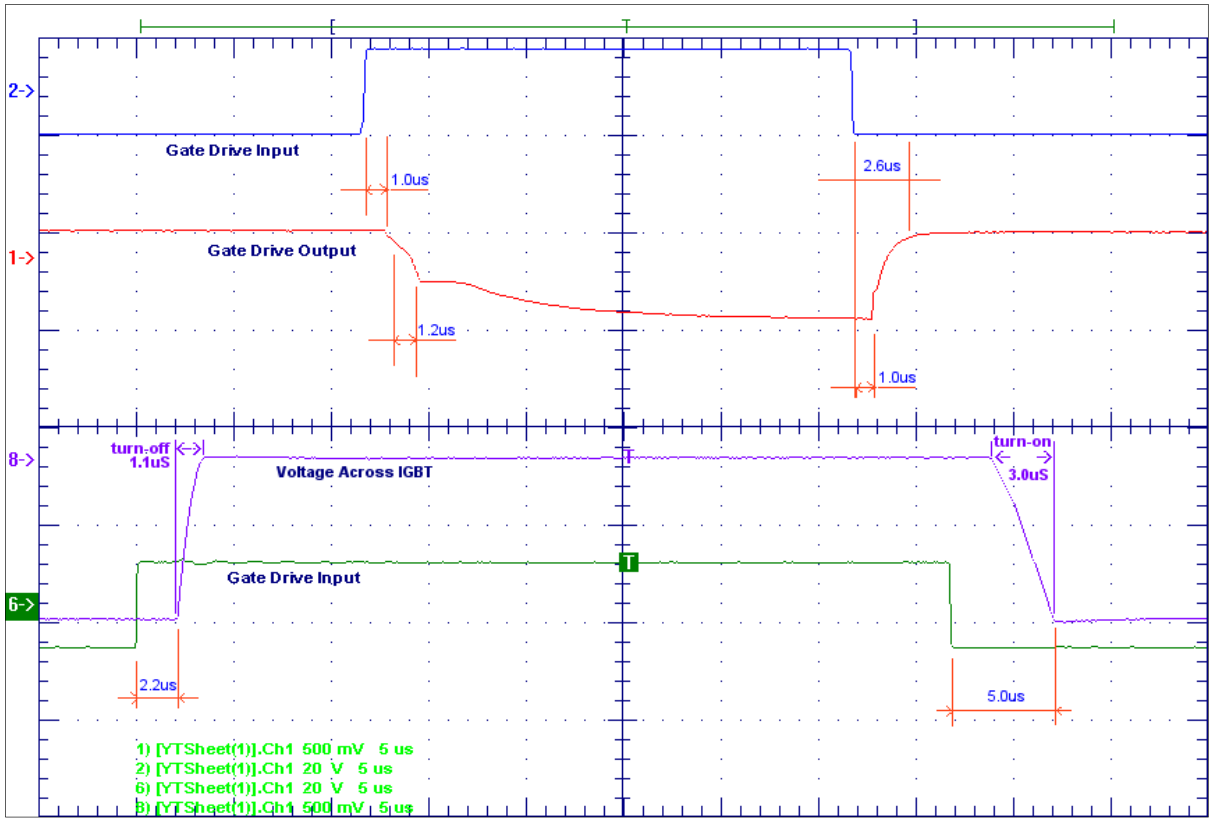
τ_i = integration time constant

= RC_1

Operational amplifier $\mathbf{A_2}$ and components $\mathbf{D_2}$, $\mathbf{C_2}$, $\mathbf{R_3}$ and $\mathbf{P_1}$ prevent the compensating current signal ($\boldsymbol{k_h i_c}$) from going above the value set by potentiometer $\mathbf{P_1}$. This value was set at 200mV. Similarly operational amplifier $\mathbf{A_3}$ and components $\mathbf{D_1}$, $\mathbf{C_3}$, $\mathbf{R_4}$ and $\mathbf{P_2}$ prevent the compensating current signal ($\boldsymbol{k_h i_c}$) from going below the value set by potentiometer $\mathbf{P_2}$.

With the system operating within limits set by $\mathbf{P_1}$ and $\mathbf{P_2}$ both $\mathbf{D_1}$ and $\mathbf{D_2}$ are reverse biased and the limiting circuits have no effect. Now consider the situation when the output attempts to go above the limit set by $\mathbf{P_1}$. This attempt will have no effect on the output of $\mathbf{A_3}$ which remains saturated near the negative supply rail causing $\mathbf{D_1}$ to remain reverse biased. The output of $\mathbf{A_2}$, however, quickly drops from its saturated value near the positive supply rail because of the relatively small value of capacitance $\mathbf{C_2}$. The value of the output of $\mathbf{A_2}$ will remain at exactly one diode voltage drop below zero as long as the voltage input from the DC offset sensor is above zero. As soon as the input voltage from the DC offset sensor goes below zero $\mathbf{D_2}$ becomes reverse biased and integration resumes. The scenario is similar when the bottom limit is reached.

B.1: Switching Delay



B.1: Typical IGBT Switching Waveforms Showing Delays

The inverter was implemented using Semikron®SKM100GB063D half bridge IGBT modules and the Semikron® SKHI22B isolated dual gate drive modules. The choice of gate drive resistance was a compromise between switching speed, switching losses and EMI generation. The gate drive resistances chosen were 68Ω for turn on and 27Ω for turn off. Figure B.1 shows typical turn on and turn off delays. Turn on delay shown could be reduced by approximately 1 to 2 microseconds depending on the physical parameters such as cable length to the solar array.