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Research Article

AlN/GaN-Based MOS-HEMT Technology: Processing and Device Results

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Process development of AlN/GaN MOS-HEMTs is presented, along with issues and problems concerning the fabrication processes. The developed technology uses thermally grown Al_2O_3 as a gate dielectric and surface passivation for devices. Significant improvement in device performance was observed using the following techniques: (1) Ohmic contact optimisation using Al wet etch prior to Ohmic metal deposition and (2) mesa sidewall passivation. DC and RF performance of the fabricated devices will be presented and discussed in this paper.

1. Introduction

The search for improved high power and high frequency performance has called attention to the most recent development in aluminium nitride/gallium nitride- (AlN/GaN-) based high electron mobility transistors (HEMTs) which target future microwave power devices. Key properties of this material system are high 2DEG sheet carrier concentration at the heterojunction interface, high carrier electron velocity, and large electric breakdown field, and so superior performance compared to conventional AlGaN/GaN devices could be achieved. With improvements in material growth and processing techniques, record performances made in this material system include 2DEG sheet carrier concentration over $3 \times 10^{13}\,cm^{-2}$ with very low sheet resistance, R_{sh}, $<150\,\Omega/\square$ [1, 2], output drain current density over 2 A/mm, transconductance over 400 mS/mm [3, 4], and cutoff frequency over 100 GHz [5].

Despite the demonstrated potential, problems such as surface sensitivity [6], high leakage current [7], and high contact resistance [3, 7] have limited the performance and reliability of these devices. Several techniques have been reported to overcome these problems. Gate dielectrics and surface passivation have been used to suppress the leakage current. Equally important, the gate dielectric or surface passivation also protects the epitaxial layers during device fabrication. For conventional HEMT processing which employs mesa etching for device isolation, leakage currents are not confined on the active area region but also along the mesa sidewalls, especially in the region where the gate metallisation overlaps with the exposed channel edge [8]. This can lead to the poor device performance, and so it is also important to protect and passivate the mesa sidewalls.

In this paper, the process development of AlN/GaN MOS-HEMT technology will be reviewed and discussed. The devices discussed here employ thermally grown Al_2O_3 as a gate dielectric and surface passivation [6]. This approach provides an opportunity to define the Ohmic contact areas by wet etching of Al (and optimisation of this processing step) prior to the formation of Al_2O_3 and Ohmic metal deposition [9]. Leakage currents on the mesa sidewalls were found to be significant, and a process technique to suppress this will also be described.

2. Process Technology Development

2.1. Ohmic Contact Optimisation. Optimal performance of AlN/GaN-based HEMT devices requires the use of low-resistance, thermally stable Ohmic contacts with good surface morphology. This is required for the following reasons: (1) to obtain the maximum value of drain current, I_{DSMAX}, (2) to reduce the on-resistance, (3) to minimise the power dissipation in the Ohmic contacts because of the high current densities, and (4) to obtain the maximum value of extrinsic

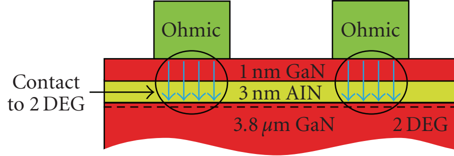


Figure 1: Optimised TLM processing summary for unprotected and unpassivated AlN/GaN HEMT samples. Processing includes (a) sample cleaning with acetone, isopropanol, and deionised water, (b) deoxidation, (c) Ohmic metallisation, (d) Ohmic annealing, and (e) TLM measurements.

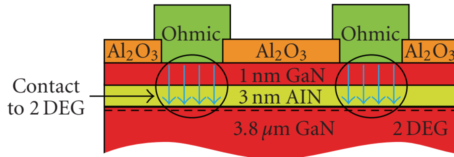


Figure 2: Optimised TLM processing summary for protected and passivated AlN/GaN MOS-HEMT samples. Processing includes (a) sample cleaning with only deionised water and deoxidation, (b) 2 nm Al deposition, (c) etching Al from Ohmic contact regions, (d) thermal oxidation of Al, (e) Ohmic metallisation, (f) Ohmic annealing, and (g) TLM measurements.

transconductance, G_{MAX}, which results in the enhancement of the current gain cutoff frequency, f_T, as well as maximum frequency of oscillation, f_{MAX}, of the devices. For these reasons, Ohmic contact optimisation processing for HEMT and MOS-HEMT in the AlN/GaN material systems is crucial to achieving good device performance. Details of the Ohmic contact process optimisation were reported in [9] and are summarised here.

Ohmic contacts on both protected (with 2 nm evaporated Al which is later oxidised to form Al_2O_3) and unprotected (as grown) AlN/GaN samples were fabricated and characterised. Figure 1 shows the optimised transmission line method (TLM) processing summary for unprotected and unpassivated AlN/GaN HEMT samples while Figure 2 shows the optimised TLM processing summary for protected and passivated AlN/GaN MOS-HEMT samples. A summary of the optimised R_C and R_{sh} values on HEMT and MOS-HEMT is shown in Table 1. The sheet resistance of the protected sample (159 Ω/□) is about one third that of the unprotected one (450 Ω/□). Clearly, protection of the samples during processing is the key to good performance. On the other hand, the TLM results of unprotected and unpassivated samples exhibited very low contact resistances for this material system with an average value of 0.31 Ω·mm. This result provides an indication of how Ohmic contacts may be processed for a protected sample.

By employing the structure in Figure 2 for TLM processing, optimisation of wet etching using $16H_3PO_4 : HNO_3 : 2H_2O$ Al etch solution prior to Ohmic metallisation produced very low contact resistance as well as very low sheet resistance as reported in [9]. Figure 3 shows the measured I-V characteristics on 5 μm TLM gap spacing of annealed Ohmic contacts under different Al etch times prior to Ohmic

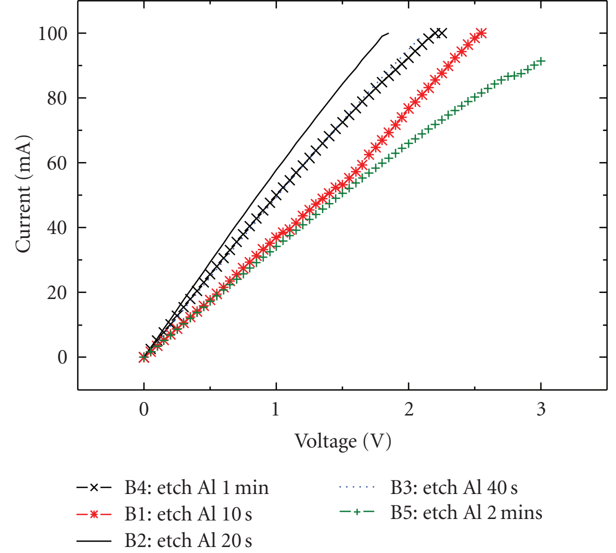


Figure 3: Current-voltage (I-V) characteristics on 5 μm TLM gap spacing of annealed Ohmic contacts under different Al etch times prior to Ohmic metal deposition.

Table 1: Summary of results for the optimised R_C and R_{sh} values on HEMT and MOS-HEMT samples in the AlN/GaN material system.

Sample	Description	R_C, Ω·mm	R_{sh}, Ω/□
A	Unprotected and unpassivated (HEMT)	0.31	480
B2	Protected and passivated (MOS-HEMT)	0.49	159

metal deposition. The processing methods for sample B2, on which Al was etched for 20 secs gave the best I-V plot as compared to other etching times. The average values of R_C and R_{sh} for this sample were 0.49 Ω·mm and 159 Ω/□, respectively. By using the correct Al etch time, it seems that the top surface of the semiconductor is etched leaving a good clean surface for metallisation. However, if the sample was left longer in the etchant the contact resistance rises indicating that further undesirable reactions may be taking place. Figure 4 shows the measured contact resistance R_C in comparison with other published work for AlN/GaN-based devices. It is clear that the adopted approach here results in one of the lowest contact resistance values for this material system.

2.2. Gate Wrap-Around MOS-HEMT Optimisation. A gate wrap-around layout technique [10], where the gate electrode encircles the drain as shown in Figure 5, was employed for process development and optimisation on AlN/GaN HEMT structures. This technique consists only of Ohmic and gate metallisation, eliminating the mesa isolation step. During process development, 10 mm × 10 mm samples cleaved from a 2-inch wafer were used. Device fabrication starts with standard sample cleaning using acetone, isopropanol, and deionised water. The optimised Ohmic contact processing

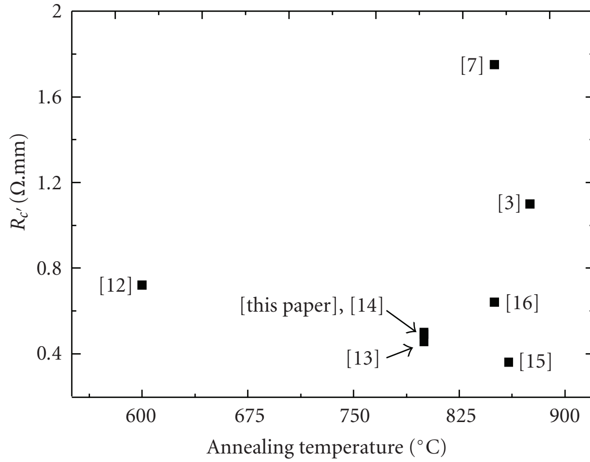


FIGURE 4: Comparison of Ohmic contact resistance, R_C, on AlN/GaN-based devices as a function of annealing temperatures from various publications.

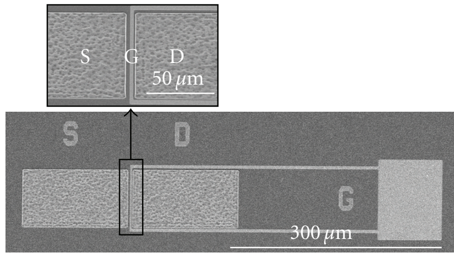
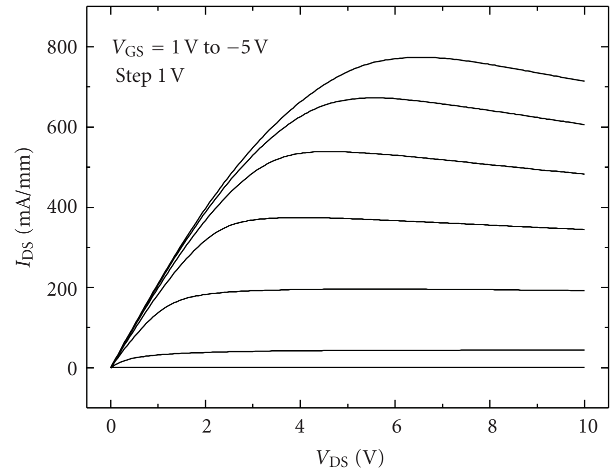


FIGURE 5: SEM micrograph of completed gate wrap-around MOS-HEMT layout. Inset: Device with $L_{SD} = 6\,\mu$m and $L_G = 3\,\mu$m.



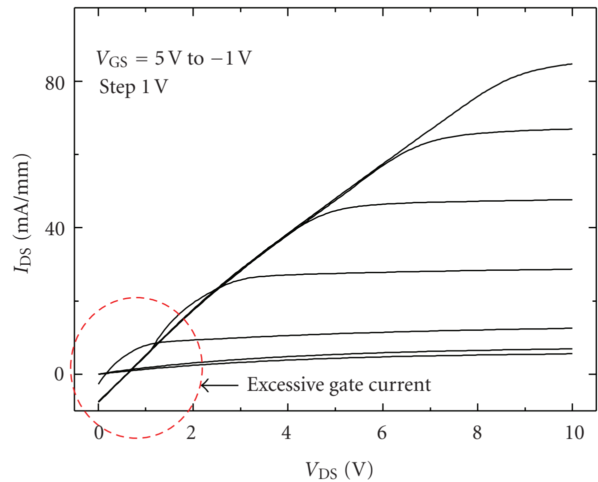


FIGURE 6: I_{DS}-V_{DS} characteristics of fabricated unprotected and unpassivated with $3\,\mu$m × $100\,\mu$m device (a) AlGaN/GaN HEMT and (b) AlN/GaN HEMT.

in Figure 1 was employed for fabrication of unprotected and unpassivated AlN/GaN HEMT devices. Deoxidation was done on the Ohmic contact regions by HCl : $4H_2O$ solution prior to Ohmic metal deposition. Ohmic metal contacts were formed by evaporation of Ti/Al/Ni/Au, followed by a lift-off process, and then annealing at 800°C for 30 secs. Thereafter, gate metal contacts were formed by evaporation of Ni/Au and followed by lift-off process.

AlN/GaN structures are known to be very sensitive to processing liquids, and so unprotected and unpassivated AlGaN/GaN HEMTs (from same/similar growth conditions) were also processed and fabricated to provide comparative data. DC measurements were done by contacting the probe needles directly on top of the source (S), drain (D), and gate (G) structures. All measurements were made at room temperature using Agilent's B1500A Semiconductor Parameter Analyzer. Figure 6(a) shows the I_{DS}-V_{DS} characteristics of fabricated unprotected and unpassivated $3\,\mu$m × $100\,\mu$m devices on AlGaN/GaN HEMT structure. Devices made on this material system exhibited good gate control of drain currents up to a gate bias of 1 V and achieved a maximum drain current of ~800 mA/mm. The devices also showed both good pinch-off and good saturation characteristics. On the other hand, devices made on AlN/GaN HEMT structure exhibited very high leakage currents, did not pinchoff, and the drain current was very low as shown in Figure 6(b).

These results, together with the TLM results described in the previous subsection, showed that there were some issues with processing of AlN/GaN HEMT structure which are not seen in AlGaN/GaN HEMTs. Exposure to different processing chemicals such as resist developer and solvents solutions could help reduce the Ohmic contact resistance but at the same time this may have led to the degradation of the quality of the AlN/GaN epilayer structures. Similar observations were made by Fan et al. [11] on the formation of low Ohmic contact on n-GaN materials, where reduced Ohmic contact resistance was caused by the damage of the RIE process employed prior to deposition of the Ohmic contact metallisation. The devices however suffered from surface sensitivity and high leakage currents. It is therefore necessary to protect the AlN/GaN epitaxial layers during device processing.

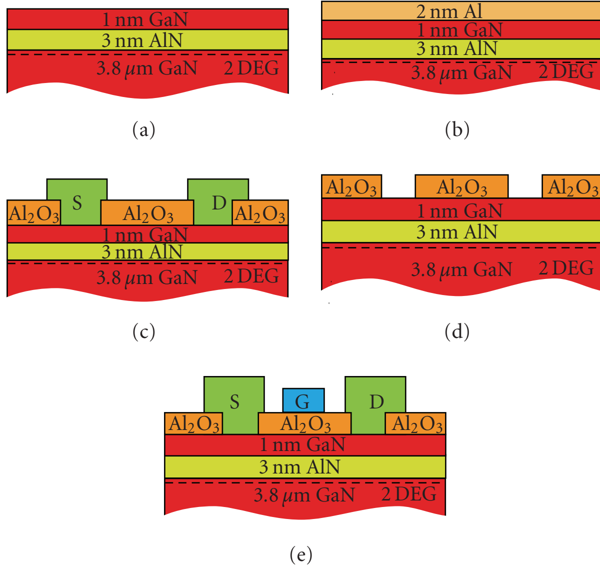


Figure 7: Process flow for fabrication of protected and passivated AlN/GaN MOS-HEMTs using the gate wrap-around technique. Processing includes (a) sample cleaning and deoxidation, (b) 2 nm Al deposition, (c) etching Ohmic regions and thermal oxidation of Al, (d) Ohmic metallisation and annealing, and (e) gate metallisation and device measurements.

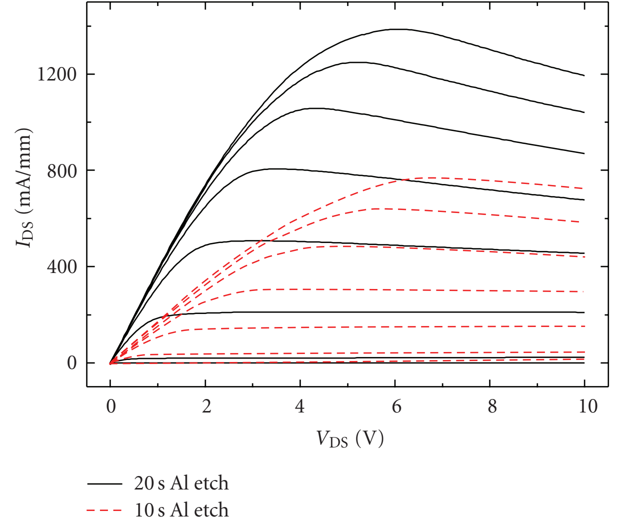


Figure 8: I_{DS} against V_{DS} characteristics of fabricated 3 μm × 100 μm gate AlN/GaN MOS-HEMT devices with different etching times using the simplified gate wrap-around method. The devices are biased from V_{GS} = +3 V to −4 V with step size of 1 V.

A new process for the fabrication AlN/GaN-based devices was therefore developed. It involved employing thermally grown Al_2O_3 for protection of the very sensitive AlN epilayer from exposure to liquid chemicals during processing [6] as earlier described for TLM experiments (Figure 2). This Al_2O_3, which is formed by thermal oxidation of evaporated Al, acts as a surface passivate and as a gate dielectric for the transistors. Figure 7 shows the process flow for fabrication of protected and passivated AlN/GaN MOS-HEMT using the gate wrap-around technique.

To further directly explore the impact of Ohmic contacts optimisation on device performance, devices were fabricated in which the etching time of the Al in Ohmic contact region was varied. Figure 8 shows the typical I_{DS}-V_{DS} characteristics of fabricated 3 μm × 100 μm gate AlN/GaN MOS-HEMT devices with different etching times, 10 secs and 20 secs. It is clear that a 20-sec Al etch has a significant impact on the device performance with the drain current at zero gate voltage (I_{DSS}) more than double that of a device in which the etching time was 10 secs. Compared to similar results for the AlN/GaN HEMT (unprotected and unpassivated device in Figure 6(b)) on the same epilayer structure, these results show that protecting and passivating the AlN/GaN layers during processing yield AlN/GaN MOS-HEMT with far superior and excellent transistor characteristics [6].

2.3. Mesa AlN/GaN MOS-HEMT Optimisation. The developed process technology was extended to realise AlN/GaN MOS-HEMTs using the conventional mesa isolation technique for devices. The process flow is similar to that for the gate wrap-around devices (Figure 7) but with additional mesa isolation and the bond pad steps. Figure 9 shows

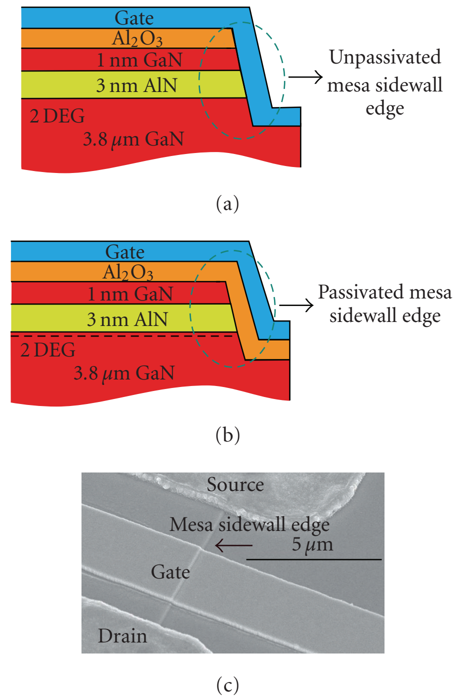


Figure 9: Schematics cross-section of fabricated MOS-HEMT (a) without mesa sidewalls edge passivation, (b) with mesa sidewalls edge passivation, and (c) top-view SEM micrograph of completed two-finger 2.5 μm gate length device.

the schematic cross-section of fabricated MOS-HEMT with (a) unpassivated and (b) passivated mesa sidewalls, respectively. Figure 9(c) shows the topview SEM micrograph of completed two-finger 2.5 μm gate length device.

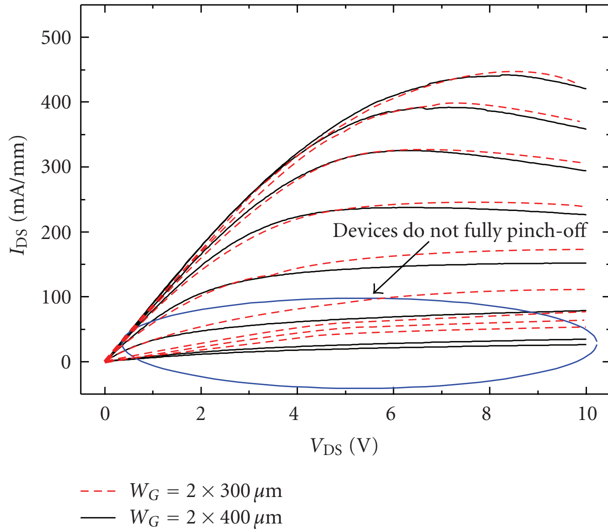
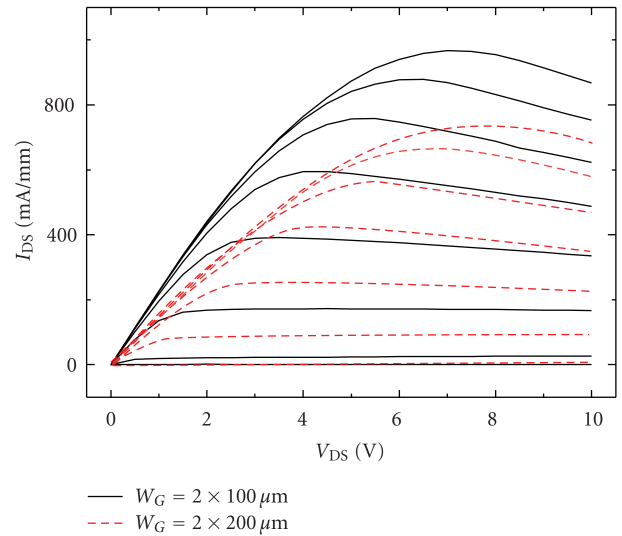
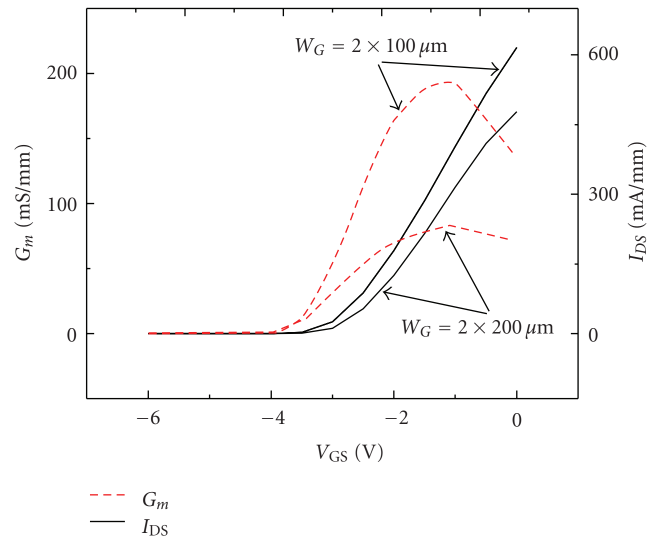


FIGURE 10: I_{DS} against V_{DS} characteristics of fabricated two-finger 3 μm gate length AlN/GaN MOS-HEMT mesa devices with unoptimised etching time (Al etch for 10 secs). The devices had no mesa sidewall passivation and were biased from $V_{GS} = +3$ V to -4 V with a step size of 1 V.



(a)



(b)

FIGURE 11: (a) I_{DS} against V_{DS} and (b) G_m against V_{GS} characteristics of fabricated two-finger 2.5 μm gate length AlN/GaN MOS-HEMT devices with optimised 20 s of etching time with passivated mesa sidewalls. The devices are biased from $V_{GS} = +3$ V to -4 V with step size of 1 V.

3. Characterisation, Results, and Discussion

Initially, mesa devices were fabricated without mesa sidewall passivation and with an unoptimised Ohmic contact process. Figure 10 shows typical I_{DS}-V_{DS} characteristics of a 3 μm gate length AlN/GaN MOS-HEMT device made this way. The devices exhibited high knee voltages (high Ohmic contact resistance) and very high leakage currents. The reason for the high leakage currents seemed to be the contact between the gate metal and the exposed mesa sidewalls edge as illustrated in Figure 9(a). To solve this problem, the devices were passivated with an additional layer of thermally grown Al_2O_3 on the mesa sidewalls edge as shown in Figure 9(b). Significant improvement in the DC characteristics of the fabricated devices using this new process was observed. The measured I_{DS}-V_{DS} characteristics and the device transconductance versus gate voltage are shown in Figure 11. The drain current and transconductance are observed to decrease with gate width. This is attributed to selfheating effects.

The small signal RF performance of this device was also measured (not shown here). A unity current gain cutoff frequency, f_T, and power gain cutoff frequency, f_{MAX}, of 2.8 and 7.9 GHz were obtained for a two-finger 2.5 μm × 100 μm device, respectively, for a device biased at $V_{DS} = 4$ V and $V_{GS} = -1$ V. Devices with gate length of 0.2 μm and 0.5 μm were also fabricated using the processing with mesa sidewalls passivation [17]. Excellent DC and RF performance was observed from the fabricated device as shown in Figure 12. f_T and f_{MAX} of 50 GHz and 40 GHz, respectively, were achieved for the 0.2 μm devices, and of 20 GHz and 30 GHz, respectively, for the 0.5 μm devices. The DC and RF measurements were made at room temperature using the Agilent's B1500A Semiconductor Parameter Analyzer and E8361A PNA Network Analyzer, respectively. Each 10 mm × 10 mm sample had approximately 70 devices, and the variation in device performance on a sample was under 5%. Two different samples from neighbouring parts of a wafer had comparable device characteristics indicating good wafer uniformity and reproducibility of the process.

4. Conclusion

The processing of AlN/GaN-based HEMTs has been described and discussed. The sensitivity of the AlN/GaN epitaxial layer structure necessitated the introduction of special processing requirements and the use of thermally

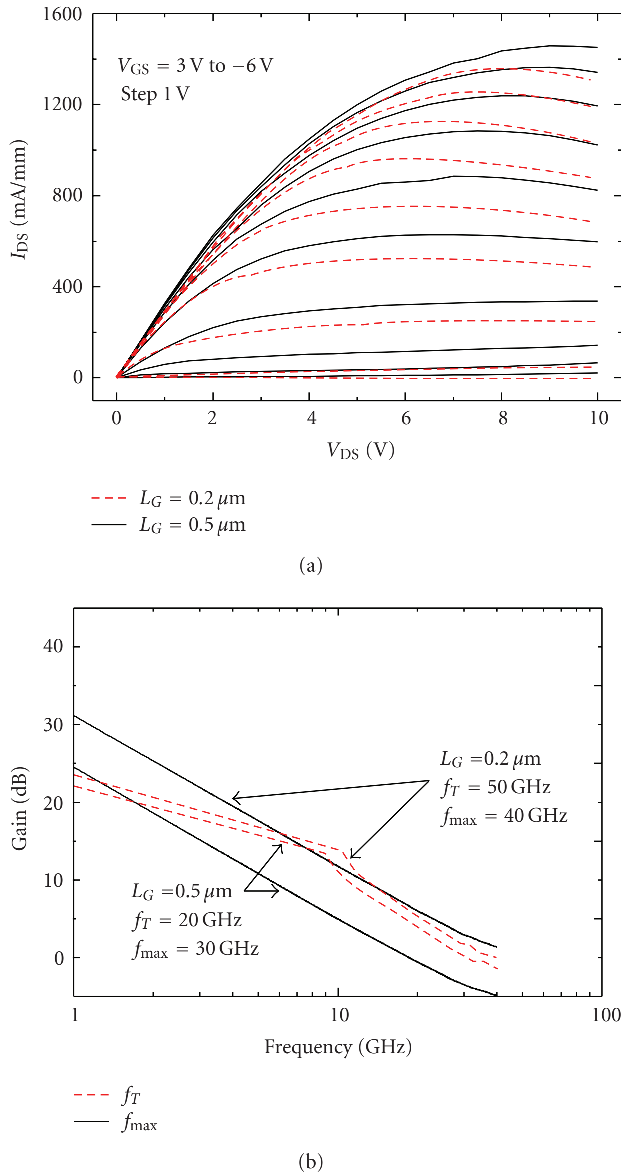


Figure 12: (a) I_{DS} against V_{DS} characteristics of fabricated two-finger 100 μm gate width AlN/GaN MOS-HEMT with gate lengths of 0.2 μm and 0.5 μm, (b) the small-signal RF performances. The devices are biased at $V_{GS} = -2.5$ V and $V_{DS} = 10$ V.

grown Al_2O_3 as a gate dielectric and device passivation. Excellent DC and RF characteristics on AlN/GaN MOS-HEMTs were achieved but further reduction in the Ohmic contact resistance is still required before the full potential of this material system can be realised. The achieved results indicate the potential of AlN/GaN MOS-HEMT technology for high frequency and high power applications.

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