DISTORTION IN SINGLE PHASE CURRENT CONTROLLED PV INVERTERS FOR GRID CONNECTION

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Abstract

Unipolar switched single-phase inverters experience lower switching losses and cause less EMI when compared with bipolar switched inverters. However, these benefits come at the expense of increased distortion in the current waveform near the voltage zero-crossing. Moreover, it is demonstrated in this paper that switching delay causes generation of low frequency harmonics in the current waveform. In spite of that, unipolar switched inverters can be designed to operate within harmonic limits specified by the Australian Standard 4777.2.

1. INTRODUCTION

The conversion efficiency of single-phase, PWM, current controlled inverters can be improved by using unipolar switching [1]. Significant reduction in voltage transitions during switching is also an advantage from the point of view of EMI generation.

The advantages of current control such as active current wave shaping, inherent current limitation, automatic synchronisation with the utility grid and elimination of lower order harmonics has been realised [2]. For simplicity and excellent dynamic performance characteristics the current loop may be based on hysteretic control [3].

It could be postulated that a unipolar switched inverter with hysteretic current control will have all the advantages listed above. But such inverters also have inherent problems that may need attention. These include:

(a) variation in the inverter switching frequency along the AC current waveform [4,5];

(b) increased distortion near the voltage zero crossing [6]; and

(c) generation of low frequency harmonics due to switching delay.

The last one of those problems is the focus of this paper. An analysis of hysteretic switching is carried out for both the unipolar switched inverter and the bipolar switched inverter. The objective of the analysis is to confirm that switching delay causes low frequency distortion in unipolar switched inverters with hysteretic current control.

The paper also explores the question of compliance to Australian Standard 4777.2.

2. INVERTER SYSTEMS

Figure 1 shows a simplified diagram of the inverter voltage control loop (VCL) and current control loop (CCL). The function of the VCL is to keep the DC voltage relatively constant. In doing so, balance between input DC power and output AC power is achieved. Increased insolation level will cause the bulk capacitor voltage v_c to tend to rise. This in turn causes the DC voltage error v_e and AC reference current i_{sref} to increase. The current controller provides switching signals for the inverter switches so that i_p closely follows i_{sref} causing the AC power to rise and match the increased DC power.

Current control may be based on unipolar switching or bipolar switching.

2.1 Unipolar Mode

Hysteretic control with a fixed tolerance band, I_{tol}, is used to force current i_p to track the reference sinusoidal current i_{sref}. The controller forces the bridge into one of four possible states depending on the need to make $|i_p|$ rise or fall and on the polarity of v_s. Whenever $|i_p|$ s falling and reaches the bottom current limit, $|i_p| - 0.5I_{tol}$, $|i_p|$ is made to rise by switching on T_{A+} and T_{B-} if v_s is positive or T_{B+} and T_{A-} if v_s is negative. Due to circuit component imperfections there is a time delay t_d between the instant $|i_p|$ reaches the bottom current limit and the instant the inverter changes state (Figure 2). Whenever $|i_p|$ reaches the top current limit, $|i_p| + 0.5I_{tol}$, $|i_p|$ is made to fall by turning off one of the previously conducting pair of transistors. Again

there is a time delay between the instant $|i_p|$ reaches the top limit and the instant the inverter changes state.

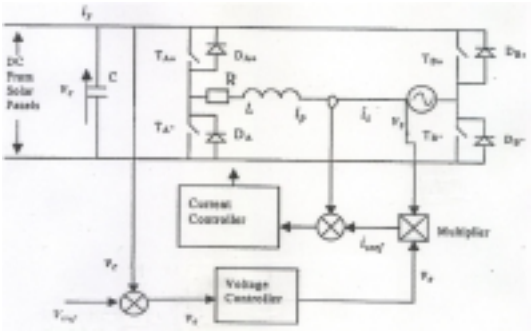
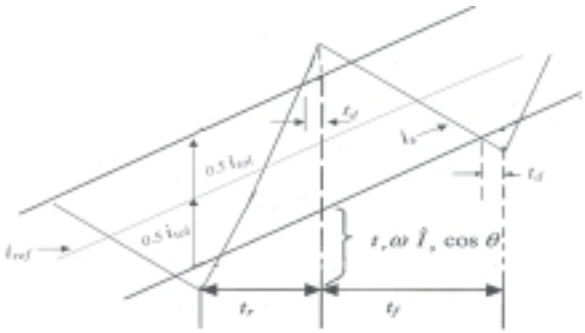


Figure 1: Single-phase grid connected PV inverter system.



(I_s = peak of i_{sref})

Figure. 2: Hysteretic current control

2.2 Bipolar Mode

Figures 1 and 2 are applicable. If we ignore blanking times the inverter operates in one of two states. Transistors T_{A+} and T_{B-} are switched on when current i_s reaches the bottom limit of the tolerance band. Transistors T_{B+} and T_{A-} are switched on when current i_s reaches the top limit. There is a time delay between the instant when i_s reaches a tolerance band limit and the instant the inverter changes state.

3. Low Frequency Distortion

SIMULINK® models were used to simulate unipolar and bipolar switching. Figure 3 shows the unipolar switching model and a similar model was developed for bipolar switching. The inverter switches were assumed to be perfect. An RLC ripple filter was added to filter out switching frequency harmonics (figure 4). The following values were used:

V_s= 240 V; I_{tol} = 0.2 A; V_c = 400 V;

I_{ref} = 4.0 A and 0.5 A; t_d= 2 μs and 8 μs;

C_F= 2 μF; L_1 = 8.0 mH; L_2 = 2.0 mH ; R_c = 5Ω ;

The rationale behind the choice of component values for the filter components is given in reference 5. That filter has practically no effect on low frequency harmonics.

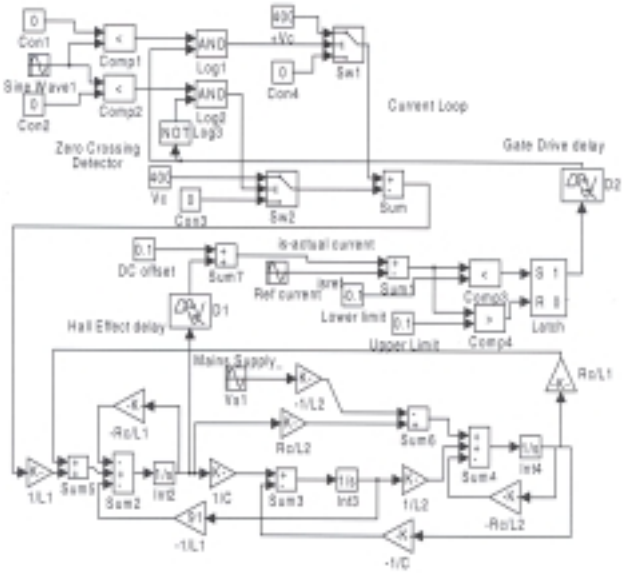


Figure 3 SIMULINK model of the current loop

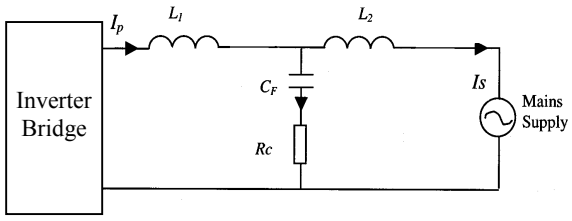
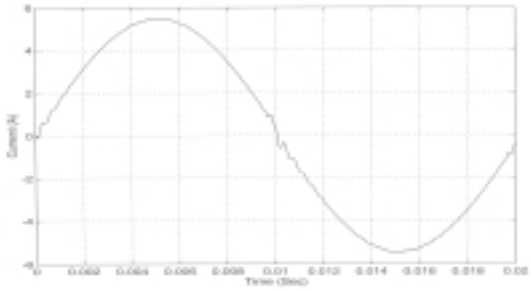


Figure 4: Ripple filter configuration

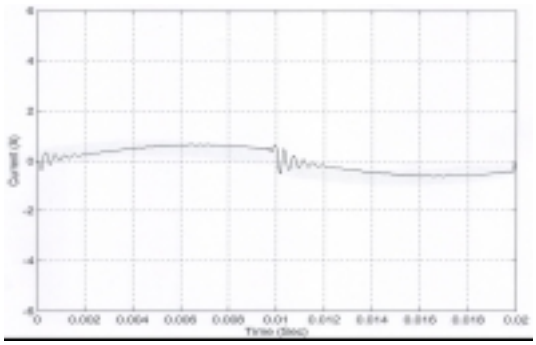
The time delay t_d represents a combination of component delays including current sensor, gate drive and main switching transistor. On grounds of power loss minimisation a Hall effect current sensor is preferred compared to a shunt resistor. However there is usually a need to keep cost down and this means that the quality of the selected Hall effect sensor will be such that it outputs a signal that is delayed. by, typically, a few microseconds compared with the actual current. The above values of t_d have been chosen to reflect this.

Simulation results are shown in figures 5 and 6. Harmonic analysis carried out on the current waveforms reveals significant levels of low frequency harmonics in the output of the unipolar switched inverter, whereas they are practically non-existent in

the case of the bipolar switched inverter (figures 7 and 8).

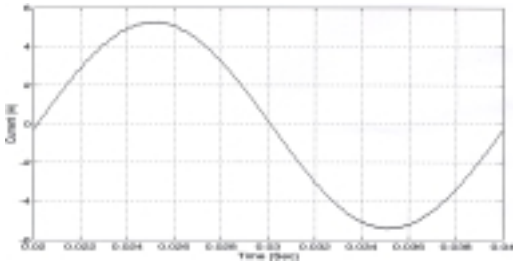


(a) Inverter supplying 4.0 A

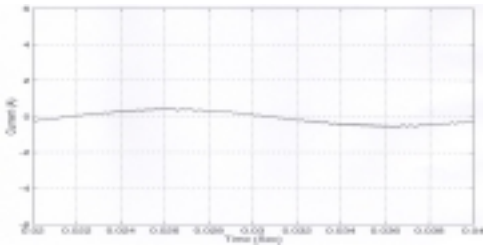


(b) Inverter supplying 0.5 A

Figure 5: Filtered output current from unipolar switched inverter

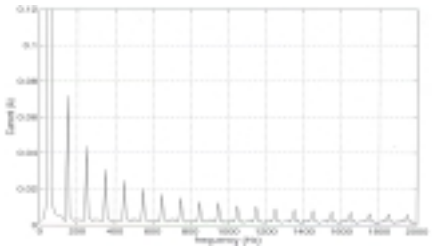


(a) Inverter supplying 4.0 A

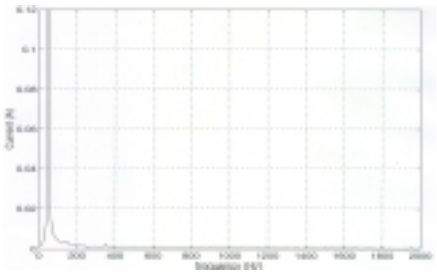


(b) Inverter supplying 0.5 A

Figure 6: Filtered output current from bipolar switched inverter



(a) Unipolar Inverter supplying 0.5 A (td = 8 μs)



(b) Bipolar Inverter supplying 0.5 A (td = 8 μs)

Figure 7: Low Frequency current harmonics

4. Origin of Low Frequency Harmonics

Refer to figure 2. Reference current i_{sref} , the bottom limit of the tolerance band and the top limit of the band are all varying sinusoidally at power frequency. But over the relatively short duration of one inverter switching cycle, they can all be assumed to be straight lines. It is also assumed that *is* rises and falls linearly during a switching cycle. Based on those assumptions, expressions will be derived for i_{av} which represents current i_p averaged over one inverter switching cycle. Current i_{av}, although averaged, is a function of time and may be regarded as current i_p with all the switching frequency harmonics filtered by a ripple filter but with any low frequency harmonic remaining intact.

4.1 Unipolar Switching

During the rise time of i_p we have:

$$L\frac{di_p}{dt} = V_c - \hat{V}_s \sin\theta \qquad (1)$$

Therefore:

$$t_r = \left(LI_{tol} + t_d V_c\right) \Big/ \left(V_c - \hat{V}_s \sin\theta - L\omega \hat{I}_{sref} \cos\theta\right) \qquad (2)$$

Similarly during the current fall-time we have:

$$L\frac{di}{dt} = -\hat{V}_s \sin\theta \tag{3}$$

$$t_f = \left(LI_{tol} + t_d V_c\right) \Big/ \left(\hat{V}_s \sin\theta + L\omega \hat{I}_{sref} \cos\theta\right) \tag{4}$$

The ripple free current i_{av} is given by:

$$\begin{aligned} i_{av}(\theta) = 1/(t_r + t_f)\{[\hat{I}s_{ref} \sin\theta - 0.5I_{tol} - (t_d \hat{V}_s \sin\theta)/L]\ t_r \\ + (V_c - \hat{V}_s \sin\theta)t_r^2/2L - (\hat{V}_s \sin\theta)t_f^2/2L \\ + [\hat{I}_{ref} \sin\theta + 0.5I_{tol} + t_d (V_c - \hat{V}_s \sin\theta)/L]\ t_f\} \end{aligned} \tag{5}$$

The following can be deduced from equation 5:

(a) If switching delay is set to zero, not surprisingly, current i_{av} matches the reference current i_{ref} exactly.
(b) A non-zero switching delay results in i_{av} being higher than i_{ref} for half of the time and lower for the other half (figure 8) signifying the presence of low frequency distortion.
(c) Percentage distortion due to low frequency harmonics is much higher at lower output current (figure 8 (b)).

The fundamental reason for i_{av} being higher than i_{sref} at lower values of v_s is that i_p is driven by a higher voltage, which is v_c- $|v_s|$, when it is rising above the top tolerance limit compared to the voltage, $|v_s|$, that drives i_p when it is falling below the bottom limit. Similarly i_{av} is lower than i_{sref} at higher values of v_s because i_s is driven by a lower voltage, which is V_c- $|v_s|$, when it is rising above the upper tolerance limit and by a higher voltage, $|v_s|$, when it is falling below the bottom limit.

4.2 Bipolar Switching

During the rise time of i_p we have:

$$L\frac{di}{dt} = V_c - \hat{V}_s \sin\theta \tag{6}$$

Therefore:

$$t_r = \left(LI_{tol} + 2t_d V_c\right) \Big/ \left(V_c - \hat{V}_s \sin\theta - L\omega \hat{I}_{ref} \cos\theta\right) \tag{7}$$

Similarly during the current fall-time we have:

$$L\frac{di}{dt} = -V_c - \hat{V}_s \sin\theta \tag{8}$$

$$t_f = \left(LI_{tol} + 2t_d V_c\right) \Big/ \left(V_c + \hat{V}_s \sin\theta + L\omega \hat{I}_{ref} \cos\theta\right) \tag{9}$$

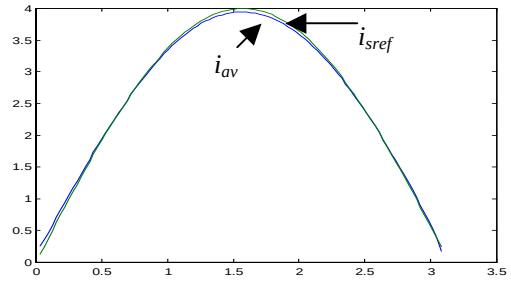
The ripple free current i_{av} is given by:

$$\begin{aligned} i_{av}(\theta) = 1/(t_r + t_f)\{[\hat{I}_{ref} \sin\theta - 0.5I_{tol} - t_d (V_c + \hat{V}_s \sin\theta)/L]\ t_r \\ + (V_c - \hat{V}_s \sin\theta)t_r^2/2L - (V_c + \hat{V}_s \sin\theta)t_f^2/2L \\ + [\hat{I}_{ref} \sin\theta + 0.5I_{tol} + t_d (V_c - \hat{V}_s \sin\theta)/L]\ t_f\} \end{aligned} \tag{10}$$

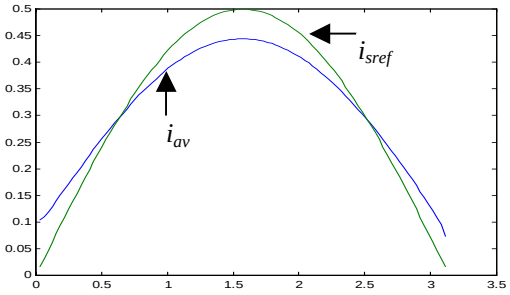
The following can be deduced from equation 10:

(a) As in the unipolar case, if switching delay is set to zero current i_{av} matches the reference current exactly.
(b) Current i_{av} is always lower than i_{sref} with the difference at a given time instant being proportional to the value of i_{sref} at that instant. This signifies that although i_{av} is lower than i_{sref}, there is no harmonic content in i_{av}.
(c) The percentage difference between current i_{av} and current i_s is higher at lower inverter output current (figure 9).

The fundamental reason for i_{av} being lower than i_{sref} is that i_p is driven by a lower voltage, which is V_c- $|v_s|$, when it is rising above the top tolerance limit and by a higher voltage, which is $V_c + |v_s|$, when it is falling below the bottom tolerance limit. The difference between those two voltages is equal to twice v_s, which is sinusoidal. This makes the difference between i_{av} and *is* sinusoidal implying that i_{av} is harmonic free.

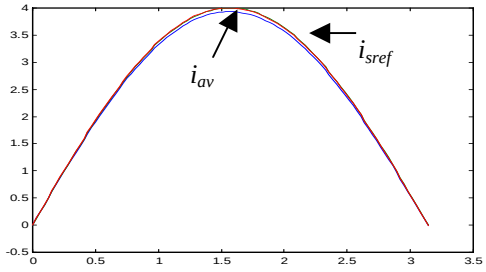


(a) Inverter supply 4.0 A

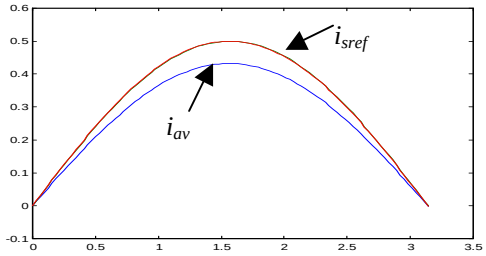


(b) Inverter supply 0.5 A

Figure. 8: Unipolar Switched Inverter: Output Current with Switching Ripple Removed.



(a) Inverter supply 4.0 A



(b) Inverter supply 0.5 A

Figure. 9: Bipolar Switched Inverter: Output Current with Switching Ripple Removed

5. Practical Implications

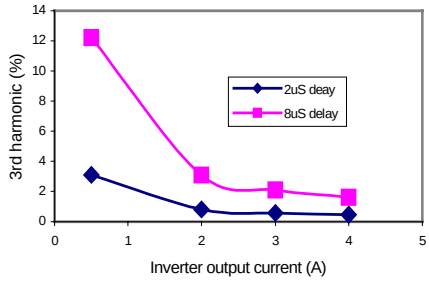


Figure 10: Unipolar: Effect of delay on 3rd harmonics

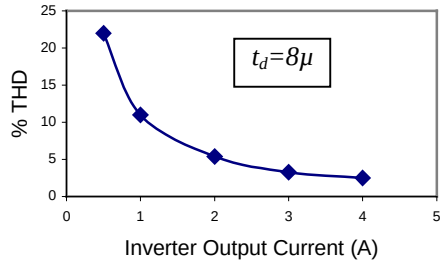


Figure 11: Unipolar: Total harmonics Distortion

An inverter selected for in grid-connected PV applications has to meet the requirements of a relevant standard that specifies distortion limits. In Australia this would be AS4777.2. The question is whether the levels of low frequency harmonics in the output of unipolar inverters fall within the limits specified by the standard. This question is best answered on a case by case basis. For the inverter considered in section 3 above, the third harmonic is the worst one and its levels are shown in figure 10. Total harmonic distortion is shown in figure 11. It has been assumed that non-zero switching delay is the only reason for the generation of low frequency harmonics. The inverter is designed for a rated output of 4 A, therefore it would satisfy the requirements of AS4777.2 even if switching delay is as high as 8 µs. Individual levels for the second to the ninth harmonic should be limited to 4% whereas total harmonic distortion should be limited to 5% [7].

6. CONCLUSION

Switching delay causes low frequency distortion in grid-connected unipolar switched inverters using hysteretic current control. A simple switching model has been used to explain how low frequency harmonics are generated. It has been shown that the unipolar inverter can still be designed to meet the requirements of AS4777.2. In spite of that, methods to reduce the percentage THD at low lower levels are currently being investigated.

7. References

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