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Electron Mobility in Surface and Buried Channel Flatband $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3 Gate Dielectric.

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Abstract—In this paper, we investigate the scaling potential of flatband III-V MOSFETs by comparing the mobility of surface and buried $In_{0.53}Ga_{0.47}As$ channel devices employing an Atomic Layer Deposited (ALD) Al_2O_3 gate dielectric and a delta-doped InGaAs/InAlAs/InP heterostructure.

Peak electron mobilities of 4300 $cm^2/V{\cdot}s$ and 6600 $cm^2/V{\cdot}s$ at a carrier density of 3×10^{12} cm^{-2} for the surface and buried channel structures respectively were determined. In contrast to similarly scaled inversion-channel devices, we find that mobility in surface channel flatband structures does not drop rapidly with electron density, but rather high mobility is maintained up to carrier concentrations around $4x10^{12}$ cm^{-2} before slowly dropping to around 2000 $cm^2/V{\cdot}s$ at $1x10^{13}$ cm^{-2}. We believe these to be world leading metrics for this material system and an important development in informing the III-V MOSFET device architecture selection process for future low power, highly scaled CMOS.

***Index Terms*— InGaAs, MOSFET, ALD, electron mobility**

I. INTRODUCTION

THE continual requirements of the CMOS International Technology Roadmap for Semiconductors [1] for increased performance and density have led to the introduction of myriad non-classical performance boosters such as high-κ metal gate stacks and strained channels, and it is expected that continued EOT scaling will require the SiO_2 interfacial layer to be eliminated [2]. As a consequence, the III-V/high-κ interface has attracted significant interest, initially due to the potential of III-V structures for high electron velocity, evidenced by the high performance achieved in scaled III-V HEMTs [3]. It is now anticipated that III-V MOSFETs may allow higher drive current and transconductance than silicon at its low power scaling limit [4], making them an attractive n-channel solution.

Much recent work [5-8] has focused on the development of inversion-mode III-V nMOSFETs. Such devices, though eminently silicon-like, have not demonstrated the superior transport potential of a heterostructure quantum well, enabled by the epitaxial techniques used in III-V fabrication. Conversely, much work has also been undertaken on the development of buried-channel quantum well nMOSFETs, but their scaling potential remains unclear as a consequence of the inclusion of wide-bandgap layers above the channel [4, 6].

In this letter, we present highly-scaled surface and buried channel flatband nMOSFET structures which maintain mobilities up to 4300 and 6600 $cm^2/V{\cdot}s$ respectively, at electron densities relevant for device operation.

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II. EXPERIMENT

For the buried channel devices, the following layers were grown sequentially by molecular beam epitaxy on 2” semi-insulating (100) InP substrates: a 400 nm $In_{0.52}Al_{0.48}As$ buffer, silicon δ-doping with a density of 3×10^{12} cm^{-2}, a 4 nm $In_{0.52}Al_{0.48}As$ spacer, a 10 nm lattice-matched $In_{0.53}Ga_{0.47}As$ channel, a 2 nm $In_{0.52}Al_{0.48}As$ barrier and a 2 nm $In_{0.53}Ga_{0.47}As$ cap. In the case of the surface channel structure, the upper two layers were omitted. Apart from the δ-doping planes, all layers were nominally undoped. The wafers were then capped *in situ* in the MBE tool using an amorphous arsenic cap to protect the surface from oxidation, loaded into an ALD chamber and the arsenic cap desorbed *in situ* [10]. 60 cycles of Al_2O_3 (approximately 6 nm) were then grown at 270ºC using TMA and H_2O precursors in a TMA-first ALD process [11]. MOSFETs were fabricated in two lithographic steps using a wrap-around gate, obviating the need for device isolation [12]. First, a platinum/gold gate was defined by electron beam lithography (EBL) and liftoff. Non-self-aligned ohmic contacts were then defined by EBL, selective wet etching of the Al_2O_3 in dilute KOH and electron beam evaporation of Ni/Ge/Au-based ohmic contacts. The contacts were alloyed in a 60s RTA process in a nitrogen atmosphere at 280ºC. MOS capacitors were simultaneously defined adjacent to the MOSFETs. The wafers underwent no additional post-

deposition forming gas processing, which has been shown to reduce the interface state density (D_{it}) [13].

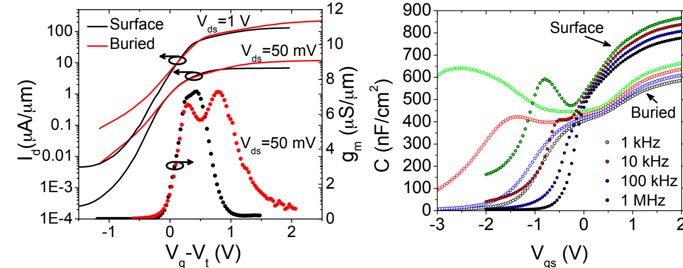

Fig. 1 a) Log I_d,g_m(V_{gs}) measurements of 20 μm gate length devices at V_d=50 mV and 1 V and matched gate overdrive.
b) C-V measurements of 100 μm diameter dots used for mobility extraction.

III. Results and Discussion

Typical log I_d,g_m(V_{gs}) characteristics of surface and buried channel 20 μm gate length devices at V_d = 50 mV and 1 V are shown in Fig. 1. The surface and buried channel devices feature threshold voltages of -0.13 V and -0.87 V respectively. For comparison, transfer characteristics are shown for matched gate overdrive. At 2 V gate overdrive and V_d = 1 V, I_d was 130 μA/μm and 195 μA/μm for the surface and buried channel devices respectively. At V_d = 50 mV, the subthreshold swings of the surface and buried channel devices were 195 mV/dec and 430 mV/dec respectively. Calculating CET at threshold, these equate to approximate D_{it} figures of 7.3×10^{12} cm^{-2} and 1.8×10^{13} cm^{-2} respectively. We believe this difference may be due to the specific bandgap energies and therefore trap distributions swept by the Fermi level at the oxide/semiconductor interface in the two device structures as the gate voltage is varied. Another notable feature in Fig. 1a is the "double-peak" in the g_m(V_g) characteristic of the buried channel device, which we believe reflects charge transfer from the channel to the upper semiconductor layers at higher gate bias. Multi-frequency C-V measurements of 100 μm diameter MOS capacitors are also included in Fig. 1. The measured maximum capacitance scales with CET as expected when considering the additional semiconductor layers in the buried structure.

The surface channel devices featured on-resistances of 3030 Ω·μm and total access resistance of 1140 Ω·μm per side. As a consequence of lower sheet resistance, the buried channel devices had figures of 1160 Ω·μm and 540 Ω·μm respectively.

Effective mobility was extracted as a function of the channel electron concentration using a combination of I-V and C-V measurements. The wrap-around gate process precludes conventional split-CV characterization, hence the mobility is determined by extracting the gate voltage dependent channel carrier density from C-V_g capacitor measurements at 1 MHz and low-field I_{ds}-V_{gs} from an adjacent MOSFET at V_d = 50 mV [12]. The resultant room temperature mobility/carrier concentration data are shown in Fig. 2. Many data, e.g. [5], published for III-V inversion channel mobility include a “correction” for the effect of the interface state density, using simulated capacitance data. It should be noted that we employ no such correction. Also shown for comparison are mobility data from various inversion channel $In_{0.53}Ga_{0.47}As$ MOSFETs [6-8] and Hall data extracted from Van der Pauw structures for both flatband designs.

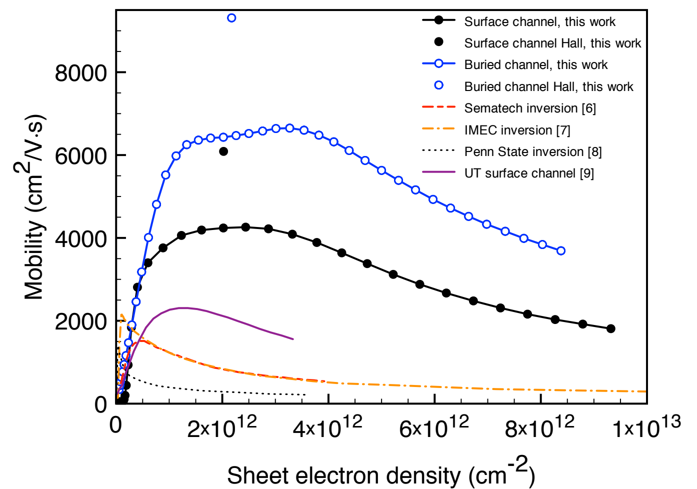

Fig. 2 Mobility of surface and buried channel flatband devices as compared to various ALD/$In_{0.53}Ga_{0.47}As$ inversion mode devices (dashed) from [6-8] and a fully-undoped surface channel quantum well [9]. In contrast to other devices, surface channel flatband devices exhibit high mobility over the complete electron density range, similar to buried channel devices.

The surface channel flatband design exhibits peak mobility of around 4300 cm^2/V·s: significantly lower than the peak mobility of 6600 cm^2/V·s extracted from the buried channel wafer, which may indicate increased roughness at the ALD oxide/channel interface over that of the epitaxial barrier/channel interface in buried channel devices. Extracted Hall mobilities on both structures are notably higher than those from transistor measurements, which may a result of the different extraction techniques, and particularly the contribution of oxide charge to the capacitance. In both cases, however, the carrier concentration dependence of the mobility is notably different from the characteristics of inversion channel $In_{0.53}Ga_{0.47}As$ devices, for which the mobility peaks at low electron concentration, then rapidly decreases with increasing density [6-8]. The mobility from our surface channel devices, in contrast, peaks at around 4300 cm^2/V·s before decreasing with increasing electron density to around 2000 cm^2/V·s at a density of 1×10^{13} cm^{-2}: behavior very similar to our buried channel devices. The only mobility data for surface channel quantum well devices in literature [9] are also included. Although otherwise similar, these devices do not feature delta doping, and their mobility, whilst higher than in an inversion channel, is relatively low and decays rapidly with increasing electron density in comparison to the data reported in this letter. The superior mobility of our devices may be explained by the use of *both* an undoped channel *and* quantum confinement in the presence of delta doping on the backside of the channel.

To explain the high mobility, numerical simulations of the electron populations of our surface channel flatband structure and a theoretical inversion mode device were undertaken, and are found in Fig. 3. Both configurations employ a lattice-matched 10 nm $In_{0.53}Ga_{0.47}As$ channel on an $In_{0.52}Al_{0.48}As$

spacer to provide heterostructure confinement. In the inversion-channel device, the channel is p-doped at 1×10^{17} cm^{-3}. The electron distributions in these two devices are compared for matched electron density in each case.

The mobility of the flatband device below threshold is likely limited by remote impurity scattering from the doping. Above threshold (Fig. 3a), the channel forms towards the back of the quantum well as a consequence of the delta doping, and a high electron density accumulates here initially, screening the dopant. In this region, the mobility is therefore largely unaffected by the oxide interface roughness scattering and dominated rather by that at the heterostructure interface.

As the gate bias is increased, electrons populate the whole channel (Fig. 3b), becoming subject to roughness scattering from both interfaces. Even at high bias (Fig. 3c), however, a significant fraction of the electrons remain at the rear of the channel, where mobility is at its maximum.

In contrast, as the inversion mode device switches on, the channel is formed close to the oxide interface. The p-doped depletion layer exerts a large vertical electric field on the inversion layer charge, which encounters strong oxide interface roughness scattering. The vertical electric field continuously increases with the increase of the channel carrier concentration as gate bias is increased. Consequently, the electron population is always subject to increased interface roughness scattering at the immediate oxide interface as compared to the flatband device.

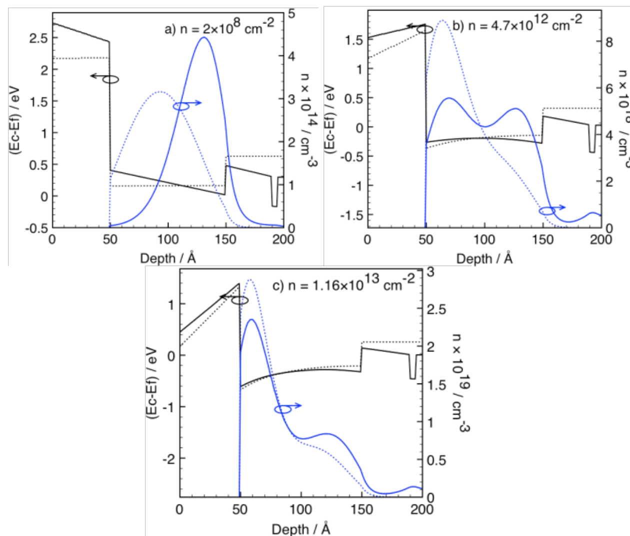

Fig. 3 1-dimensional Poisson-Schrödinger simulations of electron populations of a surface channel flatband device (solid line) and an inversion mode device comprising a 10 nm $In_{0.53}Ga_{0.47}As$ channel (dashed line), compared for matched electron densities. In each case, the flatband device electron density is less constrained to the oxide interface than in the inversion-mode device.

We believe that remote interface roughness and coulomb scattering from the oxide interface limit the mobility in our surface channel structure. In the buried channel, decreased proximity of the charge to the oxide interface further increases mobility. As a result, the vertical field dependence of the interface roughness scattering from the rear spacer interface becomes clearly identifiable at densities of $1\text{-}4\times10^{12}$ cm^{-2}.

IV. Conclusion

The development of the surface channel flatband architecture has enabled the fabrication of well-behaved MOSFETs with mobilities of up to 4300 cm^2/V·s which are sustained at high values up to channel carrier densities of $1\text{x}10^{13}$ cm^{-2}; similar to the characteristics of buried channel devices. This behavior, in contrast to inversion channel devices, arises as a direct consequence of the carrier and vertical electric field distributions in the flatband architecture, and indicates the potential of this materials architecture solution for future low power, highly scaled n-channel CMOS.

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