University of Southern Queensland

Faculty of Engineering and Surveying

Modelling Load Balancing Type Static Var Compensator Control System Response

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Abstract

As power system interconnection becomes more prevalent, there has been an increase in use of thyristor controlled shunt connected compensation devices for dynamic power system compensation and power transmission capacity increase. A Static Var Compensator (SVC) functions as a variable reactance capable of operating in both the inductive and capacitive region as required on a cycle by cycle basis to provide compensation at the point of connection to the power system.

Voltage regulation is the operational objective of most SVCs. Therefore, transient response of SVC control systems impacts overall power system performance and inappropriate settings may lead to voltage instability. SVCs are also commonly used to convert single phase load into balanced three phase load, thereby reducing negative phase sequence voltages and currents within the power transmission system. As most load balancing SVCs are consistently operated to their capacity, removal from service to apply and test control system setting changes impacts system regulation and stability. Therefore, model development of a load balancing type SVC control system to predict response to setting changes may provide an alternative to lengthy outages of SVC plant.

This paper examines the theoretical basis of thyristor controlled shunt compensation, establishing conditions for voltage support and unbalanced load compensation. Load balancing type SVC control system model development and validation is documented.

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Glossary

AC	Alternating current, a sinusoidal waveform of constant frequency.
Ampere (A)	The SI unit of current, defined the amount of current produced by an electromotive force of 1 V across a resistance of 1 Ω.
Bus	High capacity conductor used at substations for transfer and distribution of current. It is usually a hollow copper or aluminium pipe.
Coulomb	The SI unit of charge (Q), defined as the flow of 1 A for one second.
Current Transformer	A transformer with short circuited secondaries used to proportionally reproduce primary current at a level suitable for input to protection, control and measurement circuits.
Filter	A passive compensation device comprising a combination of resistance, inductance and capacitance to suppress a specific power system attribute such as harmonics.
NEC	National Electricity Code.
NEMMCO	National Electricity Market Management Company.
NPS	Negative phase sequence.
NSC	Network Switching Centre – the network operational branch of Powerlink Queensland responsible for authorising and managing access to plant connected to the extra-high voltage transmission system.
Per unit	A method of expressing a quantity as a fraction of a nominated reference value such as a system voltage, allowing easy quantity comparison. Abbreviated as ‘pu’.

Reactance	A measure of component resistance to alternating current as a function of frequency.
Reactor	A passive power compensation device comprised of inductor coils.
Susceptance	A measure defining the ease of transmission of alternating current through a circuit, with zero indicating an open circuit and infinity indicating a short circuit or no impediment to transmission of AC. Susceptance is the inverse of reactance.
SVC	Static Var Compensator.
TCR	Thyristor Controlled Reactor.
Thyristor	a power electronic device of high voltage rating that acts as a switch to allow the flow of current through a circuit when a firing pulse, or ‘on’ signal, is received.
Traction Load	Single phase high voltage load produced by electric trains.
Transmission delay	The actual delay between the generation and arrival of an analog or digital signal.
TSC	Thyristor Switched Capacitor.
Var	Volt-Ampere reactive, a measure of power consumed by devices that have reactance.
Voltage Transformer	A transformer used to proportionally reduce system voltage to a measurable level, suitable for input to control or protection circuits.
Watt	A measure of power consumed by devices that have resistance.

Nomenclature

The following symbols and representations are used throughout the document:

Table 1: Commonly used symbols and representations.

Symbol	Interpretation	Units
V	Voltage, SI unit is the Volt.	V
I	Current, SI unit is the Ampere.	A
U	Voltage (Asea and ABB convention)	V
R	Resistance, SI unit is the Ohm.	Ω
C	Capacitance, SI unit is the Farad.	F
L	Inductance, SI unit is the Henry.	H
X	Reactance, SI unit is the Ohm.	Ω
B	Susceptance, SI unit is the Siemen.	S
∅	Phase	
	Resistor	
	Inductor	
	Capacitor	
	Thyristor	

The following naming conventions are used throughout the document:

A, B, C: Identify primary 50 Hz power system phase voltages and currents, where all phases are nominally separated by 120 electrical degrees.

R, S, T: Identify phase voltages and currents referred to the secondary side of an SVC, corresponding to A, B and C phase respectively of the primary system. These quantities are phase shifted according to the vector group of the transformer.

B_{AB} : Indicates a susceptance delta connected between A and B phases of the power system. A subscript of BC indicates connection between B and C phases, and subscript CA connection between C and A phases. Likewise, RS represents connection between A and B phases referred to the secondary side of the SVC transformer.

TP1: Identifies test point 1 on an ASEA abridged schematic. TP2 indicates test point 2 and so on.

1. Introduction

1.1 Background

On the fourth of November 2004, a prolonged voltage dip was experienced at Blackwater 132kV Substation located in Central Queensland. The voltage fluctuation corresponded to a decrease of 6% of nominal voltage (132kV) for approximately 9 minutes as indicated in Figure 1.1. Events of this type affecting Power Quality are of concern as failure to comply with regulatory limits for voltage magnitude, balance and frequency results in penalties by regulatory authorities such as the National Electricity Market Management Company (NEMMCO) and possible litigation by industrial customers adversely affected by such failures.

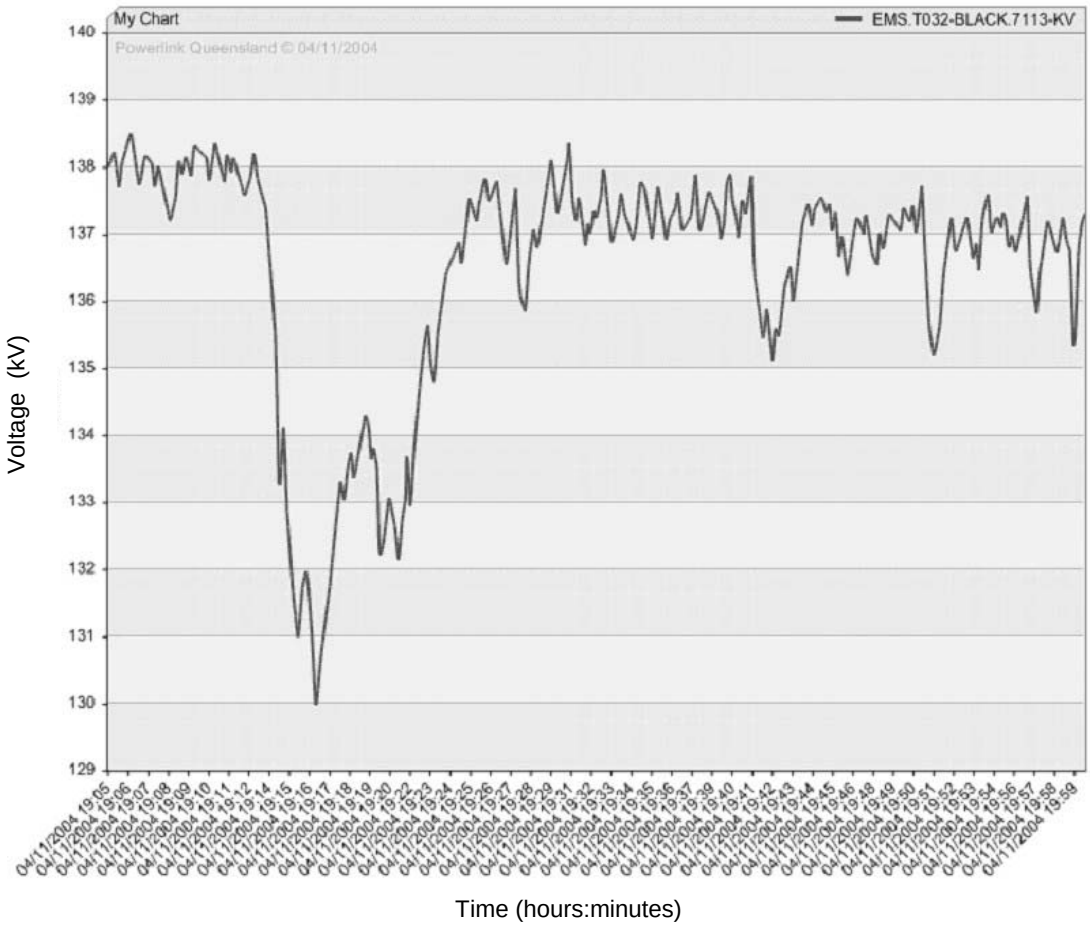

Figure 1.1: Blackwater 132kV Bus Voltage (Jones, R 2005, pers. comm., 22 March)

Blackwater substation voltage levels are regulated by a device called a Static Var Compensator (SVC). Immediately prior to the voltage dip the SVC was providing transmission system voltage support, operating in capacitive mode. As shown by the voltage and load graph Figure B.1 (Appendix B), the SVC transformer T5 exhibited an increase in real and reactive power (Vars) during the voltage dip, while the SVC operating region shifted from capacitive mode to inductive mode, as negative Vars correspond to inductive SVC operation. Concurrently with the voltage dip, Negative Phase Sequence (NPS) voltage levels displayed no clear trend as shown by Figure B.2 (Appendix B), indicating no appreciable variation in unbalanced loading.

In the months previous to this event, the Static Var Compensator (SVC) voltage support and load balancing system at Blackwater substation was observed to intermittently malfunction, either failing to support voltage or causing voltage dips for short durations. At the time of these events no obvious explanation was found as the loading magnitude and type was deemed insufficient to cause such an event.

Theoretical analysis performed by Powerlink Queensland utilising available power system models failed to identify probable cause for this voltage instability. However results indicated that the SVC is not providing compensation as designed, particularly the susceptance presented by the SVC to the power system appears to intermittently deviate from optimal values resulting in voltage fluctuations (Jones, R 2005, pers. comm. 22 March).

A requirement to investigate and rectify the cause of this apparent control system malfunction was identified. Investigation of SVC control system malfunction requires some method of theoretical modelling of the control algorithms to identify deviations of control system response from design. As the SVC in question is a specialized load balancing compensator, modelling packages for this purpose are not commercially available and a specific modelling method must be developed for detailed analysis.

One such specific model does exist, developed by Mr. Paul Windle of Powerlink Queensland, although developed for academic purposes and for an alternate SVC rating. Therefore, it is proposed that the existing model be adapted for this purpose and site, and the results obtained compared with experimental results obtained from the actual SVC control to verify the validity of the model output. As the SVC to be investigated has a primary purpose of load balancing, control system response to voltage imbalance shall specifically be modelled.

1.2 Project Objectives

It is proposed that the project fulfil the following objectives:

1. To evaluate the regulatory and operational requirements for voltage regulation and load balancing of power systems;
2. Analyse causes and impact of voltage imbalance and resultant Negative Phase Sequence voltages on high voltage plant and power system operation;
3. Research information on Static Var Compensation control system operation and its overall effect on power systems;
4. Critically evaluate mechanisms by which Static Var Compensation systems achieve voltage regulation, load balancing and minimisation of Negative Phase Sequence voltages;
5. Develop or adapt a model to simulate the action of a load balancing type SVC system in MATLAB (Simulink) based on information obtained from manufacturer's documentation and component measurements;
6. Simulate model response to voltage imbalance utilising step load imbalance to simulate worst case conditions;
7. Measure actual SVC control system signals and record response to power system voltage or load imbalances;
8. Determine if the developed model is acceptable by comparison of predicted responses with measured values and thus validate or otherwise the assumptions made;
9. Write a report documenting the development, adaptation and validation of the control system model;

And as time permits:

10. Determine if any power system conditions exist where the dynamic response of the Static Var Compensator may cause instability.

1.3 Brief Introduction to Theory

1.3.1 Impact of Power System Interconnection

Power supply systems comprise three broad categories – generation, transmission and distribution. Electricity is generated at power stations from various natural resources such as coal, natural gas, hydro and wind, in large quantities where economies of scale can be achieved (ESAA p6). These generating stations are proximate to the fuel resource, often a considerable distance from major load centres. Therefore, large quantities of electricity are transported at high voltages via the transmission network to strategically located bulk supply substations, and from there to smaller substations where the supply is further reduced for distribution as illustrated in Figure 1.2. Power generation from other states may also be linked via interconnectors, linking the transmission systems (ESAA p8).

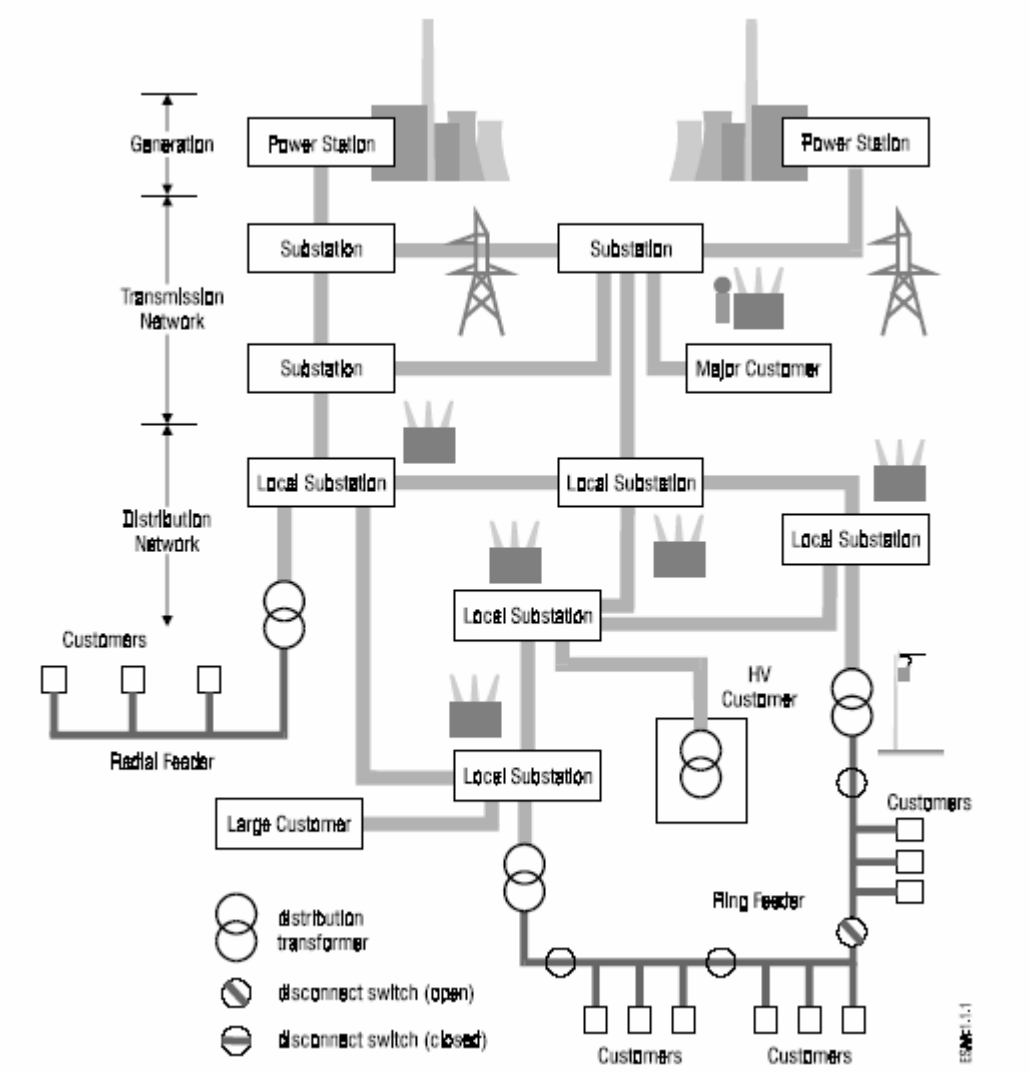

Figure 1.2: Electrical Power Supply System Interconnection (ESAA 2002, p. 5)

Modern power supply systems have evolved from separated utilities to large interconnected systems, with many generating stations and load centres being interconnected through power transmission lines. Traditionally power generation supplied local load via smaller systems operated at lower voltage levels. With the high degree of system interconnection, there is increased power exchange over larger distances at higher system voltage levels (Ghosh & Ledwich 2002, p. 4). Interconnection allows participating parties to share benefits such as power generation optimization, utilization of differences in load profiles, competition and pooling of reserve capacity (ESAA 2002, p. 8).

Operation and expansion of power systems impacts society and several factors must be considered. Technical and economic factors concern the improvement of existing equipment and design of new equipment which could offer economies. Social and demographic factors deal with the tendency of the power industry to influence social and political processes, including siting of industrial enterprises and distribution of working population (Ghosh & Ledwich 2002, p. 4). Environmental factors are concerned with the effects of the power industry upon the environment.

These concerns have resulted in the emergence of distributed generation, the current trend of interconnected smaller sized generating units such as Kogan Creek gas fired power station as opposed to the traditional coal fired large capacity stations such as Tarong and Stanwell. This trend is emerging as a consequence of increased Greenhouse gas issue significance, leading to consideration of alternate energy sources such as solar, wind and wave that operate with smaller sized generation units. These smaller units are also less complex, less expensive and more rapidly constructed, allowing more rapid adaptation to the requirements of expanding industries (Ghosh & Ledwich 2002, p. 4). Therefore, interconnection of power systems yields technical, economical and environmental benefits, as excess capacity generated by hydro resources from one region may augment load supplied by fossil-fuelled generation in another.

For interconnections to operate as intended, transmission systems must have adequate capacity or load rating to transmit the quantity of power intended. If the existing transmission system does not have adequate ratings for the predicted power transfer, additional lines may be constructed in parallel with existing transmission lines, or the transmission system may be upgraded to a higher operating voltage (Ghosh & Ledwich 2002, p. 5). This is not always possible due to environmental, economic and time factors, and public opinion.

In an electrical power system, Vars (Volt-Amperes reactive or reactive power) are generated by lightly loaded lines and cables, and absorbed by transformers and heavily loaded lines. This reactive power decreases the useable power delivered to a load as shown in Figure 1.3. Power transfer limitations may be experienced due to reactive power imbalances, often limiting the transfer capacity of parallel transmission lines. Uncontrolled flow of Vars in transmission networks can lead to system stability and overvoltage problems while the rapidly varying Var demand of certain types of industrial load such as mining loads can produce unacceptable voltage fluctuations (Ghosh & Ledwich 2002, p. 7).

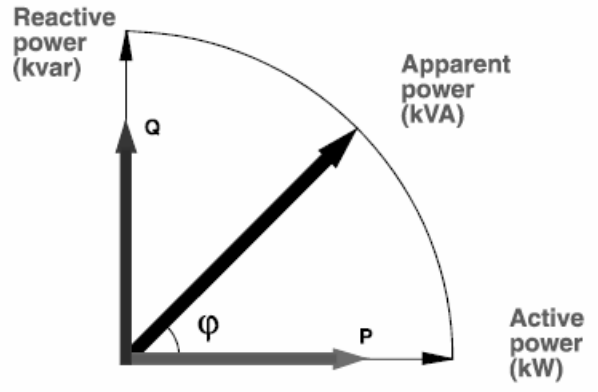

Figure 1.3: Relationship between Active, Apparent and Reactive Power (ABB 1999a).

These problems have greater impact on reliable and secure power supply in modern power supply systems due to globalisation, privatisation and energy transfer requirements (Ghosh & Ledwich 2002, p. 6). It is therefore essential to balance the supply and demand of active and reactive power in an electrical power system. If this balance is lost, system frequency and voltage excursions may occur with a worst case result of power system collapse.

1.3.2 Power Quality

Power supply systems are intended to deliver near sinusoidal voltage of rated magnitude at the stipulated 50Hz frequency fundamental. The power supply to a customer should also be reliable, that is, uninterrupted. However, the actual energy received differs from these ideal specifications dependent on factors such as climatic conditions, system load and generational changes and the occurrence of contingencies. The degree to which the actual power received conforms to specifications and standards is referred to as power quality.

Deterioration of the supply quality affects customer power demand and may result in reduced machinery efficiency, electronics service life and manufacturing quality. Customers connected on a feeder also supplying a large motor may experience severe dips in voltage when motor load is switched on. This may adversely impact sensitive loads such as hospitals, financial institutions, airports and industrial processes (ESAA 2002, p.2). Supply voltage disturbances to industrial customers may cause significant financial losses as short duration voltage dips or interruptions are often sufficient to drop out motor drive contactors and thus interrupt manufacturing processes. This may require restarting of processes or destroy entire product batches such as in semiconductor manufacture. With the current trend toward litigation this can prove very costly to the supply authority if held accountable.

Customer awareness of power quality issues has increased in recent years, with rise in power quality impact attributed to modern technology such as computers, power electronics and controls sensitive to variations and disturbances in the electricity supply previously unnoticed. As transmission services are provided under contract, restrictions on allowable voltage and current distortion, deviation and fluctuations are imposed by regulatory authorities such as the NEMMCO.

Distribution systems are where power quality issues are commonly identified. However, transmission systems also impact on the quality of power as modern transmission systems have a low resistance to reactance ratio, resulting in low system damping. Therefore, system disturbances may oscillate for a considerable time before decaying (Ghosh & Ledwich 2002, p. 6).

Transmission of power over longer distances is at higher voltages to reduce line losses, although some losses will be experienced due to corona and line energising current. These transmission lines are usually metallic structures, open to the environment and thus exposed to hazards such as storms and lightning strikes which may cause voltage spikes.

Throughout the generation, transmission and distribution networks there are factors influencing reliability and quality of power supply. Deterioration in Power Quality may be attributed to:

- Natural Causes: faults or lightning strikes on transmission lines or distribution feeders, falling of trees or branches on distribution feeders during storm conditions or equipment failure, or;
- Man-made causes: load, capacitor or feeder switching, transformer energisation, power electronic loads such as uninterruptible power supply (UPS), variable speed drives and converters, arc furnaces and induction heating systems.

Factors which affect supply quality include voltage regulation, supply frequency, voltage transients, imbalance, DC current injection, power factor, harmonic distortion and flicker.

Voltage Regulation is the maintenance of voltage within an acceptable range at the point of delivery to the customer. Regulatory authorities can impose sanctions on utilities for providing customers with out-of-range voltages (ESAA 2002, p. 42). Sustained overvoltage may cause equipment failure and insulation stress and sustained undervoltage can cause motors to stall. Voltage variations may be of short or long duration.

Any variation in the supply voltage for duration not exceeding one minute is called a short duration voltage variation (ESAA 2002, p. 43). These variations are further classified as voltage sags, voltage swells and spikes shown in Figure 1.4.

Voltage sag is a short duration decrease in supply lasting between 5 cycles to a minute, typically caused by system faults or energisation of heavy loads. Voltage may fall between a few percent below lower nominal limit to as much as 100%, although the duration is not long enough to be classed as an interruption. Most voltage sags do not exceed a 20% drop from nominal and usually persist for half a second or less (ESAA 2002, p. 43).

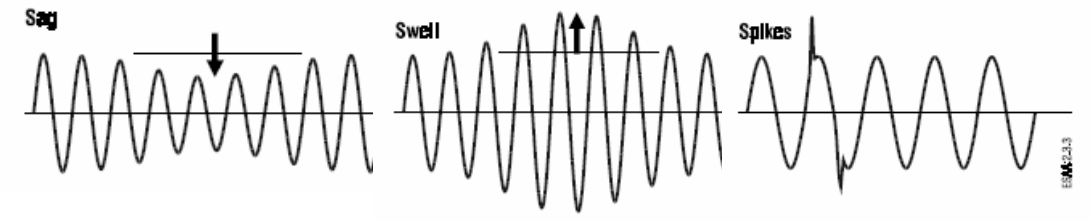

Figure 1.4: Short Duration Voltage Disturbances (ESAA 2002, p. 44)

Voltage swells are defined as increase of fundamental frequency voltage for a short duration lasting from milliseconds to a second, and spikes are very high magnitude voltage impulses lasting microseconds (Ghosh & Ledwich 2002, p. 8). Swells do not occur as commonly as sags, but might occur due to temporary voltage rise of an unfaulted phase during system earth faults.

Long duration voltage variations are any variation in the supply voltage for duration exceeding one minute and have greater impact on customers than short duration variations. These variations are further classified as overvoltages, undervoltages and sustained interruptions (ESAA 2002, p. 43).

An overvoltage or undervoltage is a 10% or more increase or decrease in RMS voltage for a long duration. Switching off large loads or capacitor bank energisation may result in system overvoltage if voltage regulation is poor. The limits defined by the National Electricity Code (NEC) as to the percentage and duration of overvoltage events are displayed in Figure 1.5.

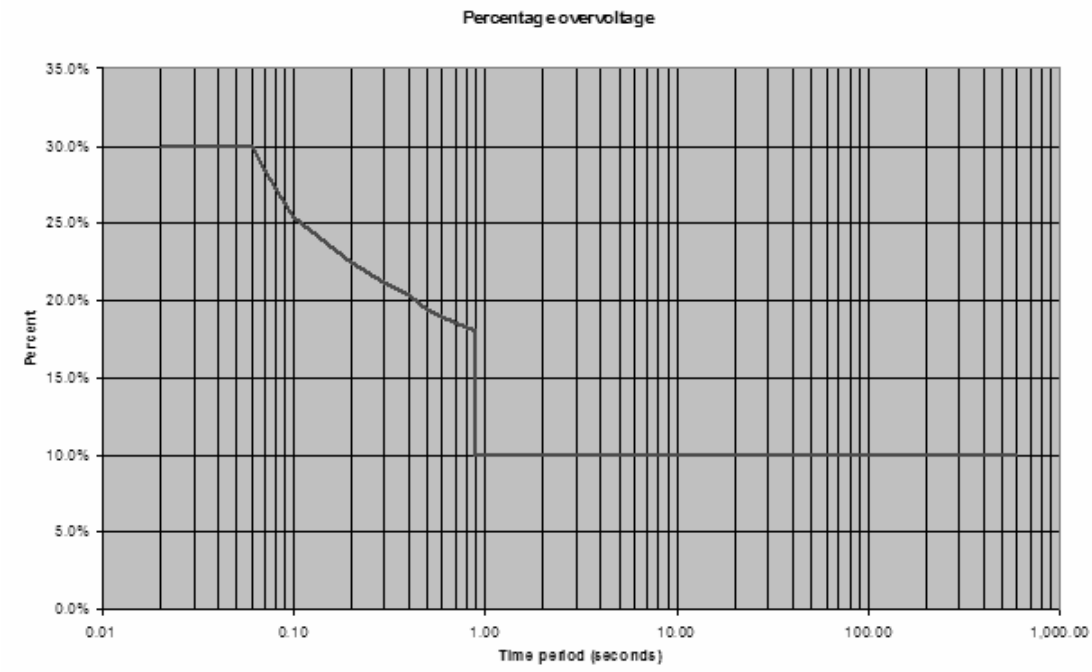

Figure 1.5: Sustained System Overvoltage Limits (NEC 2002, p. 50)

An undervoltage is the result of an event opposite in nature such as reactor energisation and a sustained undervoltage is referred to as a brownout. When supply voltage is zero for period of time in excess of 1 minute it is referred to as a sustained interruption (ESAA 2002, p. 43).

Supply frequency is the power quality aspect most easily altered and the factor most likely to have widespread impact. Frequency is the rate at which voltage alternates, generally maintained to within ±0.2% of the nominal 50 Hz. Control of frequency is a function of the generation process, determined by the speed at which the generators spin and in turn, determining motor rotational speed. Large load increases act to slow generators, decreasing frequency (ESAA 2002, p. 45). Any significant decrease in system loading allows generators to increase speed, resulting in increased system frequency.

These load changes can occur anywhere on the transmission or distribution system and rapid load changes will cause system frequency disturbances. However major events such as system contingencies or very large load loss may alter system frequency by a significant amount, referred to as an excursion. This may cause alternate speed variations of system generators, and thus of system frequency, as the generators create power oscillations known as 'power swings' (ESAA 2002, p. 45). If these oscillations are not quickly damped, synchronism and thus stability may be lost. Sustained operation outside tolerable frequency limits may result in reduced life span of generator turbine blades (Sen 1997, p. 117). If frequency falls below a certain threshold, underfrequency protection relays may trip to protect turbine blades. Certain time limits are defined and enforced by NEMMCO for restoration of system frequency to acceptable values as indicated in Table 1.1.

Table 1.1: Frequency Excursions and Restoration times (ESAA 2002, p. 46)

Event	**Range**	**Frequency (Hz)**	**Restoration Time**
	Normal	49.90 – 50.10	
Large Load Change	Normal Excursion	49.75 – 50.25	To Normal within 5 minutes
Loss of single generator unit	Frequency Tolerance	49.50 – 50.50	To Normal within 5 minutes
Single contingency	Frequency Contingency	49.00 – 51.00	To Frequency Tolerance within 1 minute, then Normal within 5 minutes
Multiple contingencies	Multiple Contingency	47.00 – 52.00	To Frequency Tolerance within 1 minute, then Normal within 10 minutes

Voltage transients are waveform components that disappear during transition from one steady-state operating condition to another (ESAA 2002, p. 43). These may be classified as impulsive or oscillatory transients. An impulsive transient is a fast rise and decay time non-power frequency change in voltage or current, mainly caused by lightning strikes (Ghosh & Ledwich 2002, p. 13). Oscillatory transients have one or more sinusoidal components multiplied by a decaying term and caused by capacitor or transformer energisation, ferroresonance and converter switching.

Voltage imbalance is a condition in which the three phases of supply are not equal in magnitude and 120 ° separation between phases is not maintained. This supply imbalance can cause temperature rise, deterioration of insulation, de-rating of motors and large motor thermal trips (ESAA 2002, p. 46). For high voltage networks, this voltage imbalance is limited to 3% variation between highest and lowest phase magnitudes (Standards Australia 1991b, p. 5).

The primary cause of voltage unbalance is single phase loads in three phase circuits, with severe imbalance resulting during single phasing conditions (Ghosh & Ledwich 2002, p. 14). Unbalanced loading in three phase systems produces unequal currents generating Negative Phase Sequence (NPS) voltages. The magnitude of NPS voltage allowable is limited by electrical utilities due to the increased heating caused in three phase motors and generators. Australian Standard AS1359 (1997) specifies that 3-phase induction machines should be designed for continuous voltage unbalance levels of 1.0%. For induction motors, the positive phase sequence voltage components create positive torque that does useful work. The negative phase sequence voltage creates a flux rotating opposite to the rotor at almost twice the supply frequency, creating negative torque, increased current flow and consequential heating.

NPS voltage is defined in terms of the fundamental phase to neutral voltage phasors V_a, V_b and V_c as:

$$V_{NPS} = \frac{\left(V_a + a^2 V_b + a.V_c\right)}{\sqrt{3}} \quad \text{where;} \quad a = e^{j120^\circ} \qquad (1.1)$$

(Standards Australia 1997, p. 4).

In balanced systems this phasor summation forms a closed triangle, giving $V_{NPS}=0$.

Direct Current (DC) injection is a situation that may cause saturation and heating of transformers and motors, and generation of excessive harmonic currents (ESAA 2002, p. 42). There are two main implications of DC current in an electricity supply system. DC current may bias the sinusoidal flux of a transformer core, positively offsetting transformer flux waveforms with the positive half cycle becoming heavily saturated while the negative half cycle remains within linear range. The increased flux peak value may result in transformer magnetic core saturation and heating due to excessive magnetising current and core losses (Ghosh & Ledwich 2002, p. 16). The other implication is that the DC current return path usually involves flowing through earth. This may involve DC current passing through subterranean metallic structures and the consequential acceleration of corrosion, possibly resulting in unsafe operating conditions if the earthing system is damaged.

Poor power factor causes unnecessary power loss. Consider a feeder supplying an inductive load, with current denoted by I_s and load voltage by V_L. If the load power factor $\cos\ \theta_L$ is lagging, the system phasor diagram may be represented as below in Figure 1.6.

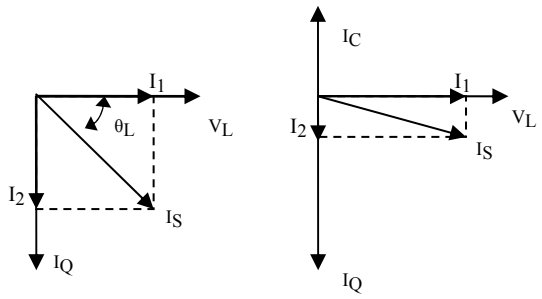

Figure 1.6: Power factor and corrected power factor

Load current I_s is resolved into a real part $I_1 = |I_s| \cos\ \theta_L$, and a reactive part $I_2 = |I_s| \sin\ \theta_L$. Actual work done depends on real power and thus the reactive power is wasted. If the load power factor is small, then the reactive current component is large, resulting in significant voltage drop. Optimally, feeders should be operated near unity power factor (ESAA 2002, p. 47).

Power factor correction is achieved by connecting capacitance in parallel with the load, drawing current I_c in phase opposition to I_Q. The resultant current drawn by capacitor load combination is I_s indicated in the second diagram of Figure 1.6. The real component of current remains constant but the reactive component of current has reduced considerably. The magnitude of feeder current and the associated power factor angle have both decreased.

Harmonic Distortions are caused by the injection of currents having frequency components which are multiples of the fundamental frequency, resulting from equipment drawing non-sinusoidal current from the supply. Power electronic loads such as uninterruptible power supplies (UPS), converters and adjustable speed drives usually cause harmonics in power systems, in addition to draglines, arc furnaces and fluorescent lighting. A measure of harmonic content is the total harmonic distortion (THD). For quality power it is recommended that THD be less than 3% (Standards Australia 1991a, p. 3).

Notching is a periodic voltage distortion due to the operation of power electronic converters where current commutates from one phase to another due to finite supply inductance (Ghosh & Ledwich 2002, p. 18). During this period there is a momentary short circuit between the two phases that distorts voltages as shown in Figure 1.7. The maximum voltage during notches depends on the system impedance. The frequency components associated with notches are usually very high.

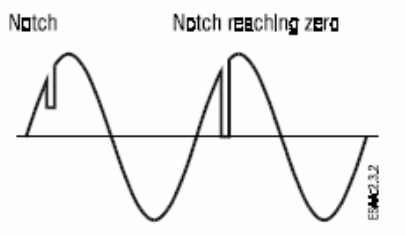

Figure 1.7: Voltage Notching (ESAA 2002, p. 50)

Analysis of harmonic distortions indicate that they are composed of a number of pure sine waves of various magnitudes and frequencies that are integer multiples (harmonics) of the fundamental frequency (50 Hz) as indicated in Figure 1.8.

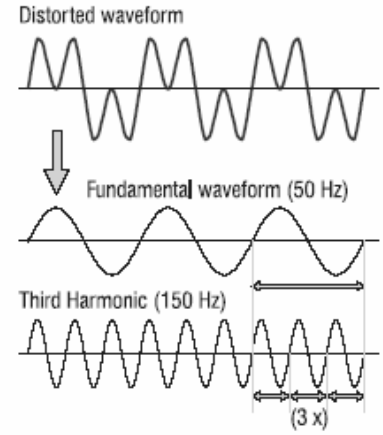

Figure 1.8: Power System harmonics (ESAA 2002, p. 48)

Flicker is rapid voltage fluctuations causing unacceptable variations in lighting levels, often very annoying to the human eye. Flicker is mainly caused by rapid current magnitude variations of loads such as arc furnaces when initial arc strike produces large inrush currents, causing a dip in the supply voltage (Ghosh & Ledwich 2002, p. 19).

Table 1.2: Power Quality Categories and Causes (Ghosh & Ledwich 2002, p. 5)

Category		**Characterisation**	**Typical Causes**
Transients	Impulsive	Peak magnitude, rise time and duration	Lightning strike, transformer energisation. Capacitor switching
	Oscillatory	Peak magnitude, frequency components	Line, capacitor or load switching
Short duration voltage variation	Sag	Magnitude, duration	Ferroresonant transformers, single line-to-ground faults
	Swell	Magnitude, duration	Ferroresonant transformers, single line-to-ground faults
	Interruption	Duration	Temporary (self clearing) faults
Long duration voltage variation	Undervoltage	Magnitude, duration	Switching on loads, capacitor de-energisation
	Overvoltage	Magnitude, duration	Switching off loads, capacitor energisation
	Sustained Interruptions	Duration	Faults
Voltage imbalance		Symmetrical components	Single phase loads, single phasing conditions
Waveform distortion	Harmonics	THD, harmonic spectrum	Adjustable speed drives and other non-linear loads
	Notching	THD, Harmonic spectrum	Power electronic converters
	Dc Offset	Volts, amps	Geo-magnetic disturbance, half wave rectification
Voltage flicker		Frequency of occurrence, modulating frequency	Arc furnace, arc lamps

As power quality problems have existed for a long time, conventional mitigation methods for these problems also are well developed. Passive filters based on inductors and capacitors are used in many transmission and distribution applications. Some of these filters are tuned to bypass specific harmonic frequencies, however the use of passive elements at high power levels result in bulky devices that are further limited due to their fixed range of operation (Ghosh & Ledwich 2002, p. 19).

1.3.3 Power System Compensation

Uncontrolled flow of Vars and imbalances in transmission networks can lead to system instability and overvoltage problems, voltage fluctuations and transmission system power transfer limitations. Var sources within power systems include the inductances in electrical machines, loaded transmission lines, transformers and reactors, and the capacitances in cables and unloaded transmission lines. The relationship between real and reactive power is indicated in Figure 1.9.

To balance or control system Vars requires the use of power system compensation. Compensation devices are used for harmonic filtering, load balancing, power factor correction and voltage regulation. These devices can be connected in both shunt and series, although shunt devices are more popular than series devices due to ease of protection. Some devices are used as load compensators to correct unbalance and distortion in load currents such that compensated loads draw balanced sinusoidal current. Compensation devices include, but are not limited to:

- Mechanically switched reactors and capacitors;
- Synchronous capacitors;
- Thyristor controlled shunt and series compensation, and;
- Converter controlled shunt and series compensation.

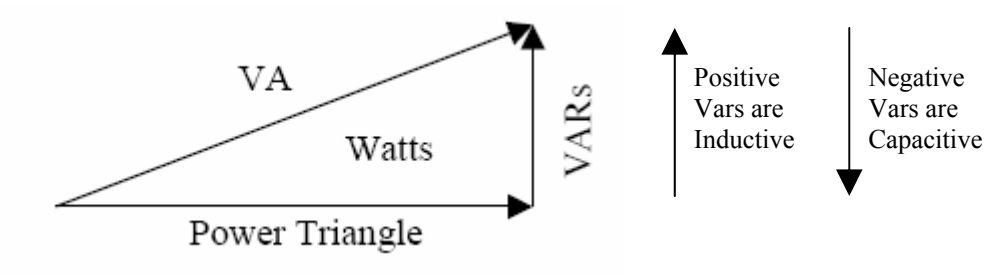

Figure 1.9: Power Triangle

Power system compensation is achieved by counteracting the Vars with a reactive power source of the opposite 'polarity'. The connection of a shunt reactor, or inductor, will lower system voltage by counteracting long or lightly loaded transmission line capacitance, whereas the connection of a shunt capacitor will raise or support system voltage by counteracting voltage drop associated inductive transmission lines or poor power factor.

An equivalent circuit of power system load conditions may be represented as in Figure 1.10 as a voltage source E, a transmission line, which may be represented as an inductance X_s, due to the high reactance to resistance ratio of the transmission network, and load X_L.

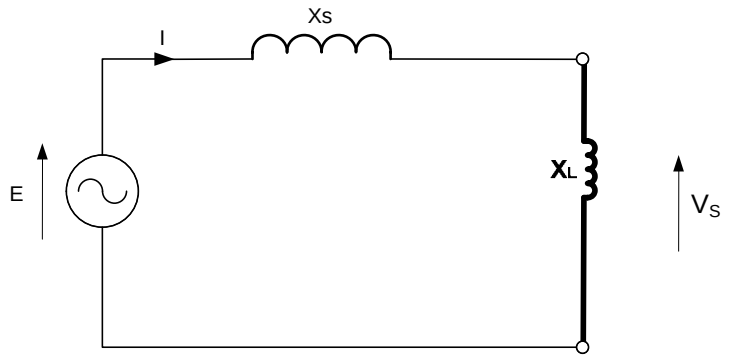

Figure 1.10: Power System equivalent circuit

Using the voltage divider rule the voltage appearing at the load terminals is defined by:

$$V_S = E \cdot \frac{X_L}{X_S + X_L} \qquad (1.2)$$

V_S will always be less than the generated voltage E as inductive reactance X_S is positive and the term $\frac{X_L}{X_S + X_L}$ will always be less than one.

An equivalent circuit of power system compensation may be represented as in Figure 1.11 as a voltage source E, a transmission line reactance X_s, and a capacitive reactance X_C.

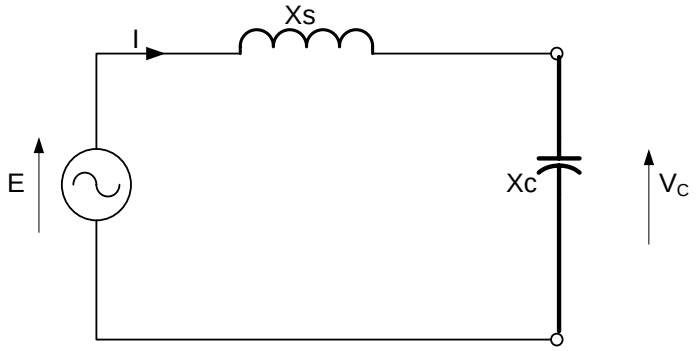

Figure 1.11: Power System compensation equivalent circuit

Now, the compensated voltage appearing at the load terminals is defined by the equation:

$$V_c = E \cdot \frac{X_c}{X_S - X_C} \quad (1.3)$$

V_C will be greater than the generated voltage E as capacitive reactance X_C is negative and the term $\frac{X_C}{X_S - X_C}$ will be a value greater than one.

Power transmission limitations may be quantified by means of the power transfer equation, with variables as defined in Figure 1.12.

$$P = \frac{V_1 V_2}{X} \sin\left(\delta_1 - \delta_2\right) \quad (1.4)$$

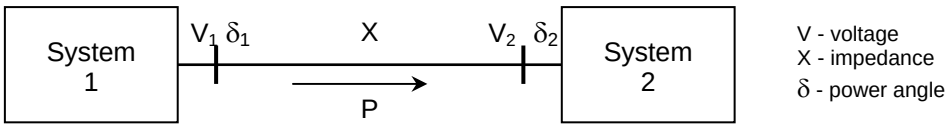

Figure 1.12: Power Transfer

Var imbalance or lack of power system compensation will result in a reduction in the receiving end voltage V_2 and a poor power factor angle δ_2, both attributes reducing the power transfer capability of the transmission line.

In theory, a transmission system can carry power up to its thermal loading limits. However in practice, loading to its thermal limits is not possible due to the following constraints:

- Transmission stability limit: the limits of transmittable power through which a transmission system can endure major faults on the system with transmission capability intact defines the transient stability limit as per Figure 1.13;
- Voltage limit: the limits of power transmission where system voltage can be kept within permitted deviations from nominal, that is +10%, -6% (NEC 2002).
- Loop flow: power flowing from one point to another may not always take the most direct path, possibly generating additional line losses or unintentionally overloading portions of the transmission network.

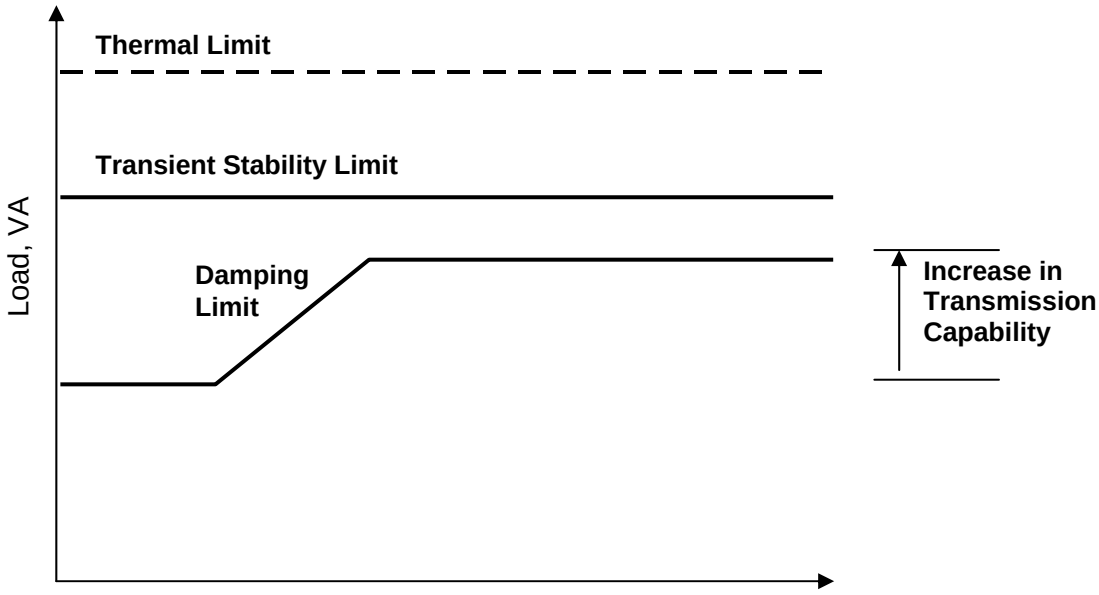

Figure 1.13: Power Transmission Capability

The voltage limits are governed by reactive power, in turn dependent on the physical length of the transmission circuit. The longer the line or the heavier the loading, the more reactive power will be present and the greater the magnitude of voltage drop due to that reactive power. Voltage will continue to drop as a consequence until a critical point is reached where the voltage collapses altogether.

Use of power system compensation will reduce reactive power present, decreasing voltage drop and increasing power system stability. Therefore the power transmission capability will be increased.

Traditional methods of power system compensation utilise fixed reactive plant such as capacitor banks and reactors. This is referred to as static compensation, and is unable to adapt to changes in power system configuration and generation patterns. Therefore dynamic compensation capable of adapting to changes in power system conditions is advantageous in that it can adjust the amount of compensation delivered.

2. Power System Compensation

2.1 Dynamic Power System Compensation

Dynamic power system compensation may be achieved by the use of Thyristor Switched Capacitors (TSC) and Thyristor Controlled Reactors (TCR) whose schematic representation is displayed in Figure 2.1.

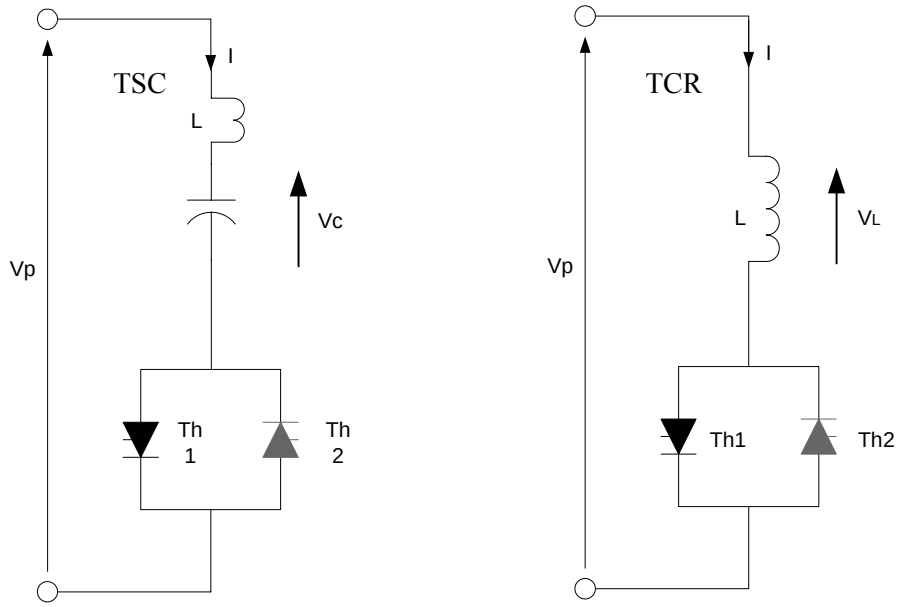

Figure 2.1: TSC and TCR line diagram (ABB 1999a)

2.1.1 Thyristor Controlled Reactor

Current in a thyristor controlled reactor can be continuously varied from zero to maximum by phase angle controlling the gating or conducting signal to the thyristors. The reactor is connected in series with two opposite poled thyristors. One of these thyristors conducts in each positive half cycle of the supply frequency, while the other conducts in the corresponding negative half cycle (Tyll 2004, p. 4).

The gating or 'turn on' signal to each thyristor is delayed by α, the firing or conduction angle, from the zero crossing of the source voltage as illustrated in Figure 2.2. As current lags the voltage across the reactor by ninety degrees, so a firing angle of ninety degrees results in maximum, that is, continuous reactor current. For a firing angle of 180°, the reactor current will be zero. As the thyristor firing angle is increased from 90 towards 180 degrees, the current in the reactor is reduced (Hingorani & Gyugyi 2000, p. 146). Therefore, the firing angle must be in the range $90\circ \leq \alpha \leq 180\circ$.

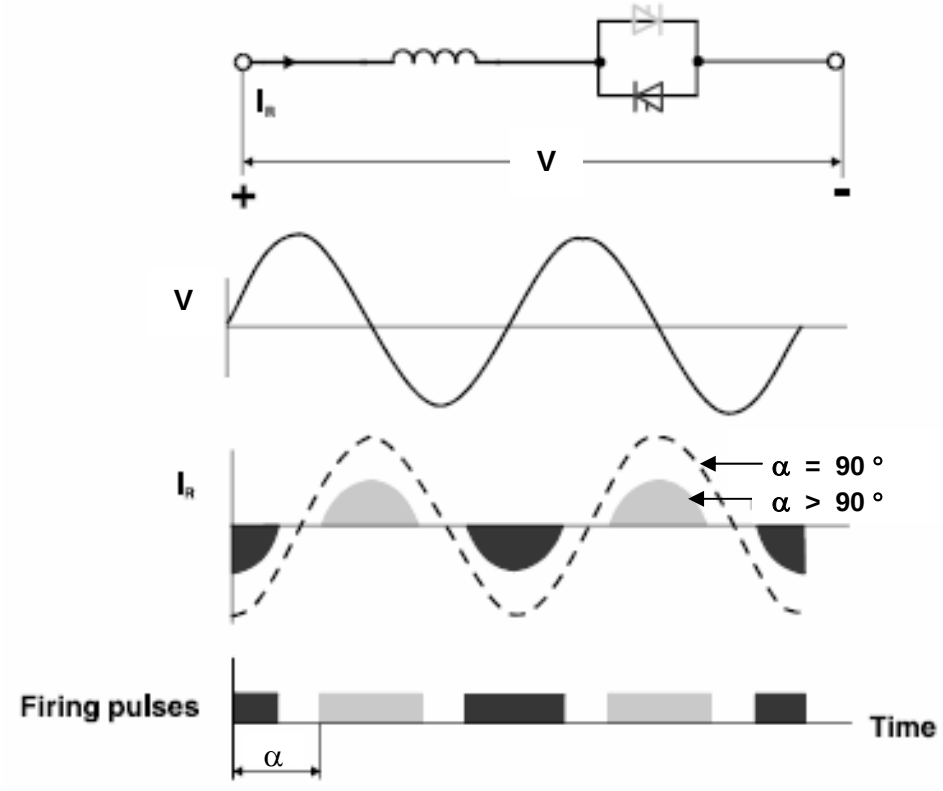

Figure 2.2: Thyristor Controlled Reactor current waveform (ABB 1999a).

Figure 2.3 indicates TCR arrangement, switching waveforms and characteristics.

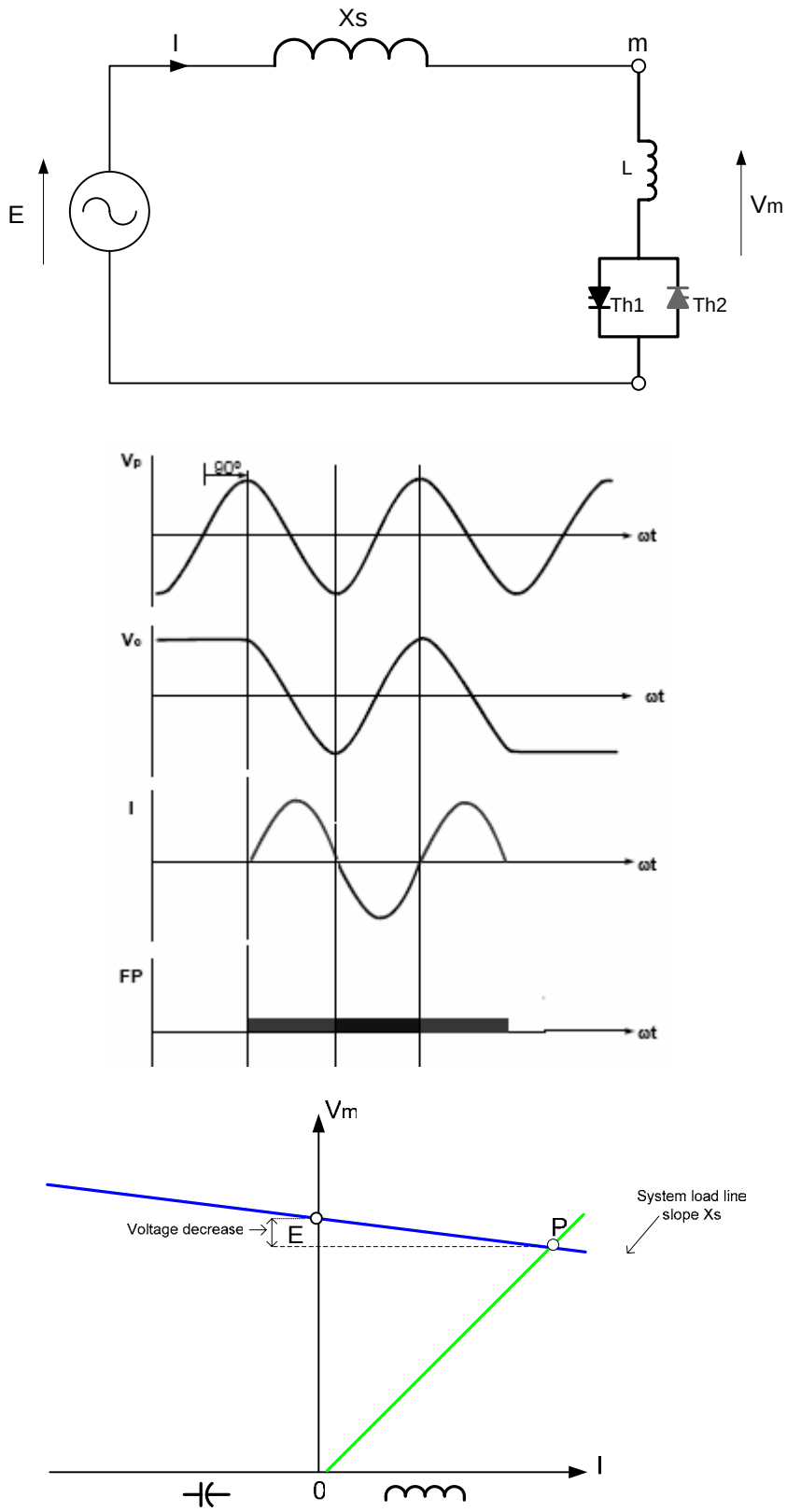

Figure 2.3: TCR Characteristic (ABB 1999b)

A current or voltage waveform that deviates from a pure sinusoid at fundamental frequency contains harmonics. For thyristor controlled reactors, as the areas under the positive and negative half cycles of the current and voltage waveforms are of equal size and shape, the wave form includes only odd harmonics (ABB 1999b). Thus harmonics of order 3, 5, 7, 9, 11 and so on will be generated by the TCR with the amplitude of the harmonics varying with the firing angle (Tyll 2004, p. 8). The third harmonic component is the most significant as highlighted in Figure 2.4.

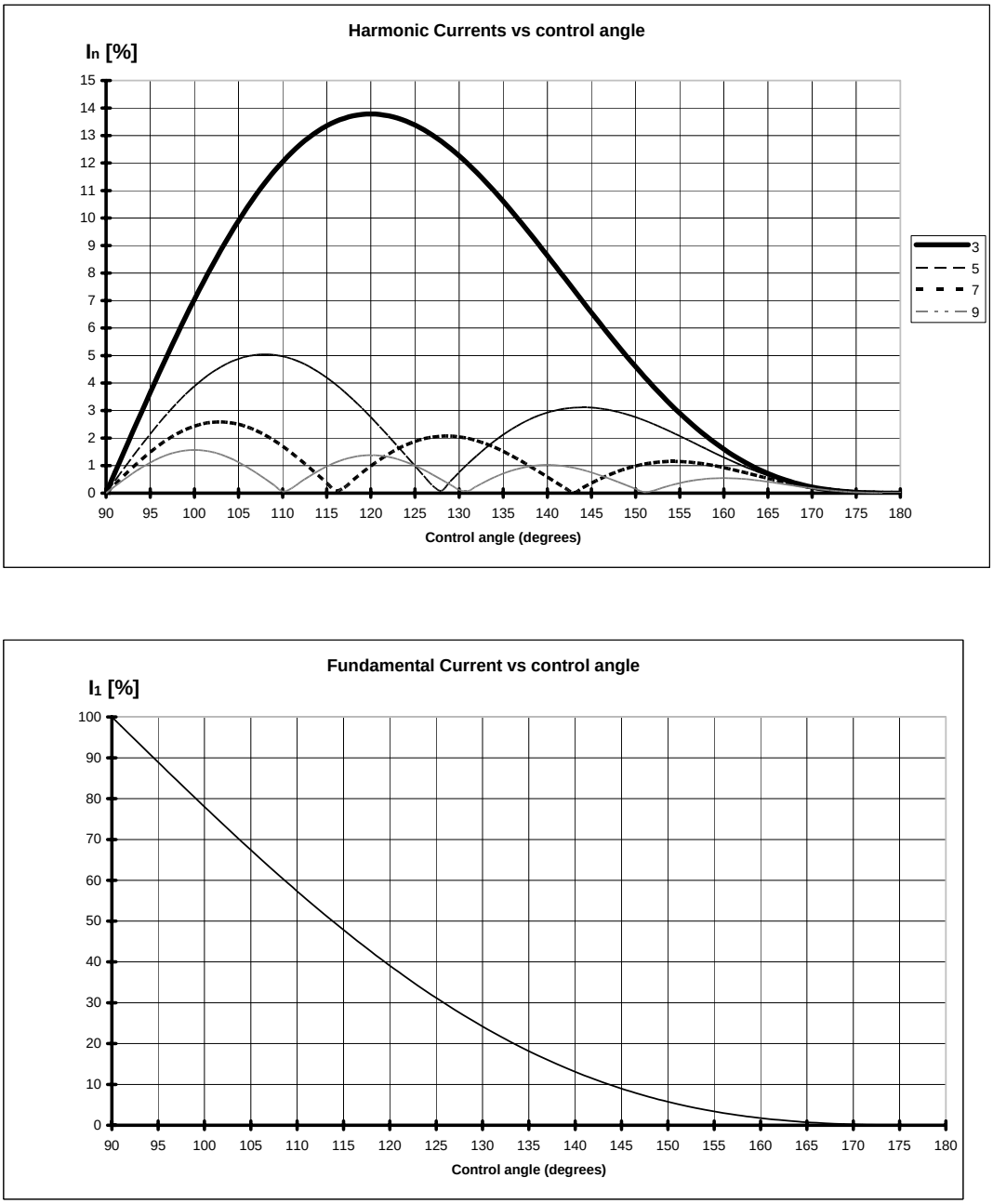

Figure 2.4: TCR Fundamental current and harmonic magnitude (ABB 1999a)

2.1.2 Thyristor Switched Capacitor

A thyristor switched capacitor (TSC) is a capacitor connected in series with two opposite poled thyristors so that one thyristors conducts in each positive half cycle of the supply frequency, while the other conducts in the corresponding negative half cycle. The current flowing through the capacitor may be controlled by blocking the thyristors. To achieve controlled reactive power a TSC is always configured in groups (ABB 1999a).

One disadvantage in utilising a TSC is the switching transients produced. Since a TSC blocks current when the thyristors are blocked and allows current to flow when the thyristors are gated, severe transients will occur if a TSC is switched off while the current through it is not zero (Tyll 2004, p. 9). Similarly, to avoid generation of transients during switch on, the thyristor must receive its firing pulse at a particular instant of the voltage cycle. That is, transient free switching may be obtained when the voltage across a capacitor is either at its positive peak or negative peak such that the current through the capacitor is zero.

A TSC exhibits a relationship between current and voltage as shown in Figure 2.5.

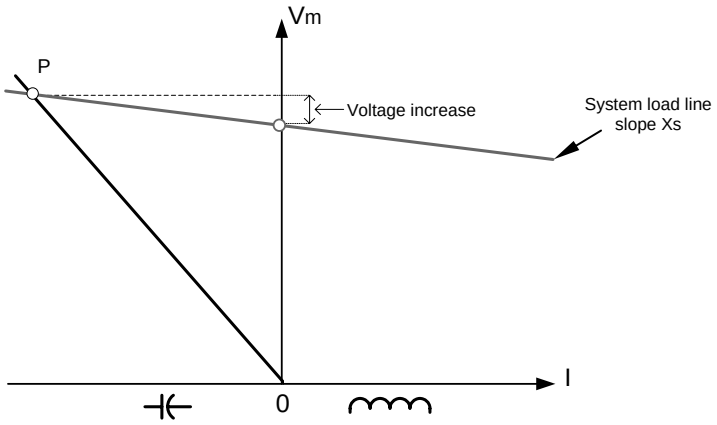

Figure 2.5: V/I performance of TSC (ABB 1999b)

2.1.3 Combined Dynamic Characteristics

A Thyristor Controlled Reactor (TCR) and capacitor combination exhibits a relationship between current and voltage as indicated in Figure 2.6.

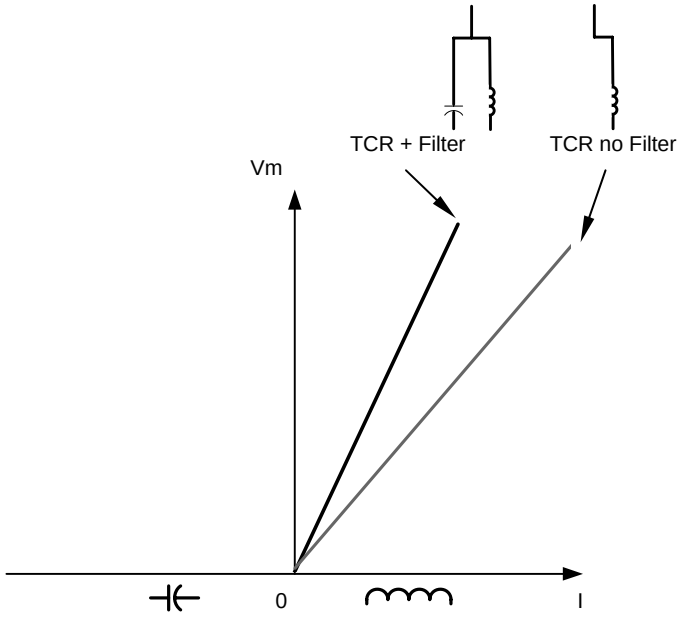

Figure 2.6: V/I performance of TCR with/without filter (ABB 1999a)

The inductive reactance X_L is defined

$$X_L = j\,\omega\,L\,, \tag{2.1}$$

and capacitive reactance X_C is defined

$$X_C = -\frac{j}{\omega\,C}\,, \tag{2.2}$$

therefore the combined reactance X_{SVC} is

$$X_{SVC} = j\,\omega\,L - \frac{j}{\omega\,C_{FC}}\,. \tag{2.3}$$

Therefore the arrangement indicated in Figure 2.7 will provide dynamic compensation over the combined inductive and capacitive Var range with the relationship between current and voltage as shown.

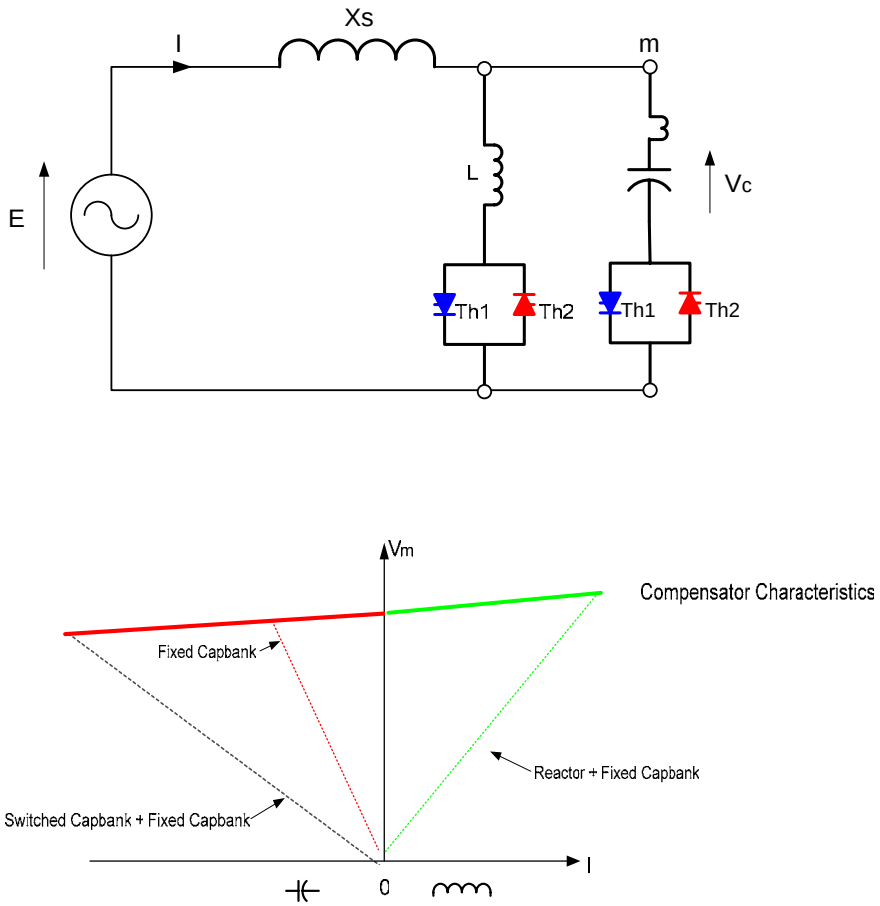

Figure 2.7: Combined TCR / TSC Characteristic (ABB 1999b)

2.2 Static Var Compensation

A Static Var Compensator (SVC) consists of thyristor controlled reactive plant, either capacitor banks, reactors or both, in combination with fixed reactive plant. This variable static equipment provides continuously variable reactive power injection or absorption to the network, facilitating dynamic Var balancing and so improves the efficiency, controllability and quality of power systems.

SVCs are commonly connected at transmission substations via star-delta vector group step down transformers, and consist of shunt connected inductors or capacitors, or more commonly a combination of the two, where at least one is variable (ABB 1999a). Variable inductors take the form of thyristor controlled reactors. Within an SVC, capacitors usually take the form of fixed or mechanically switched banks which may also be subdivided into harmonic filtering circuits tuned to the dominant frequencies. Thyristor switched capacitors are used when fast or varied frequency capacitor switching is required (Janke 2002, p. 4).

The main purpose of an SVC is to regulate and control substation bus voltage to the desired level, providing fast control of steady state and dynamic voltages and improving system stability by reactive power control of dynamic loads (Janke 2002, p. 7). This will result in increased power transfer capacity as SVCs present a variable impedance of controllable power angle (ABB 1999b) and maintain a stable voltage profile along the transmission line. SVCs also provide dynamic compensation of variable, unbalanced loads.

Damping of system electro-mechanical oscillations between generators is enhanced by controlling the power oscillations in transmission lines (ABB 1999b). Therefore SVCs enhance 'First Swing' stability by maintaining system voltages during large disturbances, providing active damping of power swings between weak interconnecting power systems (Hingorani & Gyugyi 2000, p. 139). Dynamic, fast response reactive power compensation following system contingencies such as network short circuits, line and generator disconnections and load shedding is also established by SVCs.

The use of SVCs for power system compensation provide the added benefit of reducing required insulation levels by providing fast overvoltage control and suppression of voltage fluctuations caused by disturbing loads such as large thyristor drives and electric arc furnaces. This provides improvement of the efficiency of industrial processes by voltage stabilization and fast power factor correction (ABB 1999b).

There are two main SVC types in common use, and are defined by the manner in which the reactive power is utilised for compensation. SVCs are primarily used for compensation of transmission lines and for balancing of single-phase railway loads, that is, voltage imbalance.

Static Var Compensators for transmission applications are required to:

- Regulate and control voltage at the point of connection;
- Enhance damping of system electro-mechanical oscillations, and;
- Provide fast reactive Var support following system contingencies.

Static Var Compensators for load balancing applications are required to:

- Convert single phase load into balanced three phase load;
- Reduce negative sequence components in system voltage, and;
- Regulate positive sequence components in system voltage.

SVCs utilised for transmission applications generally have symmetrical phase control and the same swing range in all three phases. Compensators for load balancing are single phase controlled and may have different swing ranges in different phase groups (ABB 1999b).

Single line drawings of a typical transmission application SVC and a typical load balance SVC are shown in Figure 2.8.

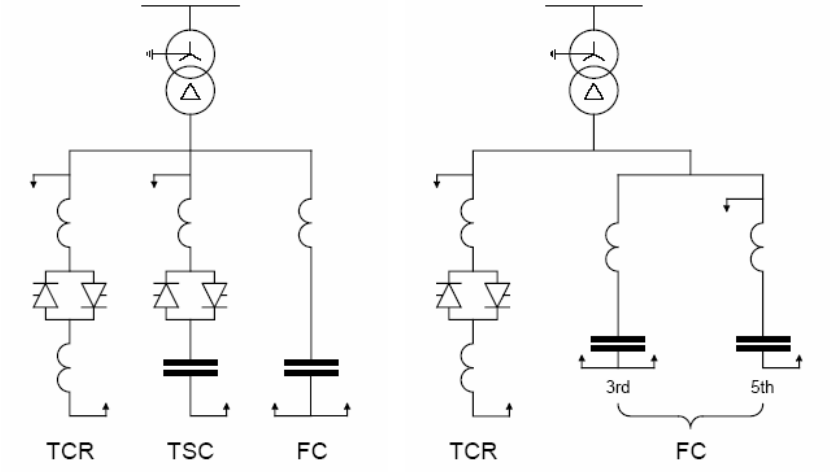

Figure 2.8: Single Line Drawings of Typical SVCs (Janke 2002, p. 6)

Both SVC types have a TCR branch and a FC branch, whereas only transmission application SVCs utilise a TSC branch. The composition and arrangement of an SVC is determined during the specification and design process (ABB 1999a).

TCRs must be delta connected to allow the current through the reactors to be continuously controlled from zero to full conduction. The TSC branch has a current inrush limiting reactor and is also connected in delta. The fixed capacitor (FC) branch is arranged as one or more tuned filters and may be connected in star or delta (ABB 1999a). If the fixed capacitor is specified as balanced on all three phases, a star connection is more economical. If the swing range of the SVC, that is the range of reactive power that the SVC provides, is unbalanced then one or more of the filters may be delta connected.

A load balancing type SVC will usually operate with asymmetrical phase swing ranges, and the triplen harmonics generated by the thyristor switching will not be suppressed in the delta winding of the transformer. Therefore, this type of SVC will require a third harmonic filter (Janke 2002, p. 7).

2.3 Load Balancing Static Var Compensation

2.3.1 Load Balancing Requirements

Queensland Rail (QR) operates an AC electrified railway in the central Queensland region. The railway is a heavy haul system comprising over 1000 km of track and is used to transport coal from inland mines to export and generation facilities on the east coast. Supply is provided from a 132kV network via 13 railway substations, each of which has two or three separate 30MVA single phase 132 / 50 kV transformers (ABB 1999b).

The traction system is supplied via a 25kV catenary provided by 50 / 25 kV autotransformers located at intervals along the track. Traction loads are single phase with time dependent characteristics and may reach short duration peaks of between 20 and 40 MVA (ABB 1998). As this region is located at some distance from generating stations, most parts of the system used to supply the railway loads possess low fault levels due to high source impedance. This would result in unacceptable levels of NPS voltages and currents in the power system if no compensation was applied (Janke 2002, p. 6).

A fully loaded locomotive imposes a 50 A load at 50 kV (ABB 1998). As a heavy coal train consists of four such locomotives it imposes a 10 MW unbalanced load upon the supply system. Several coal trains may be present upon a particular section of the rail system at any time. Harmonics are generated by the locomotive thyristor drives, and NPS is generated due to the unbalanced nature of traction loading. Therefore, 3^{rd}, 5^{th} and 7^{th} harmonic filters are required on the 50kV system to mitigate the effect of the traction loading (ABB 1999b).

The Australian Standard for induction motor design AS1359.31 specifies that motors should be designed to withstand 1.0 % NPS only, with the NEMA standard of the USA similar to this. EDF, the French standard for traction loading, also allows a maximum 1.0 % NPS under normal system conditions but with an increased limit of 1.5 % under contingency situations. The UK standards BS2613, BS4999 and BS5000 allow NPS levels of 2.0 % for one minute only under contingency conditions.

The German VDE0530 standard allows 0.7 % NPS for 10minutes such that

$$k_u = \sqrt{\frac{1}{T}\int_{i=0}^{T} V^2{}_{NPS}\, dt} < 0.7\ \%\ , \qquad (2.4)$$

and the limits imposed by QR of

- 0.7 % for half hour maximum demands;
- 1.0 % for five minute peak loads, and
- 2.0 % for one minute peak loads,

are almost identical to the German Standard.

Nine load balancing type SVCs are used throughout Central Queensland, as shown in Figure 2.9, to provide voltage support and reduce NPS voltages caused by the unbalanced loads.

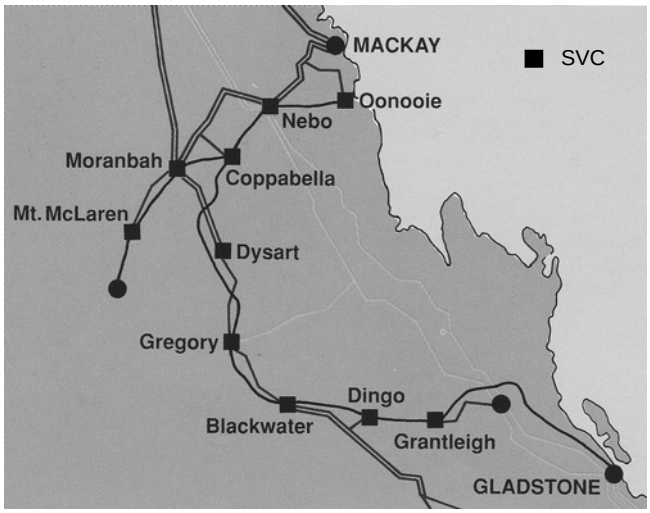

Figure 2.9: Load Balancing SVC location (ABB 1998)

The SVCs are required to balance the single phase traction load and to provide power system voltage regulation. Each SVC is configured to ensure that the overall NPS voltage at the various railway substations does not exceed the regulatory limits (ABB 1998).

Figure 2.10 shows the impact of the SVCs on voltage balancing as well as voltage support of the 132kV supply system.

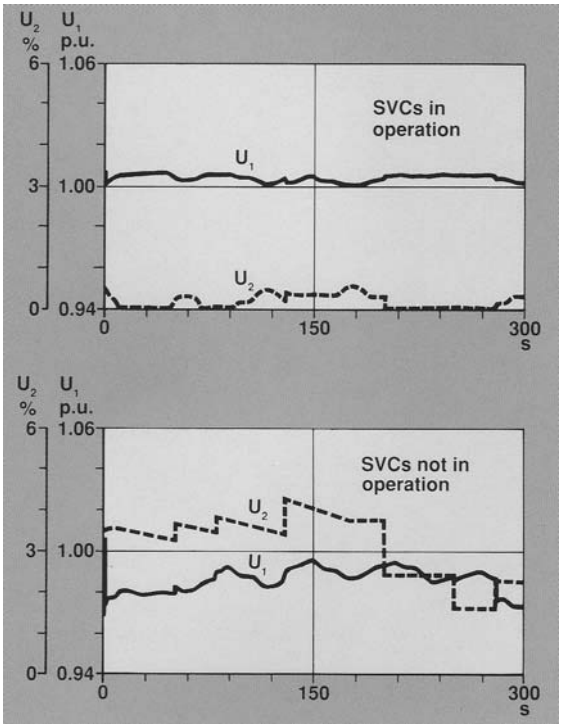

Figure 2.10: Positive and Negative Sequence voltage balancing (ABB 1998)

In addition to the nine SVCs, a total of 28 single phase harmonic filters have been installed in the 13 railway substations, tuned to the 3rd, 5th and 7th harmonics (Ghosh & Ledeich 2002, p. 38), to prevent the injection of substantial amounts of harmonics generated by locomotives into the 132kV Power system.

2.3.2 Load Balancing SVC Substations

A typical traction substation arrangement is in accordance with Figure 2.11. The SVC usually comprises a TCR operating in parallel with a fixed capacitor bank configured as a third or fifth harmonic filter (Janke 2002, p. 9).

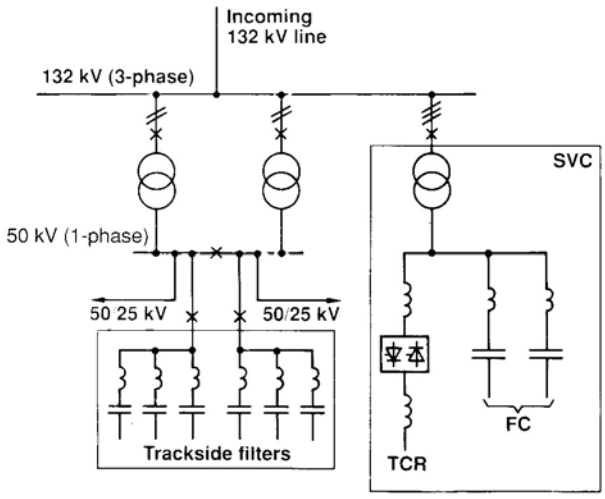

Figure 2.11: Typical Traction Substation arrangement (Janke 2002, p. 13).

The thyristor valve of the TCR is water cooled and consists of a number of thyristors connected in series. Thyristor control circuitry is of the magnetic firing type which supplies trigger pulses from the ground potential without the need to obtain auxiliary power from the voltage across the thyristors. This firing system is very simple and reliable and is used in SVC systems worldwide (Bacha et. al. 2004, p. 2).

To enable load balancing, each phase of the SVC is controlled individually by dedicated voltage regulators. As the SVC phases operate independently, each phase may possess a different swing limit. The TCR rating is determined by the highest inductive requirement per phase plus the necessary inductive reactive power to provide bias for the capacitive requirement (Janke 2002, p. 38). Ratings and swing ranges of the central Queensland load balancing SVCs are listed in Table 2.1.

Table 2.1: Load Balancing SVC range and ratings (Janke 2002, p. 41)

Load Balance SVC Location	Swing Range + Capacitive MVar, - Inductive MVar		Transformer & Reactor Ratings
Grantleigh	A – B B – C C – A	+13 to -4 +7 to -10 +7 to -10	TCR = 51 MVar Transformer = 36 MVA Ratio = 132 / 5.7 kV
Blackwater	A-B, B-C & C-A	+18 to -33	
Gregory	A-B, B-C & C-A	+30 to -21	
Mt McLaren	A-B, B-C & C-A	+33 to -18	
Dingo	A – B B – C C – A	+10 to -13 +10 to -13 +17 to -6	TCR = 69 MVar Transformer = 40.5 MVA Ratio = 132 / 7.7 kV
Dysart	A-B, B-C & C-A	+29 to -40	
Oonooie	A – B B – C C – A	+17 to -14 +19 to -12 +16 to -15	TCR = 93 MVar Transformer = 60 MVA Ratio = 132 / 10.4 kV
Coppabella	A – B B – C C – A	+20 to -11 +20 to -11 +18 to -13	
Moranbah	A-B, B-C & C-A	+42 to -51	

The principle by which traction load is balanced is simple. For example, traction loading connected between B and C phase may be represented by two phasor sets of equal magnitude but opposite phase rotation as shown in Figure 2.12. Load balance is achieved by introducing a set of three phasors with negative phase rotation and a 180 ° phase shift to the original NPS phasor. In this manner the traction load appears as a three phase symmetric load of correct phase rotation and the NPS component is nullified.

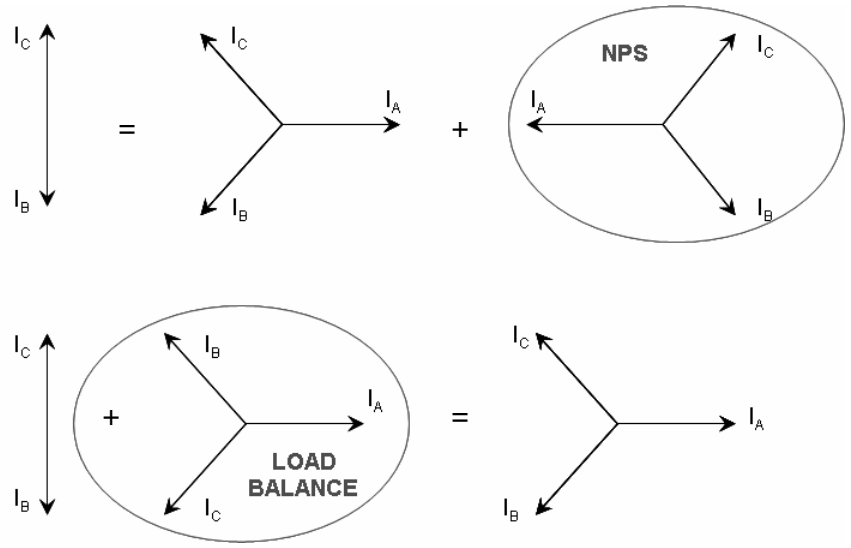

Figure 2.12: Phasor representation of balancing single phase loading (NOT TO SCALE).

2.3.3 Blackwater Static Var Compensator

The Blackwater 132 kV Static Var Compensator is located approximately 200km west Rockhampton. This station is included in stage one, Gladstone to Blackwater, of the Queensland Rail electrification project (ABB 1998). The single line diagram of the SVC layout is illustrated in Figure 2.13.

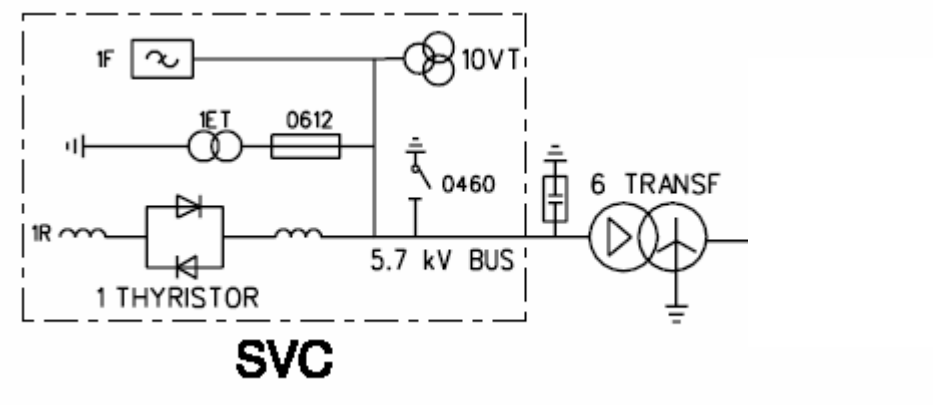

Figure 2.13: Blackwater SVC single line diagram (Powerlink 2005)

Blackwater SVC is designed to compensate for NPS and voltage variations caused by the single phase locomotive loads. This is achieved by connecting a fixed capacitor bank and thyristor controlled reactors to the network. The capacitor bank is tuned to the 3rd harmonic current in order to filter the harmonics produced by the thyristor switching (ABB 1999b). As the Blackwater SVC supplies three 132 / 50 kV railway substation transformers, each supplying two traction feeders, the SVC swing range is balanced on all three phases and hence the capacitor bank is of equal phase ratings and star connected.

The SVC is connected to the 132 kV transmission system via a 132 / 5.7 kV, 36 MVA step down transformer of the Y / d11 vector group. The voltage transformer supplying the regulator voltage reference circuits is also connected to the 132 kV transmission system. All other SVC plant such as the TCRs, third harmonic filter, earthing transformer and voltage transformer supplying the thyristor reference voltage circuits are supplied at 5.7 kV to reduce the insulation levels required (ASEA 1986, p. 5). This introduces a phase shift between the two voltage transformer secondaries and as the 5.7 kV voltage transformer provides the phase reference for the thyristor firing, this must be compensated for within the SVC control system.

3. SVC Control Systems

3.1 Nomenclature

Table 3.1 provides an interpretation of selected symbols used in within ASEA SVC control system abridged schematics. This table has been devised by a comparison of abridged schematics, the circuit diagrams available and inspection of the control system card circuitry.

Table 3.1: Identification of ASEA SVC control system abridged schematic symbols.

Symbol	Interpretation
	Integrator
	Constant multiplier
	Proportional Integral controller
	Inverting rectifier
	Variable Limit
Σ	Summing junction
S&H	Sample and Hold
U	ABB / ASEA naming convention denoting voltage

3.2 SVC Control System Function

The primary purpose of an SVC control system is to produce firing signals to thyristor valves to phase angle control the reactor in such a manner that a continuous controllable output of reactive power is obtained on a cycle by cycle basis produces the desired effect on the transmission system (Janke 2002, p.5). When the thyristors in the thyristor valve are fully conducting, the reactor consumes more than the reactive power generated in the fixed capacitor bank and the net output from the compensator is inductive. When the thyristors are blocked, there is no current in the reactor and the output from the compensator will be all the reactive power generated in the capacitor bank.

To fulfill its primary purpose, a SVC control system may utilise input signals such as voltage, summated current and synchronizing signals. Output signals would include the firing signals to the thyristor valves. A simplified view of SVC control system function is illustrated in Figure 3.1.

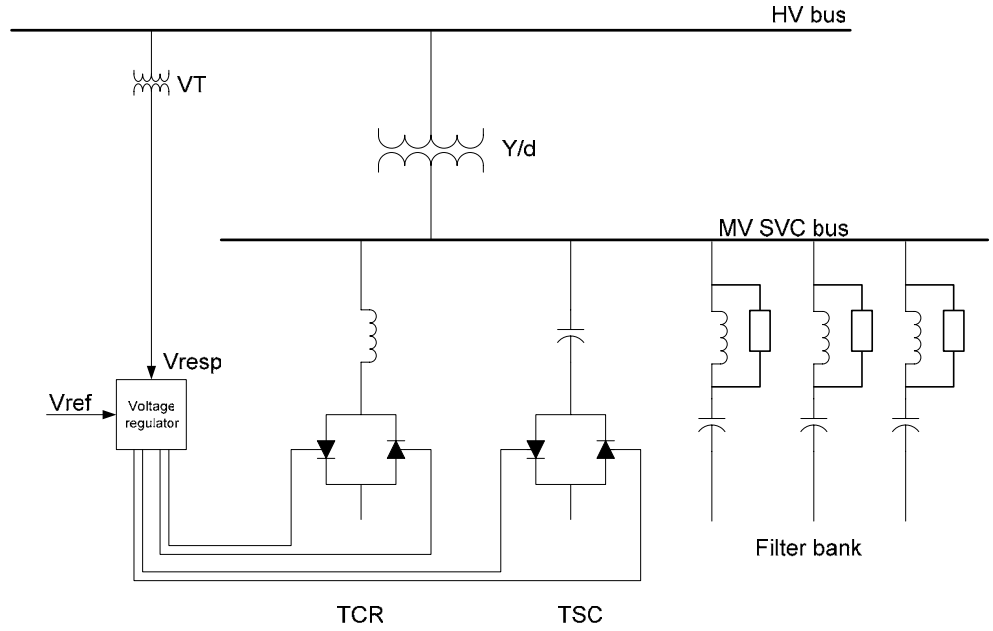

Figure 3.1: SVC Control System Overview (ABB 1999b)

3.3 SVC Control System Structure

An SVC control system consists of:

- A measurement and comparison system;
- Automatic voltage regulator (AVR), and
- A calculated susceptance output, B_{REF} .

Figure 3.2 indicates the composition of a basic SVC control system.

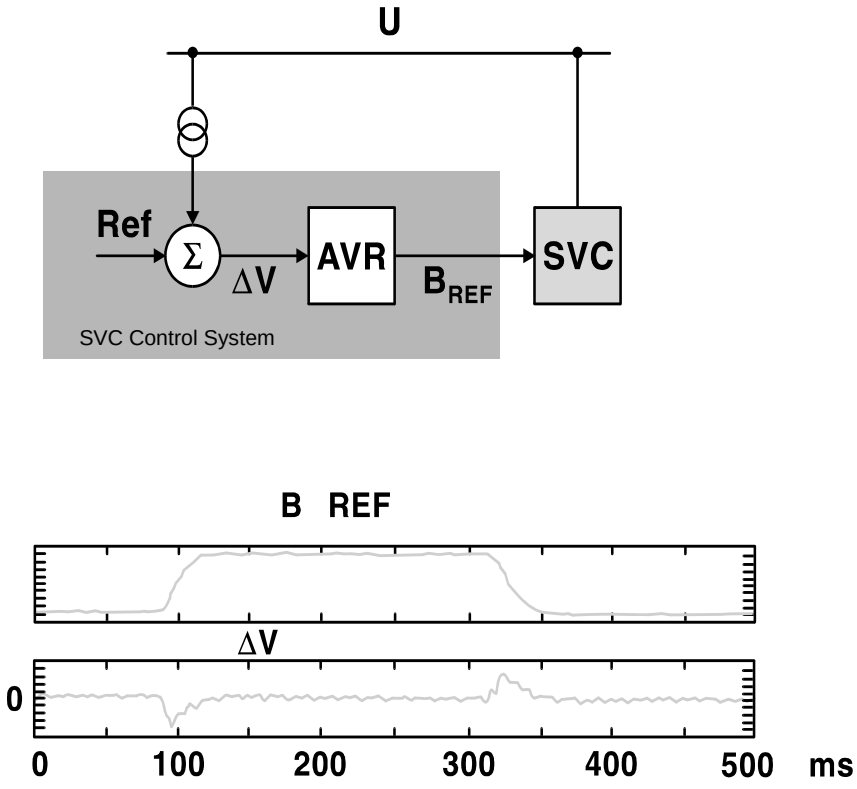

Figure 3.2: Basic SVC Control System composition (ABB 1999b)

The measured system voltage is compared with the target voltage, V_{REF} , with the difference denoted ΔV, or the error voltage. This ΔV determines the voltage response of the SVC, as error signal determines the susceptance calculated by the AVR and this signal in turn determines the firing angle of the thyristors.

3.3.1 Automatic Voltage Regulator

The automatic voltage regulator (AVR) uses a PI regulator to maintain primary voltage at the reference voltage and to return system voltage to this reference as rapidly as possible after a system disturbance (ASEA 1986, p. 16). PI controllers are characterised by rapid response to large error signals due to the proportional control element, and no steady state error due to the action of the integral controller.

Regulator gain determines the control system response time and stability. Gain is the amplification of the voltage response signal, and an optimum gain setting would be determined during commissioning of the SVC (Janke 2002, p. 7).

Transmission application SVCs commonly utilise automatic gain control (AGC). If power system configuration or load were to alter substantially, the gain setting may be too high resulting in unstable SVC response. This instability is detected by the AGC and the gain reduced until response stability is detected (Janke 2002, p. 8). The gain is then reset to the optimum value when the system is restored to the normal configuration. Figure 3.3 indicates the configuration of a basic SVC control system.

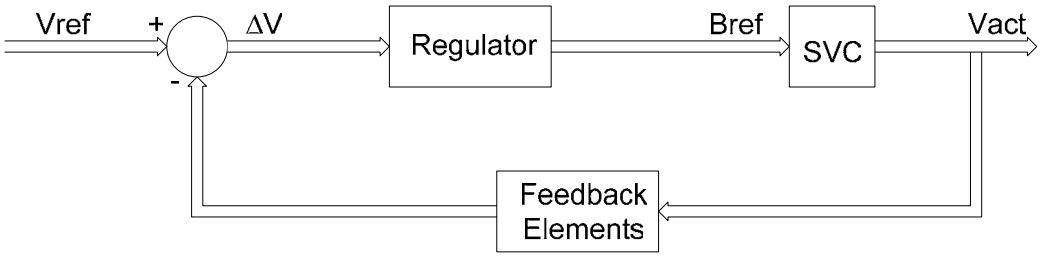

Figure 3.3: Basic Closed loop SVC control (ABB 1999b)

Primary susceptance B_{ref} is calculated by the voltage regulator and determines the TCR firing angle α. As susceptance is the inverse of reactance, the larger the calculated signal the more current that will flow within the SVC. The output of the SVC will follow the V-I response to a maximum voltage of 1.1 per unit. If the control system calculated susceptance attempts to increase voltage beyond this point, the control system will limit the TCR current to a maximum value. This facility is called Q-limit control and is implemented within the control system to ensure that the equipment ratings are not exceeded (Janke 2002, p. 16).

3.3.2 Slope

Slope, or voltage 'droop', is defined as the allowable amount of deviation of the actual voltage from the target voltage as illustrated in Figure 3.4. SVC slope is provided to stabilise voltage control in the presence of other regulators, such as where adjacent SVCs may attempt to respond to the other's control actions. The slope circuit reduces by some percentage the response of the SVC to a given voltage error. In the absence of a slope setting, the SVC attempts to reduce the error voltage to zero (ABB 1999b). In this situation a small capacity SVC connected system with low source impedance would exhibit very large changes in output for very small changes in bus voltage.

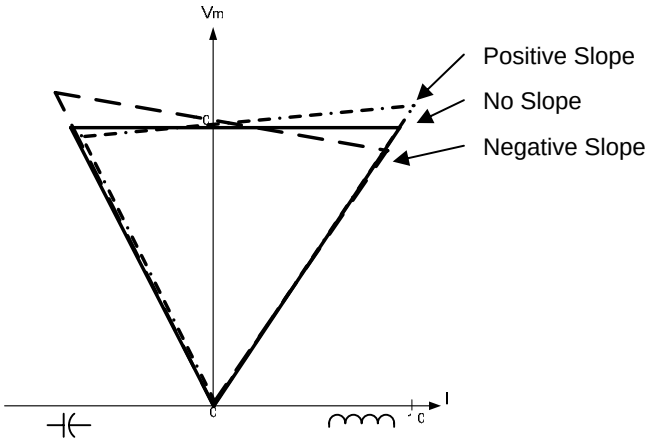

Figure 3.4: Slope correction (ABB 1999b)

As the slope setting is increased, the SVC output swing for a set change in system voltage is decreased. This is achieved by feeding back a proportional amount of B_{REF} (ABB 1999a) as indicated in Figure 3.5.

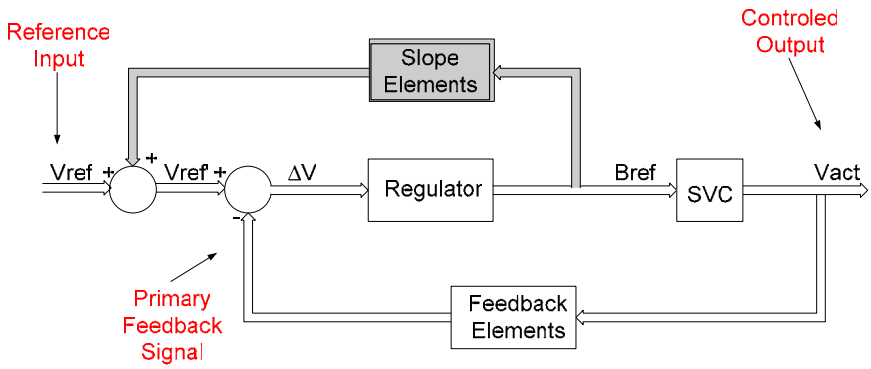

Figure 3.5: Closed loop SVC control with slope correction (ABB 1999a)

3.3.3 Data Acquisition

The most common input quantities to an SVC control system are the primary phase voltages and supply currents as may be determined from Figure 3.6. SVC control system measurement structures are configured to detect positive-sequence primary voltage. For transmission applications the SVC measurement systems utilise discrete Fourier computation techniques to evaluate fundamental voltage over a one-cycle running average window (ABB 1999b). The voltage measurement incorporates a phase-locked loop (PLL) circuit to accommodate system frequency variations (ABB 1999a). Load balancing application SVCs use analog inputs, rectified and filtered to produce DC voltage levels from which the individual phase voltage regulator response may be determined.

Current measurement allows SVC control systems to calculate primary reactive power. For transmission application SVCs this calculated power is used for power oscillation damping (POD), providing dynamic and rapid response to electro-mechanical oscillations between interconnected power systems (Janke 2002, p. 5). Load balancing type SVCs utilise this quantity to calculate the compensating reactance required for each individual phase pair.

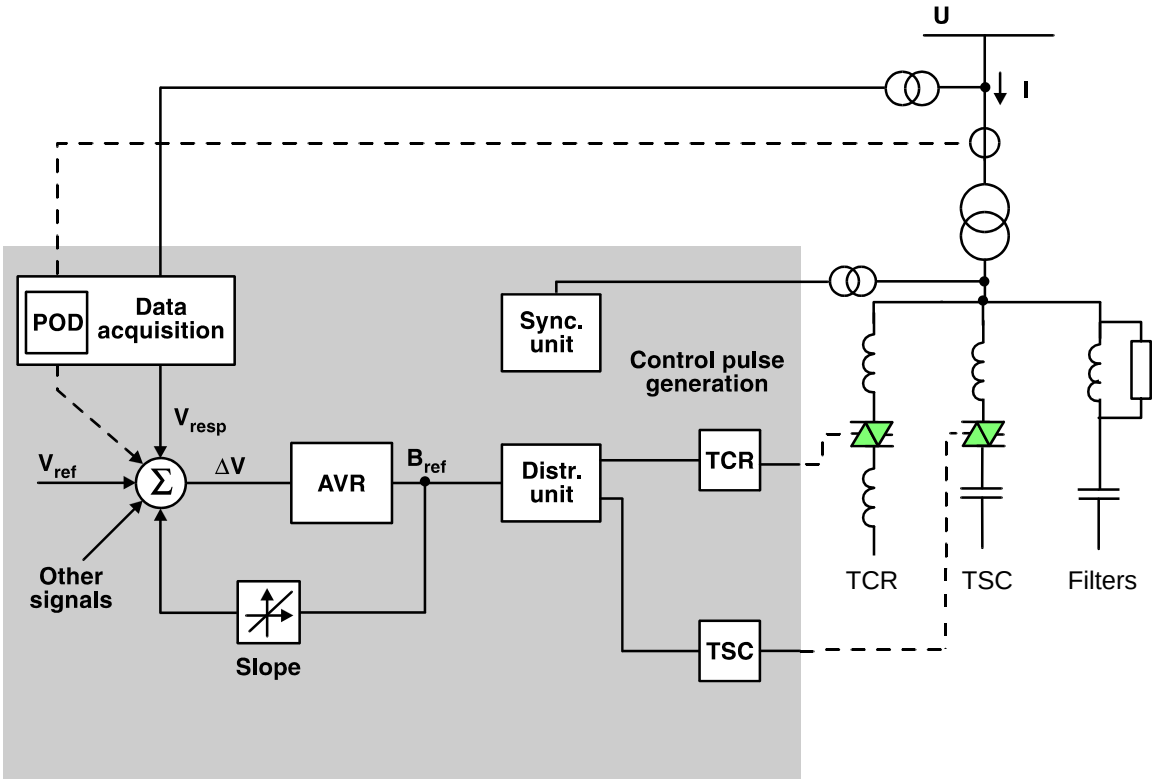

Figure 3.6: I/O signals associated with typical SVC control systems (ABB 1999a)

3.3.4 Modes of Operation

SVC control systems may have both a manual and an automatic operating mode. Manual operating modes are often referred to as B_{REF} control and the automatic mode as V_{REF} control. In B_{REF} control mode, the SVC operates as if it were static reactive plant providing fixed susceptance to the power system.

When selected to V_{REF} control mode, the SVC attempts to maintain target voltage and the SVC susceptance output will vary according to the system voltage. If the measured power system voltage was greater than the target, the control system response is such as to create an inductive reactance to decrease system voltage. For measured power system voltages less than the target value, control system response is intended to present a capacitive reactance to the power system and thus raise voltage levels.

3.4 Load Balancing Type SVC Control Systems

The purpose of load balancing type SVC control systems is to regulate TCR current in order to balance traction load and force each phase voltage to assume equal magnitude with correct phase displacement and rotation. This type of SVC comprises two parallel control systems. One is an open loop load balancing scheme and the other is a closed loop voltage regulating scheme for NPS voltage minimisation and positive sequence voltage support (Janke 2002, p. 12). For balancing of asymmetric load by means of an SVC, individual control of phase to phase SVC susceptances is required, necessitating the use of three separate voltage regulators as highlighted in Figure 3.7.

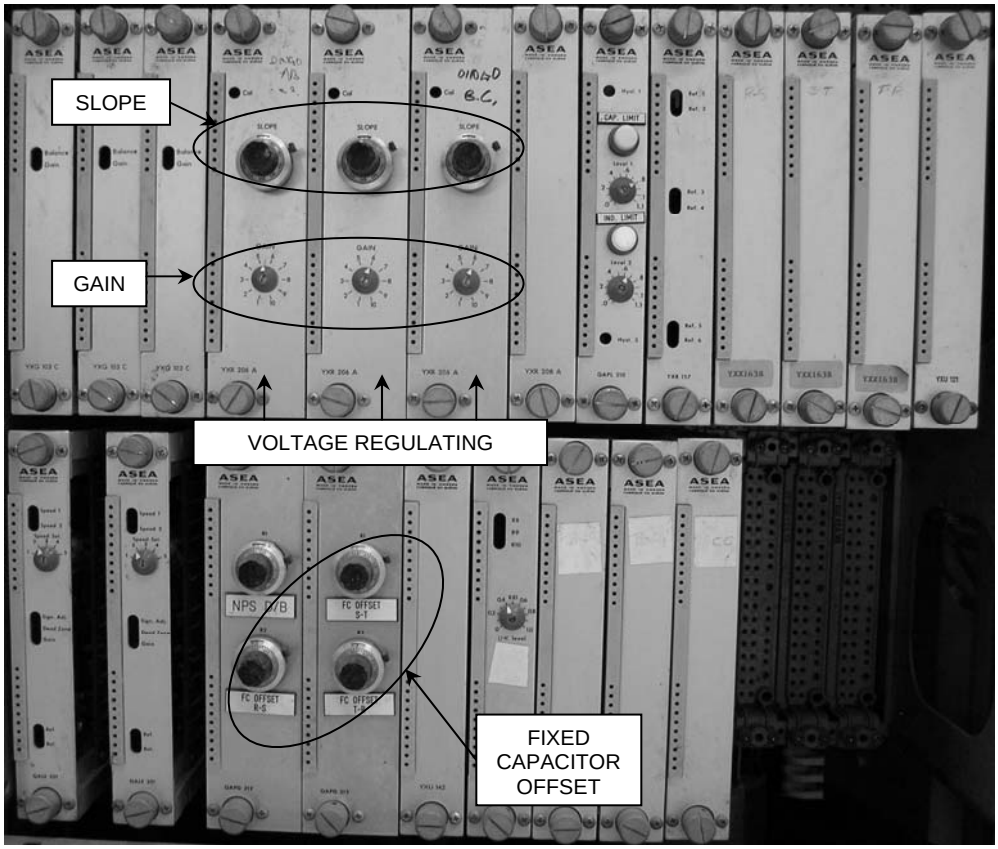

Figure 3.7: Load balancing SVC control system

The manufacturer's abridged schematics for they key functional control system modules are contained in Appendix C. To avoid confusion, the voltage phases within the SVC are referred to as R, S and T for A, B and C phases respectively.

3.4.1 Open loop Load Balancing

In the load balancing scheme, load reactive power consumption is measured phase by phase and thyristor control signals generated to adjust the phase reactive components until all three currents have the same magnitude and phase angle as the system voltages. SVCs are well suited to load balancing applications as they can respond quickly to load variations and thus minimise NPS voltages within the power system.

The open loop controller utilises the “Steinmetz” method for load balancing. This method provides rapid response to unbalanced loads (Bacha et. al. 2004, p. 2), and its output is supplied directly to the SVC control system phase susceptance calculations.

Load balancing utilising Steinmetz equations is achieved as follows:

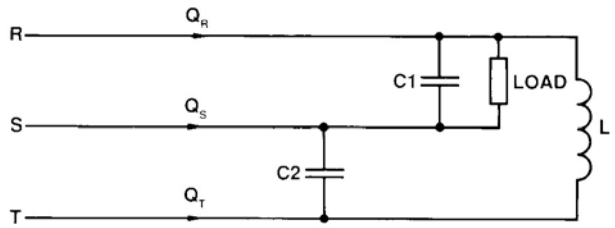

Figure 3.8 : Single Phase Loading (ABB 1998)

Phase currents during unbalanced loading as shown in Figure 3.8 may be defined as follows:

$$I_A = I_{AB} - I_L ; \quad (3.1)$$

$$I_B = I_{C2} - I_{AB} , \text{ and} \quad (3.2)$$

$$I_C = I_L - I_{C2} . \quad (3.3)$$

A load connected between two phases of a three phase system can be made to appear symmetrical and have unity power factor as seen from the three phase system by applying reactive elements between the phases (Ghosh & Ledeich 2002, p. 42).

The Steinmetz formula relates the per phase reactive powers to a set of phase to phase reactive powers as follows:

$$Q_{RS} = Q_R + Q_S - Q_T \ , \tag{3.4}$$

$$Q_{ST} = Q_S + Q_T - Q_R \ , \text{ and} \tag{3.5}$$

$$Q_{TR} = Q_T + Q_R - Q_S \tag{3.6}$$

(Janke 2002, p. 45). If the single phase load consumes an active power P and a reactive power Q, it can be demonstrated that the reactive values needed between the phases for total three-phase symmetry are given by

$$Q_{C1} = Q \ , \tag{3.7}$$

$$Q_{C2} = \frac{P}{\sqrt{3}} \ , \text{ and} \tag{3.8}$$

$$Q_L = \frac{P}{\sqrt{3}} \ . \tag{3.9}$$

(Janke 2002, p. 45).

This is verified graphically in Figure 3.9. Traction load aggregate values of P and Q change substantially with time and require individual control of phase-to-phase susceptances, thereby satisfying the above equations (Bacha et. al. 2004, p. 2).

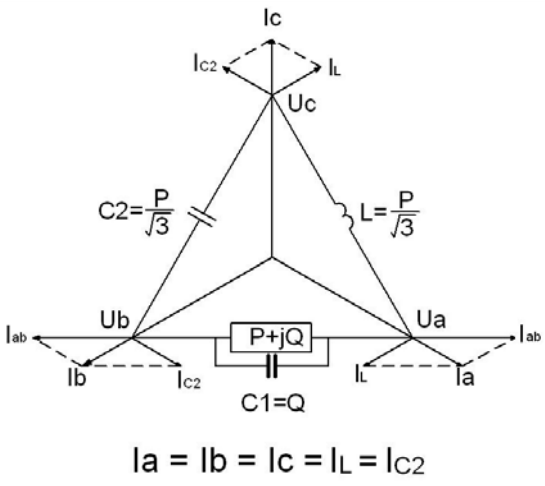

Figure 3.9: Symmetrizing of Single Phase Loads (Janke 2002, p. 45)

However, the TCR is delta connected on the secondary side of a Y / d11 vector group transformer. Applying the necessary transformations to relate the required reactive power of the TCR to balance and compensate the load measured on the primary side of the transformer yields the following formulas:

$$Q_{RS} = \frac{-Q_A + 5\,Q_B - Q_C}{3} \tag{3.10}$$

$$Q_{ST} = \frac{-Q_B + 5\,Q_C - Q_A}{3} \tag{3.11}$$

$$Q_{TR} = \frac{-Q_C + 5\,Q_A - Q_B}{3} \tag{3.12}$$

(ASEA 1986, p. 42)

The open loop control is configured to directly apply this linear combination of measured reactive powers, and the resultant signals Q_{RS}, Q_{ST} and Q_{TR} are supplied to the closed loop controller where they are added to the voltage regulator calculated output.

3.4.2 Closed Loop Voltage Regulation

In the closed loop voltage regulation scheme, the phase to phase voltages are measured and corrective actions calculated to reduce NPS and maintain the voltage at the target value, referred to as positive phase sequence regulation. System voltage NPS is reduced by forcing the voltages in each phase group to assume the same magnitude. Positive sequence voltage control is achieved by the symmetrical addition or subtraction of reactive power (Ghosh & Ledeich 2002, p. 38). Therefore the closed loop voltage regulator will inherently reduce NPS voltages associated with three phase load imbalance on untransposed transmission lines.

The closed loop voltage regulation circuits comprise the following functions:

- Voltage response;
- Voltage reference;
- NPS deadband, and
- Voltage regulator.

Each individual regulator controls the voltage for one phase pair, and the actual voltage of that phase pair is compared to the target voltage. This is used by the voltage regulator to generate the required corrective action in terms of a susceptance referred to the A-B-C phase system, as opposed to the R-S-T phase system on the secondary side of the SVC transformer. For an ASEA manufacture load balancing type SVC control system, closed loop voltage regulation is performed by the YXR 206A card. As this is the most critical component of the SVC control system during normal operation, the majority of the project modelling and validation was devoted to this function.

The following main functions are indicated on the YXR 206A circuit board in Figure 3.10:

1. Active rectifier for voltage response;
2. Summing junction for response and reference;
3. Sample and hold to produce error signal ΔV;
4. PI-regulator;
5. Slope and NPS deadband;
6. Summing junction for regulator output and load balancing circuit output, and
7. Sample and hold for resulting B_{REF} value.

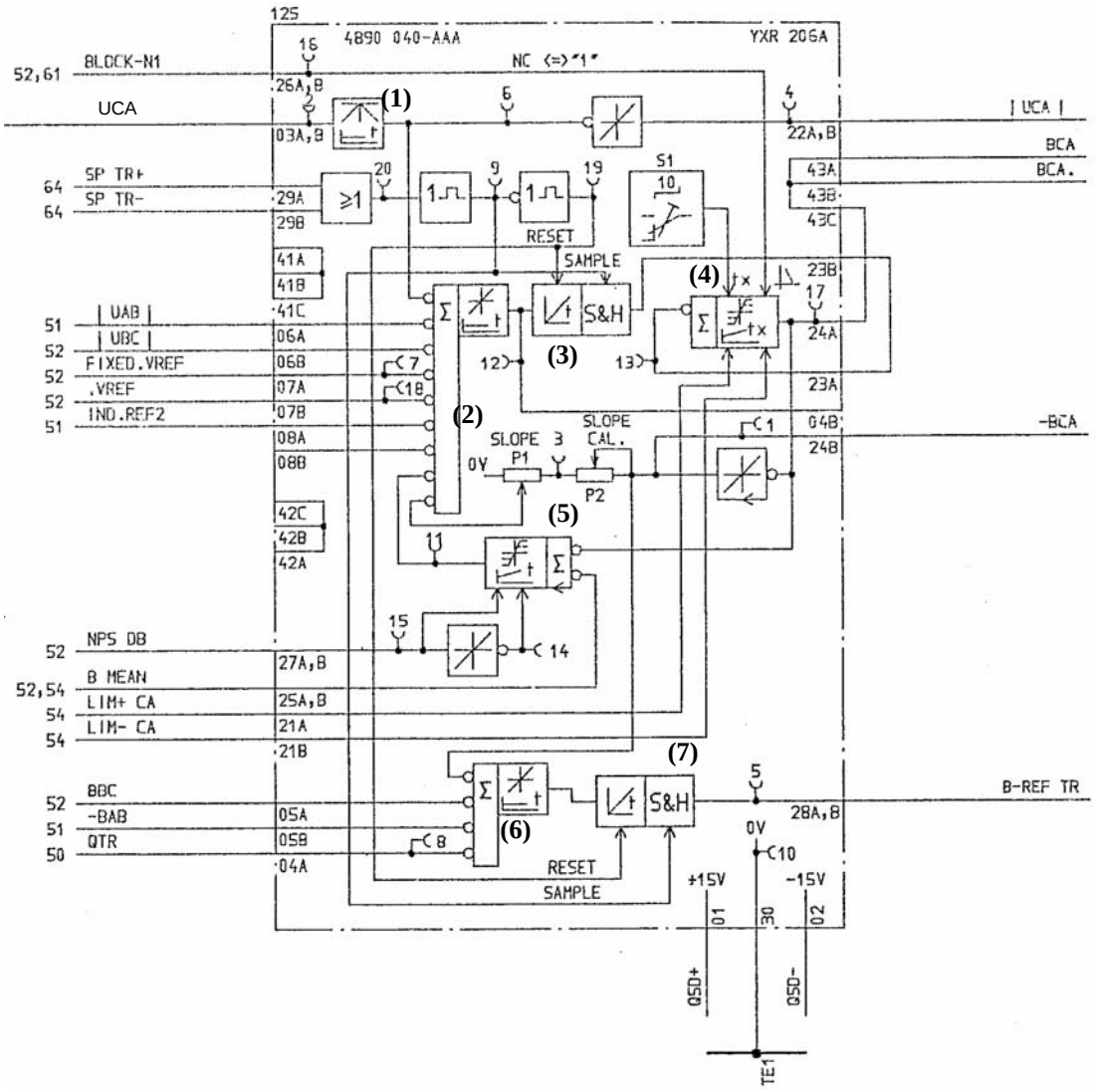

Figure 3.10: C-A∅ closed loop voltage regulation card abridged schematic (ASEA 1986, p. 15)

Point (1) in Figure 3.10 corresponds to the active rectifier, which outputs a two pulse rectified signal. As the phase to phase peak voltage will be 10 V corresponding to a primary system voltage of 132 kV, or 1.0 pu, the average value of the inverted and rectified waveform will be – 5.2 V (ASEA 1986, p. 16). The inverted and rectified signal is then exported for use on the other phase regulators.

In the summing junction at (2) the rectified voltage response is combined with a proportionally reduced input from the other two phases, and compared with the voltage reference. The resultant error signal, ΔV, contains a 100 Hz ripple due to the two-pulse rectified voltage response (ASEA 1986, p. 16). This ripple is eliminated in the sample and hold circuit at (3).

Error voltage ΔV is input to the PI controller, identified as item (4) on Figure 3.10. By means of a 10-step selector switch S1, the integration time constant may be varied between 0.33 and 10 ms, corresponding to a gain factor of approximately 1.5 between the settings available (ASEA 1986, p. 17).

Due to load balancing type SVC requirements for individual phase voltage regulation, automatic gain control is not incorporated as it would be in transmission application SVC control systems. Load balancing type SVC voltage regulator gain is manually set by the dial on the front of the control system card YXR 206A, and must assume the same value for all three phase regulators.

The operational gain setting is determined during the manufacturer's commissioning process and may not be appropriate for the current power system configuration if significant changes have occurred. This would include changes in system impedance as influenced by the expansion of industrial load and reconfiguration or extension of the local power system.

SVC Slope is obtained by feeding back the PI regulator output signal to the summing junction via potentiometer P1. Without slope the voltage regulators will attempt to maintain voltages UAB, UBC and UCA at an equal value (ASEA 1986, p. 17).

The NPS deadband setting determines the power system voltage NPS level which will be tolerated before corrective action is taken and is introduced at point (5) on Figure 3.10. This is a PI controller that compares the phase susceptance, BCA in the abridged schematic, with the BMEAN signal which is the average of BAB, BBC and BCA. If BCA is not equal in magnitude to BMEAN, an additional signal will be input to the summing junction to for the phase susceptance to equal the average (ASEA 1986, p. 24). This results in symmetrical control of the SVC, allowing some NPS to remain in the power system voltage.

If the deadband setting is large, the closed loop voltage regulator will be forced to perform positive phase sequence voltage control in the absence of the open loop load balancer operation (ASEA 1986, p. 24). That is, the closed loop control scheme can be configured to perform load balancing operations but NPS minimisation capability will be sacrificed.

The output of each voltage regulator is then ‘star-delta’ transformed to convert the A-B-C susceptance requirement to a R-S-T susceptance value at point (6) on Figure 3.10, by application of the following formulas:

$$B_{RS} = \frac{2\ B_{AB} + 2\ B_{BC} - B_{CA}}{3}\ ; \qquad (3.13)$$

$$B_{ST} = \frac{2\ B_{BC} + 2\ B_{CA} - B_{AB}}{3}\ , \text{and} \qquad (3.14)$$

$$B_{TR} = \frac{2\ B_{CA} + 2\ B_{AB} - B_{BC}}{3}\ . \qquad (3.15)$$

(ASEA 1986, p. 18)

A signal Q is added from the load balancing circuits and contains a 100 Hz ripple due to the multiplication in the Var-transducers (ASEA 1986, p. 18). This ripple is eliminated in the sample and hold circuit at (7). The output from this point is the required SVC susceptance BREF to be input to the control signal generation. At this point, 10 V corresponds to the full range of the TCR (ASEA 1986, p. 18). The required SVC susceptances are then produced by altering the delay angles of the thyristor firing pulses.

If the signal BLOCK-N1 goes low, the voltage regulator output is forced to zero (ASEA 1986, p. 18). This signal is applied when the SVC is halted.

3.4.3 Priority Control

Each load balancing type SVC control system has a priority system established such that the order of priority of its three main functions is:

1. Open loop controller load balancing;
2. Closed loop controller balancing of the 132 kV phase to phase voltages thereby eliminating NPS, and
3. Closed loop controller regulation of the 132 kV voltages to be equal to the primary reference voltage, also referred to as positive phase sequence voltage control.

(Janke 2002, p. 18).

When the TCR current in one phase reaches a limit, either fully off or fully on, the priority control system alters the voltage reference point away from the set value so that NPS control can be maintained. That is, the ability to maintain system voltage at the set point is sacrificed in order to maintain NPS minimisation. The priority system detects the presence of capacitive or inductive limits by checking if the secondary control signals are in their valid working range of 0 to 9.2 V (ASEA 1986, p. 27).

Once the priority control system operates, the positive sequence voltage will no longer be regulated to the target value and load balancing will no longer provide power factor correction (Janke 2002, p. 18). When a TCR operational limit is encountered, the priority controller rapidly increments the reference voltage set point in the opposite direction to allow the TCRs to return to nominal operational range. The priority controller then slowly increments the reference voltage set point back towards the target value (ASEA 1986, p. 20). If the target voltage is not achievable, the priority controller will be in continuous operation ramping quickly away from the encountered limit and ramping slowly toward the target voltage. This will result in an SVC output appearing as a saw-tooth wave. Therefore, the voltage dip exhibited in Figure 1.1 may have been due to the SVC priority controller encountering a TCR operational limit.

Positive phase sequence regulation has the lowest priority in the control system. The control system ramps the voltage set point as required to increase the load balancing capability and will continue to ramp away from the set point until simultaneous inductive and capacitive limits are reached (Janke 2002, p. 18).

3.4.4 Control Signal Generation

Load balancing type SVC control system signal generation is accomplished on the YXR 208A card. The abridged schematic indicating broad function is contained in Appendix C, Figure C.8.

The control signal generation card performs the following functions:

- Summation of B_{AB}, B_{BC} and B_{CA} ;
- Offset of B_{REF} to compensate for the SVC filter size;
- Generation of limiting signals, and
- Generation of minimum and maximum control signals.

(ASEA 1986, p. 19).

B_{AB}, B_{BC} and B_{CA} are summated to obtain the average susceptance, B_{MEAN}, used by the closed loop voltage regulator to control NPS. This value is generated by adding the three susceptance signals with a gain factor of one third (ASEA 1986, p. 20).

Each TCR has a control signal, US, which varies between 0 and 9.2 volts. The control signal generated in the YXR 208A card is transmitted to the trigger pulse circuitry controlling TCR thyristor firing. A US signal of 0 V supplied to the thyristor circuitry results in zero TCR current, whereas a signal of + 9.2 V results in full rated TCR current (ASEA 1986, p. 20). If the B_{REF} signal is equal to zero, SVC current should be zero and therefore the B_{REF} signal must be offset to compensate for the size of the SVC filter.

The output susceptance signal from the voltage regulators shall be limited according to the actual SVC operational limits. When an individual susceptance control signal approaches an inductive limit, the voltage regulators are limited in the negative direction by the signal LIM-. At the capacitive limit the voltage regulators are limited in the positive direction by the signal LIM+ (ASEA 1986, p. 21) as observed on Figure C.8 in Appendix C.

Values corresponding to the permitted minimum and maximum values of the US control signals are generated for use in the priority system (ASEA 1986, p. 21) and are set as part of the manufacturer's commissioning process.

4. Methodology

Project methodology has been developed to attain the general requirements of the project and to ensure model development and validation procedures are carried out in an efficient and effective manner. In addition, well documented project methodology ensures that foreseeable risks, resources and time requirements are accounted for.

The methodology determined for the research project is as follows:

- Investigation of the problem by theoretical analysis;
- Design Requirement also by theoretical design;
- Validation will be by empirical methods, that is, experimental, and;
- Reporting of results and conclusions.

4.1 Preliminary Tasks

The preliminary research project tasks may be divided into research of industry methods and requirements with regards to power system compensation, completion of technical research and choice of a model validation site for experimental work.

4.1.1 Industry Requirements

This objective shall be achieved by an evaluation of regulatory and operational requirements for voltage regulation and load balancing of power systems. This shall be sourced from National regulations and Queensland utility requirements such as the National Electricity Code (NEC), Electricity Supply Association of Australia (ESAA) regulations for supply quality and NEMMCO regulations.

4.1.2 Technical Research

The technical research project component shall be achieved by the collation of information regarding voltage compensation and balancing, including the varying techniques utilised by organisations to mitigate their impact. Control system operation and mathematical procedures for determining SVC response shall also be evaluated. This data may come from Australian Standards, technical papers, manufacturer's documentation, power system analysis and power electronics textbooks.

Technical research shall encompass a brief analysis of the causes and impacts of voltage imbalance, attributed to unsymmetric lines, voltage sag, switching and other transients, harmonics, unmatched load impedances such as those produced by traction loading, and power system faults. The impact of the resultant negative phase sequence (NPS) voltages on high voltage plant and power system operation shall also be reviewed.

Traction loading of power systems shall be discussed, with detailing of connections, load sizes, duty cycles and resultant unbalancing effects, that is, magnitude of NPS generation.

A review of power system compensation principles will be required, and a justification for the use of Static Var compensation provided. Information on the operation of SVC control systems and overall effect on the power system shall be discussed, and the mechanisms by which it achieves compensation for target power system conditions such as unbalance, abnormal voltage levels and NPS. A critical evaluation of the mechanisms by which SVC systems achieve voltage regulation, load balancing and minimisation of NPS voltages shall be performed. Input parameters required by the control system to achieve its functions shall also be identified.

4.1.3 Validation Site

The site for SVC control system validation was chosen to be Blackwater 132/66kV Substation, a Powerlink Queensland asset. This site was deemed most suitable for model validation as the initial voltage regulation malfunction was observed at this location. Blackwater SVC is located in the Central Queensland coal mining region and experiences significant traction loading. Historically, this site has displayed significant problems with NPS voltage levels and voltage stability.

As this SVC site is the most heavily loaded in the region and access is difficult to arrange, due to the potential impacts of control system malfunction it was deemed prudent to perform preventative maintenance before investigation of control system operation. To reduce the time the SVC was out of service, permission was obtained to perform the testing necessary for model validation concurrently with maintenance.

4.2 Model Development

A representation of the SVC control system model developed by Mr. Paul Windle of Powerlink Queensland is contained in Appendix D, Figure D.1. As the existing model is constructed using the Simulink SimPowerSys blockset, familiarity with Simulink and associated toolboxes must be developed. Continuation of development of the existing MATLAB model is justified by the large inbuilt maths library, power system toolbox and graphical tools. The model may be adapted utilising information obtained from manufacturer's documentation. The aim is to create a model that is simple to use and accurate. Model output should be graphically displayed in an easy to read and printable format, as graphical output is the most easily interpreted and widely accepted for control system responses.

Model development entails identification of required functionality and output. The SVC control system consists of a closed loop and open loop system in parallel and each system requires certain inputs and will output specific parameters. As a PI controller or similar is commonly utilised in SVC control systems, it is assumed that a second order approximation will provide acceptable accuracy. Major control system operational blocks must be identified and adequately represented.

Model response to step voltage imbalance will simulate relevant worst case conditions, as the Blackwater SVC experiences significant traction loading. Obtained responses must be assessed for validity, as for example the physical system is proven stable for 10 – 35 MW traction loading and model responses indicating instability in this region would be invalid. This will also verify to some degree the accuracy of the model content prior to validation.

4.3 Model Validation

Test methodology was required for the model validation process, as experimental requirements were considerable. Experimental framework was established as follows to ensure an efficient and effective testing process was implemented and that comparison of results was meaningful.

- The aim of the experiment was defined as *"To measure SVC control system voltage regulator response to step load imbalance"*.
- Control system output signals identified as required to be measured for direct comparison with theoretical results and calculation of system parameters are defined in Appendix C, Table C.2. Also identified is the associated signal ground for each measurement point as identified on the manufacturer's abridged schematics.
- The necessary inputs to the SVC control system to obtain the required outputs are provided by the ABB power system simulator, which allows the control system to operate while connected to a simulated network. This precludes the possibility of damage to SVC plant or instigating transmission network voltage disturbances.
- Test circuit layout necessary to obtain the required control system outputs was considerably simplified as the power system simulator connects directly to the SVC control system. Each chart recorder shall be connected to the measurement points and signal grounds as identified in Appendix C, Table C.2.
- The test equipment resources required to successfully obtain the experimental data required are listed in section 4.5.
- Test circuitry developed is detailed with the reporting of the experimental results obtained. This is presented in chapter 6.
- Consultation with the on-site supervisor, Mr. Phil Harvey, was conducted to ensure that developed experimental methodology was acceptable.
- Experimental documentation to provide guidance through the test procedure and facilitate reporting of results was developed to ensure repeatability. All chart recorder channels were permanently allocated to specific signal and identifying labels applied within the chart recorder setup as detailed in Appendix C, Table C.2.

The model validation process would then be performed. In order to perform these tests certain items were to be prearranged. These included human resources, transport, accommodation, access to test equipment, access to the SVC which involving an application to the Powerlink Network Switching Centre (NSC) with appropriate lead time, and availability of high speed chart recorders to measure control system responses.

Actual SVC control system response to power system load imbalances was to be measured and determination of the developed model validity by comparison of the predicted responses with measured values performed. Through the comparison of model responses against actual measurements discrepancies and anomalies were to be identified and investigated, seeking to identify probable cause and validating or otherwise the model and assumptions made during development. If significant discrepancies were identified it must be determined if the assumptions made during model development were unsuitable, such as if the second order system representation were too simplistic or the controller parameters incorrect. Identification of such issues should result in a model revision as time permits.

4.4 Experimental Methodology

Uniform SVC control system configuration was utilised to ensure repeatability of experimental testing and validity of comparison with theoretical responses as follows:

- The SVC control system was to be confirmed to be off line and the associated high voltage plant isolated and earthed;
- All chart recording equipment channels were to be connected to the measurement points defined in Appendix C, Table C.2 and confirmed at test commencement;
- Availability of mains power to the ABB power system simulator was to be confirmed, the test set turned on and the injection lead connected to the SVC control system cubicle panel designated KT1, terminal strip B50 at the plug sockets labelled as X7, X8 and X9;
- The SVC control system operating mode switch labelled KT1 was to be selected to TEST AUT, and
- Power system simulator potentiometers located on the test set cards labelled as QECS 7, 8 and 9 were to be set as outlined in section 4.4.2.

The following SVC control system settings were to be modified and records kept of the original settings to allow re-instatement at the conclusion of testing:

- NPS Deadband: Potentiometer R1 on card labelled QAPG 212 to be set to 0.0;
- Slope: Potentiometer on all three cards labelled YXR 206A to be set to 0.0;
- Gain: Dial setting on all three cards labelled YXR 206A to be varied from one dial setting below the initial set point for the first set of tests, to the initial setting for the next set and to one dial setting above for the last set of tests performed;
- Load Balancing: The ON-OFF switch labelled LOAD BALANCING on panel KT1 to be selected to OFF, and
- Priority System: Disabled by removing card QAPL 210 from panel KT1 rack U33 module position 135.

The ABB power system simulator was configured with a supply voltage negative phase sequence level of 0.0 % and a fault level of 280 MVA as selected by potentiometer SK1. System loading was selected on the three potentiometers labelled P_{AB}, P_{BC} and P_{CA} on the power system simulator as 0.2 per unit for two phases and 0.5 per unit for the remaining phase.

The experimental data was then obtained in the following manner:

- The chart recorder was confirmed as ready to capture data and suitably configured;
- SVC control system was activated, waiting several seconds for the start sequence to elapse;
- Step unbalanced load was applied by selecting the LOAD toggle switch on the power system simulator to ON for one second and then OFF, and
- The experimental data waveform captured by the chart recorder was printed out and the data file saved as a .MEM file with a unique identifier.

The unbalanced phase loading arrangement was then modified so as to apply to 0.5 pu load step to an alternate phase. The test was performed again as described and the load step moved to the remaining phase.

Voltage regulation gain, selected on the control system card labelled YXR 206A, was then modified and the entire sequence repeated. This process was conducted for all three gain settings as discussed.

At the conclusion of testing all original control system settings were re-instated to ensure correct functioning of the SVC when returned to service.

4.5 Test Equipment

The following test equipment has been identified as necessary for successful completion of project model validation:

- Two Fluke Digital Multimeters, for current and voltage measurements;
- Omicron Secondary Injection Test Set, incorporating high precision voltage and current outputs, logic inputs, outputs and a timer;
- ABB power system simulator, a device capable of simulating the single phase loading effect of traction loading on the power system as presented to the secondary systems, that is, the current and voltage transformer secondaries;
- Hioki high speed chart recorder with a minimum of six channels, utilized to capture control system output waveforms for analysis;
- Assorted connection leads with 4mm and 2mm plug attachments, for connection of injection and measurement equipment to the SVC control system;
- Extension leads and a residual current device for power supply to the test and measurement equipment while protecting personnel from electric shock, and;
- A variety of hand tools such as pliers and screwdrivers as required for isolation of CT and VT secondary circuits of the control system from supply to enable safe access, and for the connection of test and measurement equipment.

4.5.1 Chart Recorder

The chart recorder available to obtain the experimental data was a Hioki 32 channel hi-speed chart recorder, model 8826. This model is compatible with the Hioki 'Wv' proprietary wave viewing software version 1.17, allowing import of waveform data to computer. The capability to export the data in .csv file format for use by other applications is incorporated in the wave viewing software.

4.5.2 Power System Simulator

The ABB power system simulator provides a network model comprising the SVC transformer, reactors and filters, and the transmission network representation of generators, line impedances and loads (ASEA 1986, p. E.1). Circuits for measurement of voltage, NPS and load magnitude are also provided, with these values displayed as per unit quantities on the simulator as shown in Figure 4.1.

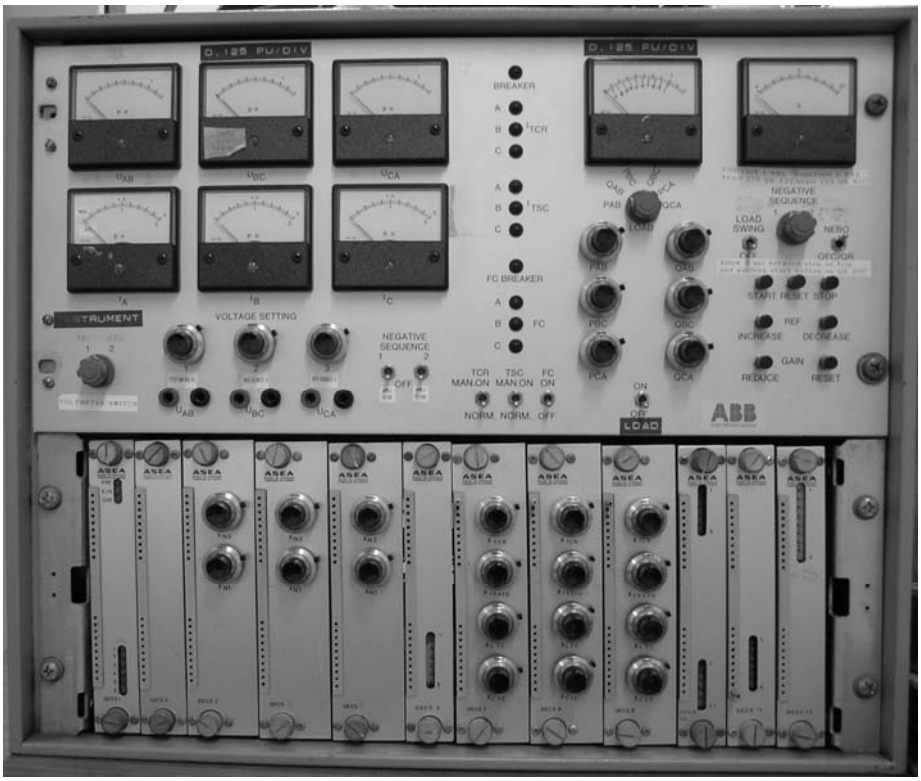

Figure 4.1: ABB power system simulator.

Apparent network impedances connected to the SVC control system may be adjusted to reflect actual values by potentiometers located on the front of the circuit boards. SVC transformer impedance X_T, TCR impedance X_{TCR} and filter impedances X_{CFC} and X_{LFC} may also be set to the values calculated by the manufacturer as specified in Table 4.1. The TCR and filter impedances for the Blackwater SVC are balanced across all three phases. Simulation of the SVC transformer also incorporates a summation amplifier forming the phase-current resulting from the Y / d11 vector group.

Table 4.1: Power system simulator settings for cards QECS 7, 8 and 9 (ASEA 1986, p. E.25)

SVC	Simulator Potentiometer Settings							
	X_T	X_{TCR}	X_{LFC}			X_{CFC}		
	All Phases		A – B∅	B - C∅	C – A∅	A - B∅	B - C∅	C – A∅
Blackwater	9.82	4.60	0.95	0.95	0.95	2.43	2.43	2.43
Gregory	9.82	4.60	1.21	1.21	1.21	1.86	1.86	1.86
Mt McLaren	9.82	4.60	1.07	1.07	1.07	2.13	2.13	2.13
Dysart	8.35	2.94	0.83	0.83	0.83	2.75	2.75	2.75
Moranbah	5.04	1.88	0.71	0.71	0.71	3.15	3.15	3.15
Grantleigh	9.82	4.60	1.06	2.65	1.06	2.14	0.44	2.14
Dingo	8.35	2.94	1.61	0.69	0.69	1.27	3.21	3.21
Oonooie	5.04	1.88	0.44	0.46	0.59	4.46	4.19	3.63
Coppabella	5.04	1.88	0.36	0.44	0.44	5.02	4.46	4.46
Nebo	0.11	0.30	0.06	0.06	0.06	8.10	8.10	8.10

The simulated network can be loaded individually between each pair of phases, with both active and reactive power and may be varied between 0 and 100 MVA using potentiometers. The load may be measured on the instrument meter provided.

Connection of the ABB power system simulator to the SVC control system is achieved by attachment of the injection lead to plug sockets provided at the rear of the control system cubicle.

The SVC control system may be operated through the power system simulator via five push buttons on the front panel. In order to start the power system simulator the start button must be pushed and no trip signal detected from the SVC control system. If this condition is fulfilled the power system simulator sends a signal to the control cubicle, which responds by issuing a close command to the simulated SVC circuit breaker. The SVC control system is now on line and regulating the simulated power system.

If the simulator stop button is pushed, a signal is sent to the control cubicle which issues a SVC circuit breaker trip command. The simulated circuit breaker status is then changed to open and the control system is deactivated.

4.6 Required Skills

It has been identified that the following skills and knowledge must be developed to reach a successful project outcome:

- Familiarity with MATLAB Simulink and the associated SimPowerSys blockset. This is required to develop and operate the SVC control system model, and therefore obtain predicted responses.

- Understanding of the operation of the load balancing type SVC control system, from block diagram level to specific module functions.

- The ability to interpret the manufacturer's abridged schematics was required to obtain system parameters for theoretical modelling. This also required the ability to interpret abridged schematic functional blocks by comparison with available circuit diagrams.

- Familiarity with the ABB power system simulator, to configure the test set to suit the Blackwater supply system parameters and correctly simulate step unbalanced load to obtain control system responses comparable with those predicted.

- Ability to operate a Hioki 8826 high speed chart recorder and the associated proprietary wave viewing software. This is required to obtain measured SVC control system responses and import acquired data to computer for viewing, processing and comparison with theoretical responses for model validation.

- Import of experimental and theoretical data into MATLAB in a format allowing comparison. This is required to perform model validation.

4.7 Reporting

At the conclusion of model development and validation, reporting requirements for the successful completion of the research project must be achieved. This involves the collation, validity assessment and analysis of accumulated data, the formulation of conclusions and the preparation of the final report. Documentation of the model development, adaptation and validation procedure shall be performed as these procedures are performed.

The communication of experimental results shall include deviations from expected results and any such deviations noted shall be investigated as far as possible to identify probable cause. Reporting shall include a review of previous research pertaining to the topic and identification of future work required to achieve a solution to the identified problem. Aligning project outcomes attained with the specific objectives shall determine the level of achievement obtained, and this shall be clearly stated.

5. Control System Model Development

5.1 Background

The SVC control system determines the thyristor firing angle controlling the magnitude of the TCR current. This determines SVC susceptance and the magnitude of the reactive power injected to or absorbed from the power system to which the SVC is connected.

Modification of SVC control system settings while the system is on-line may result in discontinuity of voltage profile, SVC plant damage due to overvoltage or abrupt changes in thyristor firing angle, or worst case outcome is system instability and localized loss of supply. As indicated in Figure 5.1, a system disturbance occurred at 14:39:20 on 22 May 2004 due to a fault at Nebo Substation in North Queensland. The subsequent Northern and Central region transmission system disturbance resulted in a 132kV bus voltage dip at Blackwater substation and within 40 seconds the SVC controlled voltage become unstable and resulted in a complete loss of supply at Blackwater substation at 14:40:15 at the far right of Figure 5.1. The loss of supply data was not available for display.

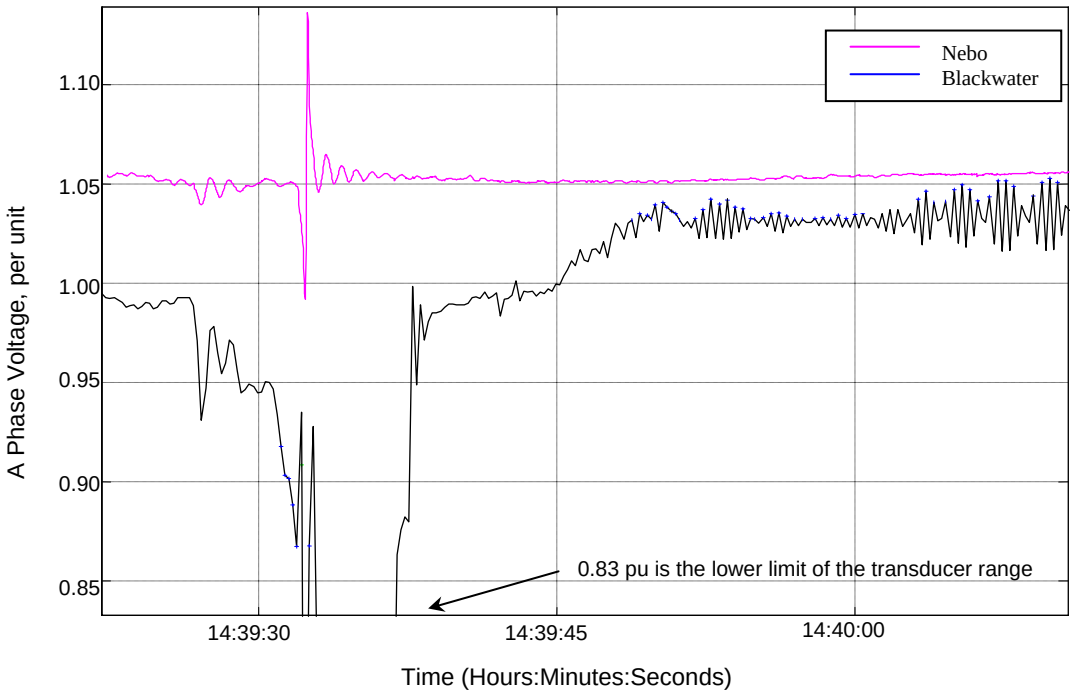

Figure 5.1: 132kV Bus Voltage at Nebo and Blackwater Substations, 22 May 2004.

Due to the undesirability of potential substation plant damage and litigation by the industrial customers supplied by this substation, it was deemed inadvisable to modify the SVC control system settings while the system remained on-line. The traditional method used to modify and validate control system settings was to remove the SVC from service for a period of approximately one week, to apply the settings and confirm suitability by performing a set of commissioning tests. During this process it sometimes became necessary to recalculate the control system settings if it became apparent that undesired side effects would result as a consequence of the proposed changes.

This process was unable to be applied at Blackwater substation SVC as it is the most heavily loaded in the Central Queensland region, and NPS levels rise above regulatory limits when it is out of service. For such a critical system, off-line time is restricted. Therefore a method to predict the impact of setting changes prior to application is required to enable control system changes to be made with confidence and reduce the validation time required.

The significant advantage in the development of a theoretical model representing SVC control system function was identified. As a consequence of this project, the Blackwater SVC control system model was developed and it is hoped that this model will eventually form part of a larger model reflecting the behaviour of the entire SVC.

5.2 Generic Control System Model

A generic SVC control system model developed by Mr. Paul Windle of Powerlink Queensland was made available for testing and modification. This model was constructed using the MATLAB Simulink SimPowerSys toolbox and was originally intended as an academic exercise to determine if such a model could be developed, but its function was never verified or validated.

Due to the requirement for load balancing type SVC control systems to use individual phase regulation, the generic control system model was large and complex as a result of the high degree of block interconnection. Since the model was intended as a purely academic exercise, no documentation existed to identify block type or function and labelling within the model was abbreviated, resulting in cryptic designations. The full top layer of the generic control system model requires one A3 size page to display and is contained in Appendix D.

5.2.1 Voltage Regulation

The critical control system model components are the three voltage regulation blocks, one for each delta connected phase of the TCR. The general layout is reproduced in Figure 5.2, with a more detailed version contained in Appendix D, Figure D.2 to allow viewing of specific functional blocks.

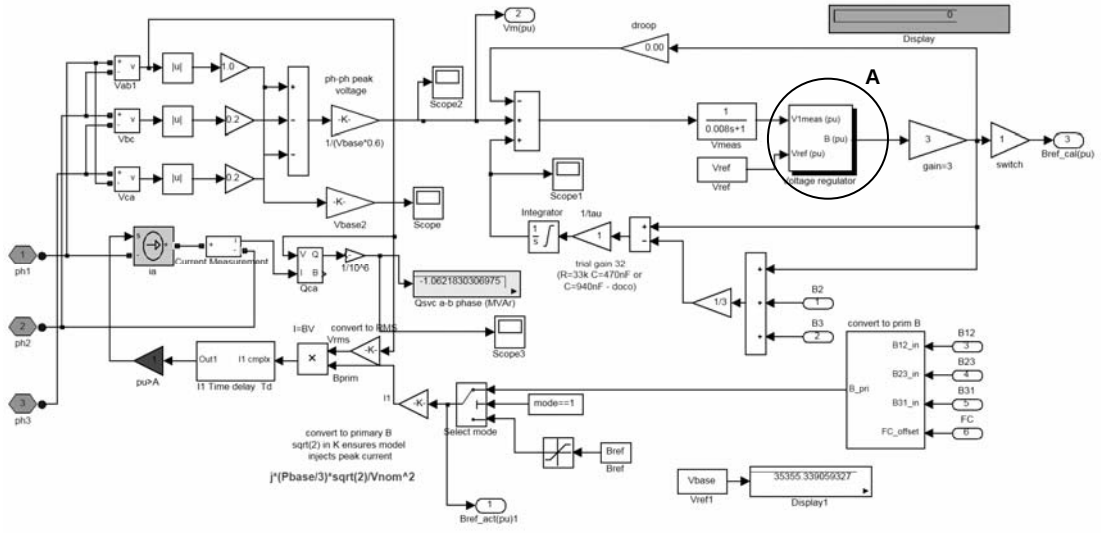

Figure 5.2: Generic control system model voltage regulation block A-B phase.

5.2.2 PI Controller

The block denoted A in Figure 5.2 of the previous page, is the PI controller block displayed in further detail in Figure 5.3. Measured voltage is compared to the set voltage reference point, with the error signal equal to the difference. The PI controller is used as the proportional element ensures fast response to large discrepancies between measured and set voltages, with the integral element ensuring no steady state error. This block originally included the algorithm to calculate droop or slope of the SVC, previously defined as allowable voltage variation at full SVC susceptance output, however this was disabled by breaking the algebraic loop after failing to function correctly (Windle, P. 2005 pers. comm., 14 Jun).

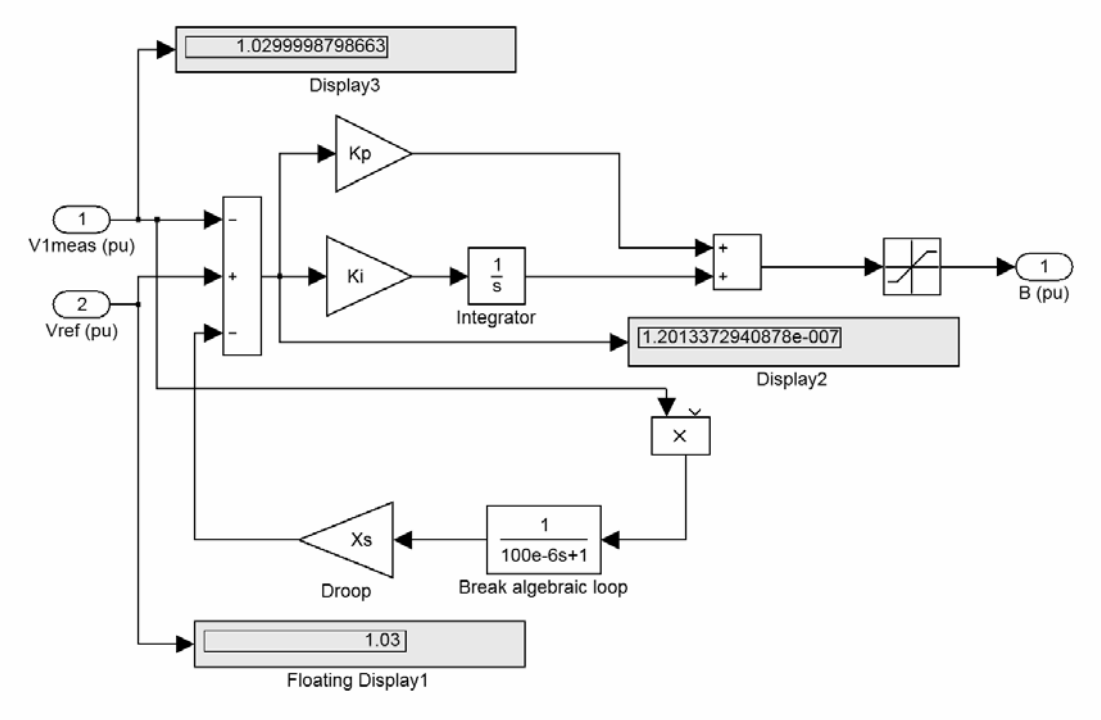

Figure 5.3: Generic model voltage regulation PI controller block A-B phase.

5.2.2 Control signal generation

The final major functional model block implements the Steinmetz equations for open loop load balancing, and converts the calculated secondary susceptance values to primary system values, allowing for the phase shift of the SVC transformer vector group. This is performed by summating a linear combination of the delta connected phase susceptance magnitudes and applying a gain of one third. The fixed capacitor offset is applied to compensate for the effects of the filter capacitance, allowing for the additional inductance required to achieve the target output susceptance. Functional block detail is displayed in Figure 5.4.

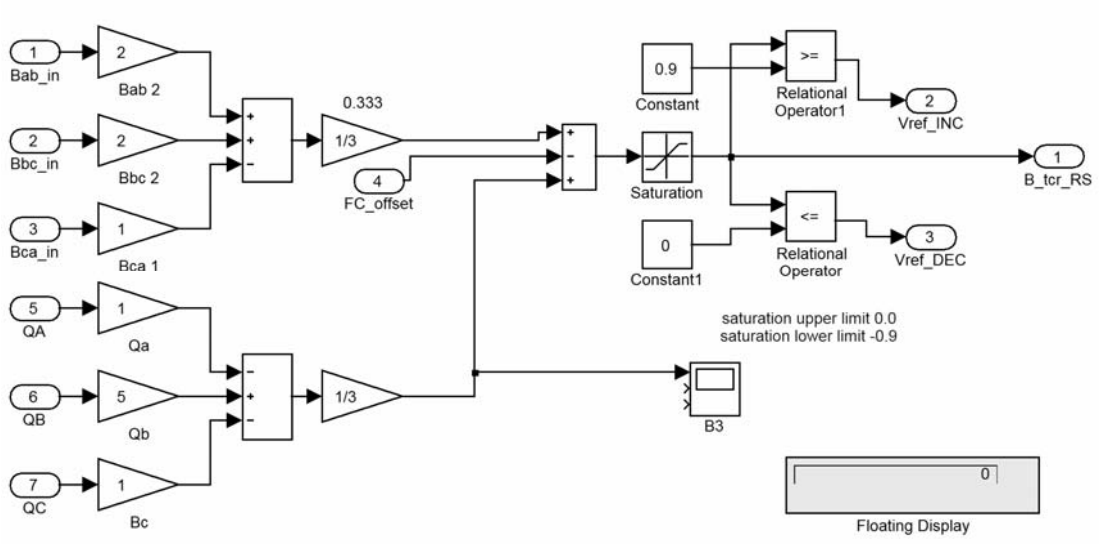

Figure 5.4: Generic model interface and steinmetz block A-B phase.

5.2.4 System load

Simulated power system loading may be presented to the model via delta connected resistances as displayed in Figure 5.5, individually definable through the block parameters. The load base is 10 MW. Due to the high power factor of train loads, it was not deemed necessary to incorporate reactive loads in the system load mode (ABB 1999a).

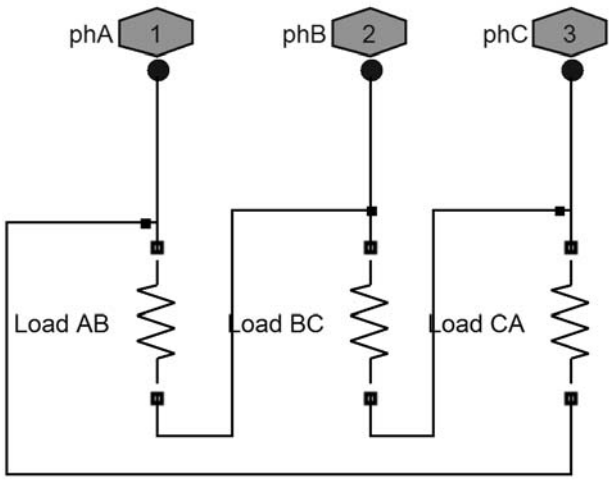

Figure 5.5: Control system model three phase load.

The control system model available details the functions prior to the thyristor firing circuitry, producing a susceptance value output. Therefore the theoretical analysis will focus on the control system elements impacting this output or those parameters significantly altered for the Blackwater site.

5.3 Blackwater SVC Control System Model

The model reference set points, inputs and gains were modified to reflect the Blackwater SVC control system settings. Some functionality included in the generic model was not required to simulate the Blackwater system, and this was removed to simplify the model.

5.3.1 System Load

The system loading of specific interest within the scope of this project is voltage imbalance, most significantly resulting from single phase high voltage loading presented by electric trains. Each locomotive is rated at 3.3 MVA and has a power factor of 0.95 or higher (ABB 1999a). A fully loaded coal train comprises four locomotives, resulting in a total load of 13.2 MVA.

These quantities are converted to a per-unit base suitable for input to the control system model. The power system base defined as

$$MVA_{BASE\ 3\phi} = 100 \text{ MVA},$$

and therefore the single phase base for per-unit calculations is

$$MVA_{BASE\ 1\phi} = 33.33 \text{ MVA}.$$

Calculating load presented by a fully loaded train in per-unit quantities gives a per-unit apparent power of

$$S = \frac{MVA_{LOAD\ 1\phi}}{MVA_{BASE\ 1\phi}} = 0.3960 \text{ per unit}, \qquad (5.1)$$

adjusted to obtain a real load power of

$$P = S \cos\theta = 0.3762 \text{ per unit}. \qquad (5.2)$$

Allowing for a maximum three phase load of 60 MW that may exist before the train loading is added, determined from site metering data, balanced phase load was set in the model at 0.2 per unit per phase. As it was advised to limit model input loading to no greater than 0.5 per unit (Windle, P 2005, pers. comm.., 10 August), the unbalanced phase load magnitude was set at 0.5 per unit.

Therefore the load presented to the control system model was set at 0.5 per unit for the unbalanced phase and 0.2 per unit for the other two phases. It was determined that this loading should represent the absolute worst case loading presented to the Blackwater SVC.

5.3.2 Voltage Reference

The SVC control system settings sheet number 41 issued 15 July 1998 by the Queensland Electricity Corporation (QEC) for Blackwater substation is a controlled document, and should accurately reflect the actual control system settings applied. Appendix E contains a copy of the SVC control system settings sheet.

As per the setting sheet the SVC voltage reference V_{SET} is 134 kV. As the system base voltage is 132 kV, this equates to

$$V_{pu} = \frac{V_{SET}}{V_{BASE}} = 1.015 \text{ per unit}. \qquad (5.3)$$

The setting sheet specifies that the Steinmetz controller is selected to off, allowing all voltage regulation to be performed by the closed loop algorithm.

5.3.3 SVC Slope

SVC slope is selectable in ten increments of 0.4 %, representing the range 0 – 4 %. The setting sheet specifies that Blackwater SVC slope be set equal to 0, that is, 0 %. Therefore the associated control system blocks may be deleted to allow simplification of the model.

5.3.4 Fixed Capacitor Offset

The principle of SVC control system operation is that when the reference susceptance signal output from the voltage regulation card, B_{REF}, is equal to 0 V, the net SVC output susceptance shall be zero (ASEA 1986, p. 20), that is, presenting an infinite reactance to the network. For the SVC output to be zero, the system voltage must equal the set voltage resulting in the fixed capacitor and TCR susceptance values equal in magnitude but opposite in sign. Within the control system, the fixed capacitor offset voltage is chosen so that TCR susceptance equals the fixed capacitor bank susceptance when $B_{REF} = 0$, indicated by point FC in Figure 5.6. This fixed offset value allows the control system to compensate for the effects of the fixed capacitor when calculating the TCR current required to achieve the calculated SVC susceptance. When the SVC operates at its maximum inductive output, the thyristor firing circuit control signal voltage U_s, representing the desired SVC output susceptance, has a value of 9.2 V.

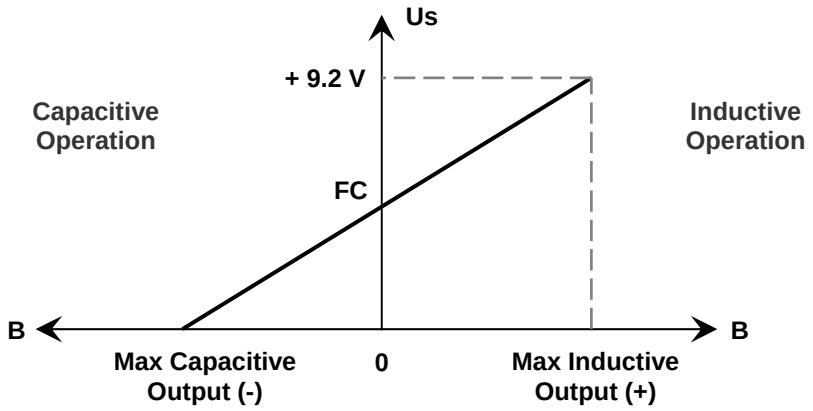

Figure 5.6: Fixed Capacitor Offset.

To calculate the fixed capacitor offset requires the susceptance of the reactors and the fixed capacitor bank, configured as a tuned filter, to be evaluated. The reactors are connected in delta and the fixed capacitor star connected, therefore to compare the susceptances the filter reactance values must be converted to the equivalent delta connected system for analysis.

Individual component values are indicated on the extract from the Blackwater SVC construction schematic displayed in Figure 5.7.

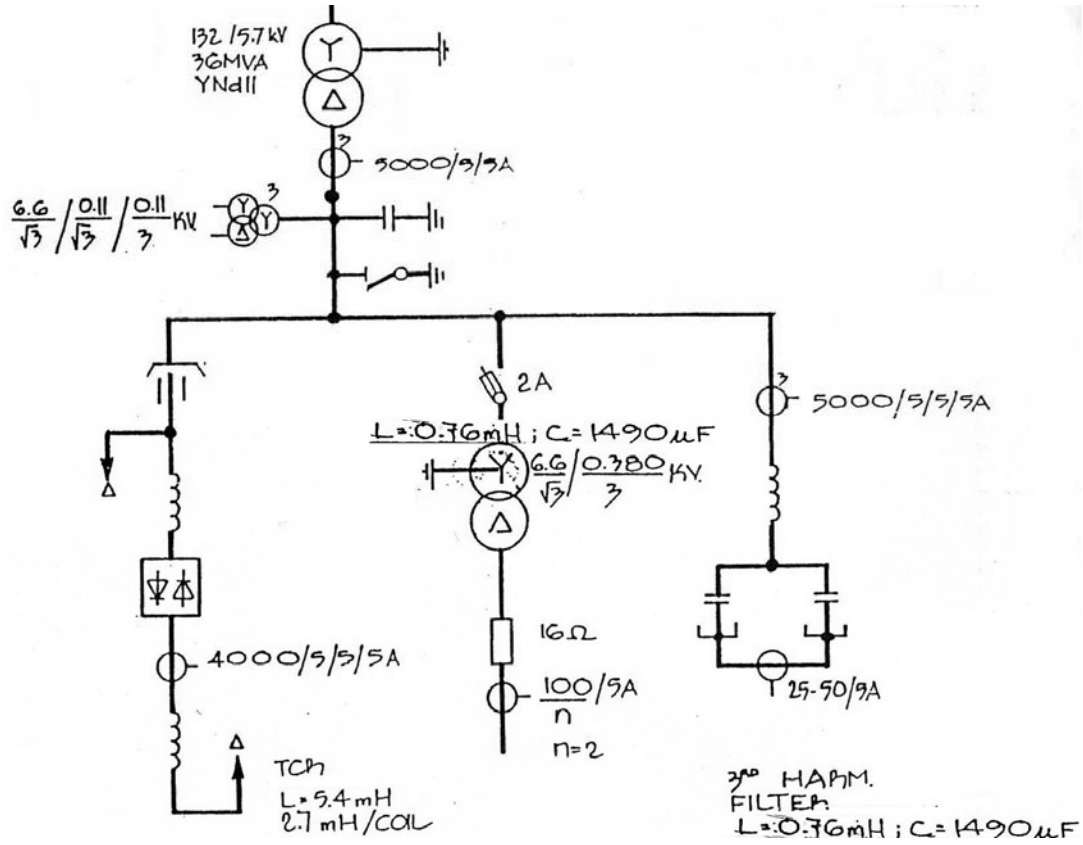

Figure 5.7: Blackwater SVC component values (QEC 1992).

Using the convention that inductive reactance is positive and capacitive reactance negative, and assuming ideal components, the SVC component susceptance values are calculated as follows.

TCR Inductance per phase is given in Figure 5.7 as

$$L = 5.4 \times 10^{-3} \text{ H},$$

therefore inductive reactance is calculated as

$$X_L = 2 \pi f L = 1.6965 \ \Omega \qquad (5.4)$$

per phase.

As susceptance is the inverse of reactance, that is,

$$B = \frac{1}{X}, \tag{5.5}$$

TCR susceptance is calculated as

$$B_{TCR} = 0.5895 \text{ S.}$$

The fixed capacitor is constructed as a tuned filter as indicated in Figure 5.8.

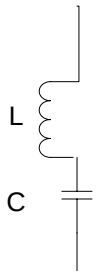

Figure 5.8: Single phase of SVC tuned filter.

Component values are given in Figure 5.7 as an inductance of

$$L = 0.76 \times 10^{-3} \text{ H}$$

and a capacitance of

$$C = 1490 \times 10^{-6} \text{ F}$$

for each star connected phase.

The net filter reactance will be the difference between the capacitive and inductive component reactances, calculated as

$$X = X_L - X_C \tag{5.6}$$
$$= 2\,\pi\,f\,L - \frac{1}{2\,\pi\,f\,C}$$
$$= -1.8975\ \Omega$$

per phase, the negative sign indicating that it is capacitive reactance.

Converting from star connection to a delta configuration uses the relationship

$$X_{ab} = X_a + X_b + \frac{X_a\,X_b}{X_c}\ , \tag{5.7}$$

(Sharma 2005, p. 17) where X_{ab} represents the delta connected reactance between A and B phase and X_a, X_b and X_c represent each of the star connected reactance values. As the filter is balanced, all phase reactance values are equivalent and the relationship reduces to

$$X_{ab} = 3\,X_a = -5.6926\ \Omega. \tag{5.8}$$

All three delta connected reactance values will be equal, therefore it is sufficient to calculate one only. Phase susceptance of the fixed capacitor is calculated as

$$B_{FC} = -0.1757\ \text{S},$$

with the negative sign signifying a capacitive susceptance.

When the TCR is operating at its maximum output, the output susceptance of the SVC is the difference between the TCR and fixed capacitor susceptance values. That is,

$$B_{SVC} = B_{TCR} + B_{FC} \tag{5.9}$$
$$= 0.4138\ \text{S}.$$

When the TCR current is zero, the SVC susceptance is determined solely by the fixed capacitor and

$$B_{SVC} = B_{FC} .$$

Therefore the required fixed capacitor offset equals the thyristor firing signal voltage level U_s when B_{REF}, is equal to 0 Volts and is calculated using the voltage divider rule as

$$U_S = 9.2 \times \left| \frac{B_{FC}}{B_{TCR} - B_{FC}} \right| \qquad (5.10)$$

$$= 2.7417 \text{ V.}$$

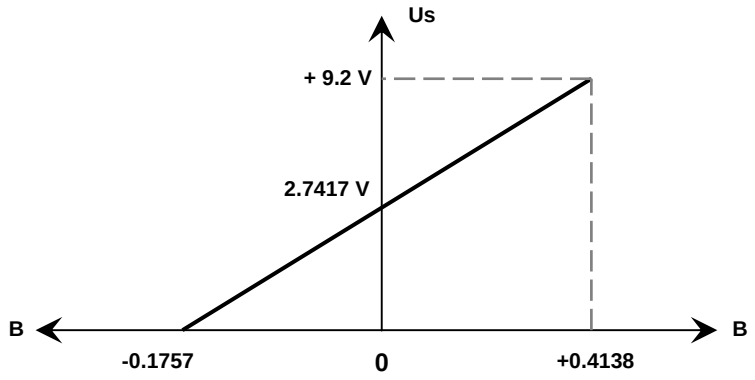

Figure 5.9: Calculation of fixed capacitor offset value.

Figure 5.9 illustrates the relationship between the thyristor firing signal and susceptance signal voltage levels. As the control system model uses per unit quantities, and ten volts equates to 1.0 per unit in the SVC control system (ASEA 1986, p. 8), the required fixed capacitor offset value is 0.2742 per unit.

5.3.5 Voltage Response

As the control system voltage regulation card is a signal processing device composed mainly of operational amplifiers, the manufacturer has chosen the gain of these devices to ensure that the signals input to, or output from any amplifier remain within the acceptable range of that device. Very little detail was available within the manufacturer's documentation regarding individual circuitry components and function with the exception of some scaling factors relating test point measured voltages to a one per unit input. Verification of amplifier gains applied within the model voltage response and reference circuits prior to PI controller input is required to ensure accuracy. This shall be performed by simulation in MATLAB.

Manufacturer's documentation states that the voltage regulation card YXR 206A summates the rectified input voltage for the regulated phase with 20% of the inverted rectified voltage input from the remaining two phases. This proportional reduction is performed to allow the three voltage regulation cards to operate independently (ASEA 1986, p. 16). For example, where $|UAB|$, $|UBC|$ and $|UCA|$ represent the rectified voltage inputs to the SVC control system voltage regulators, the A – B phase voltage regulation card will summate the inputs in the proportions

$$1.0\ |UAB| \ - \ 0.2\ |UBC| \ - \ 0.2\ |UCA|$$

as shown in Figure 5.10, an extract from the abridged schematic (Appendix C, Figure C.3).

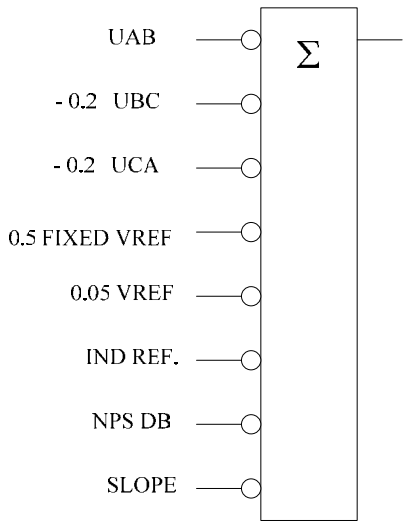

Figure 5.10: A – B phase voltage regulation card YXR 206A summing junction.

The summing junction output is ΔU , the difference detected by the control system between the measured and set voltages, producing an average zero output if the input voltage and set point voltage are identical. Output from the summing junction will be negative in magnitude if the measured voltage is less that the reference and positive if it exceeds the reference.

As the supply voltage of the summing junction amplifier is ± 15 V (ASEA 1986, p. 7) the operational range of the device will be within these limits and may be exceeded by a linear combination of the rectified voltages $|UAB|$, $|UBC|$ and $|UCA|$ in the proportions stated in the manufacturer's documentation.

Manufacturer's documentation states that the FIXED VREF input signal shown on the YXR 206A abridged schematic (Appendix C, Figure C.3), is 10V in magnitude but reduced by half when summated (ASEA 1984, p. 17). The VREF signal represents the variation of the SVC set voltage from 1.0 pu where 10 V represents 0.1 pu variance such that a set voltage of 1.03 pu equals a VREF of 3 V. This input is applied at 10% of the FIXED VREF gain (ASEA 1984, p. 17), that is, applied with a gain of 0.05.

Let the peak amplitudes of |UAB|, |UBC| and |UCA| be equal. If the phase to phase voltages are 1.0 pu in magnitude and the SVC set voltage is 1.0 pu, that is VREF is 0, the output from the summing junction will also be 0. Therefore, a scaling factor x must be obtained such that a linear combination of these voltages equals the combined fixed reference voltage and reference voltage signals. The required relationship is represented as

$$x\ |UAB| - 0.2\ x\ |UBC| - 0.2\ x\ |UCA| = 0.5\ FIXED\ VREF + 0.05\ VREF$$

resulting in a calculated x of 1.6.

Therefore the measured and rectified input voltages to the SVC control system voltage regulation circuits must be combined in the proportions

$$1.6\ |UAB| - 0.32\ |UBC| - 0.32\ |UCA|$$

for the A – B phase voltage regulator.

The inductive reference signal, IND REF, shown as an input to the summing junction in Figure 5.10 on page 78, is only utilised during SVC start up process where the thyristors are forced to fully conduct for the first second of operation. As this is not within the scope of the project this signal is disregarded. The slope of Blackwater SVC control system is set to 0% as discussed in section 5.3.3, and this input need not be considered. As formulated in the experimental methodology, the control system NPS deadband is to be set to 0% for testing purposes, therefore this input may also be disregarded. The linear combinations required to model the function of the summing junction have now been defined and may be simulated.

The output of the summing junction corresponding to voltage regulation card YXR 206A test point TP12 is related to the magnitude of input, with the scale 4.98 V equalling 1.0 pu (ASEA 1984, p. 16). Test point TP13 is also assigned a scale of 3.32 V equalling 1.0 pu.

As can be seen from the voltage regulation card abridged schematic (Appendix C, Figure C.3), test point TP12 is located prior to TP13 in the circuit. Therefore as both scaling factors relate to a 1.0 per unit signal, the gain A of the amplifiers between the two test points must be the ratio of the two scaling factors, that is,

$$A = \frac{2}{3}.$$

The circuit diagram in Figure 5.11 is an extract from a YXR 206A schematic found at the Blackwater SVC site (Appendix C, Figure C.1) and represents the integrator and sample and hold functions located immediately after the summing junction.

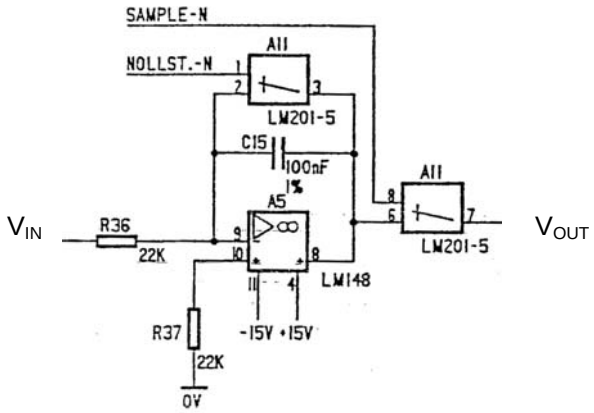

Figure 5.11: Voltage regulation card YXR 206A integrator, sample and hold circuit.

From Figure 5.11, the gain of the inverting amplifier is determined by the resistor R_{36} and capacitor C_{15}. Considering an input voltage signal V_{IN} of 5 V and assuming that the amplifier is capable of infinite gain, the current flowing through R_{36} may be calculated by application of Ohm's Law.

$$I = \frac{V_{IN}}{R_{36}} = 2.27 \times 10^{-4} \text{ A} \quad (5.11)$$

The sampling time of the circuit is 10×10^{-3} s (ASEA 1986, p. 16), that is, output will be obtained from the integrator for 10 ms before resetting. Therefore charge is calculated as

$$Q = I \,.\, t = 2.27 \times 10^{-6} \text{ C} \quad (5.12)$$

Assuming that the amplifier is ideal and has infinite input impedance, all current flowing through resistor R_{36} must flow through capacitor C_{15}. As charge is also defined as

$$Q = C \,.\, V \,, \quad (5.13)$$

amplifier output voltage V_{OUT} may be calculated as

$$V_{OUT} = 22.73 \,.$$

That is, for a 5 V input signal, the output will be 22.73 V. Therefore the closed loop gain A_{CL1} of the integrator is calculated as

$$A_{CL1} = -\left(\frac{V_{OUT}}{V_{IN}}\right) = -4.55 \,. \quad (5.14)$$

As per the YXR 206A circuit schematic (Appendix C, Figure C.3) an additional amplifier prior to the test point TP13 exists as displayed in Figure 5.12.

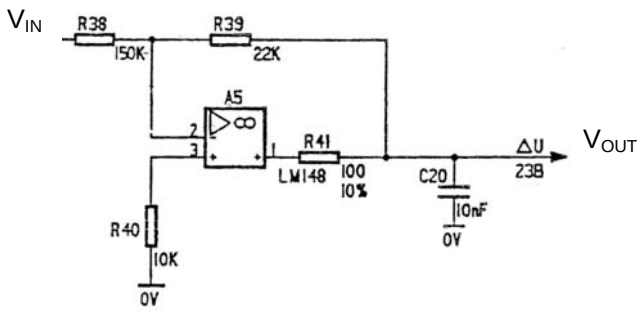

Figure 5.12: Voltage regulation card YXR 206A gain circuit.

From Figure 5.12, the gain of the inverting amplifier is determined by the resistors R_{38} and R_{39}. Assuming that the amplifier is capable of infinite gain, the closed loop gain A_{CL2} of the inverting amplifier gain may be calculated as

$$A_{CL2} = -\left(\frac{R_{39}}{R_{38}}\right) = -0.1467 \qquad (5.15)$$

Therefore the overall amplifier gain between the test points TP12 and TP13 located on voltage regulation card YXR 206A will be the product of these two gains, that is,

$$A = A_{CL1} \,.\, A_{CL2} = \frac{2}{3} \,. \qquad (5.16)$$

This verifies that the application of amplifier gains within the control system model voltage regulation module conform to manufacturer's specifications and the output gain of the model voltage response subsystem will be set to 1.5.

Using the amplifier gains and required linear combinations calculated, the MATLAB script replicated in Appendix H.3 was formulated to simulate the voltage reference and response circuits prior to the PI controller input on voltage regulation card YXR 206A. This code was configured to have the capability of importing experimental data to perform the same simulation operations and directly compare the predicted voltage response of the actual voltage inputs with response measured.

5.3.6 PI Controller

Information regarding the PI controller was not readily available in the manufacturer's documentation. As previously mentioned, some abridged schematics and circuit diagrams were available but individual components were difficult to identify. Using the abridged schematic for the YXR-206A card (Appendix C, Figure C.3) and determining component values from the card circuitry resulted in the representation of the inverting amplifier with PI control in Figure 5.13, excluding the switching circuitry.

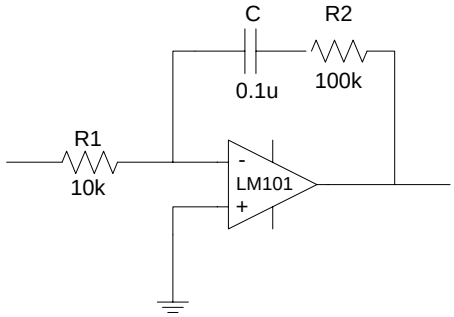

Figure 5.13: Voltage regulator PI controller.

This is identified as an active RC lead-lag integrator (Stanley 1994, p. 139). The voltage regulator card YXR-206A gain setting dial selects a value for resistor R_1. When the gain is set to 6 as specified on the setting sheet contained in Appendix E, R_1 is selected as 10 kΩ.

The values identified in the card circuitry are

$$C_2 = 0.1\ \mu\text{F}$$

and

$$R_2 = 100\ \text{k}\Omega\,.$$

The circuit time constants, τ_1 and τ_2, may be calculated as

$$\tau_1 = CR_1 = 1.0\ \text{ms} \tag{5.17}$$

and

$$\tau_2 = CR_2 = 10\ \text{ms}\,. \tag{5.18}$$

This allows the associated transfer function $G(s)$ of the active RC lead-lag integrator to be represented as

$$G(s) = \frac{1+s\tau_1}{s\tau_2} = \frac{1+0.001s}{0.01s} \tag{5.19}$$

(Stanley 1994, p. 139). The bode plot of the lead-lag integrator is included in Appendix F, Figure F.7.

This transfer function may be rearranged to yield the standard form of a PI controller.

$$G(s) = \frac{\tau_1}{\tau_2} + \frac{1}{\tau_2 s} = K_P + \frac{K_i}{s} \tag{5.20}$$

The proportional gain of the controller is determined by the resistors R_1 and R_2 such that

$$K_p = \frac{R_2}{R_1} = 10 \ . \tag{5.21}$$

The integral gain of the PI controller is determined by the resistor R_1 and capacitor C as

$$K_i = \frac{1}{\tau_2} = 100 \ . \tag{5.22}$$

Insufficient information existed to model the PI controller parameters with confidence due to the presence of additional switching circuitry. The calculated values of

$$K_p = 10$$

and

$$K_i = 100$$

will be adopted as the model defaults and alterations made to match the parameters to the actual control system response after experimental test results are obtained if time permits.

5.4 Theoretical Results

5.4.1 Voltage Response

A 50 Hz sinusoidal three phase voltage input of 1.0 per unit amplitude was input to the regulator voltage response simulation (Appendix H.3) developed to allow verification of the outputs. Simulation of the theoretical operation of the active rectifier and summing junction of the SVC voltage regulation card YXR 206A obtained the waveform in Figure 5.14.

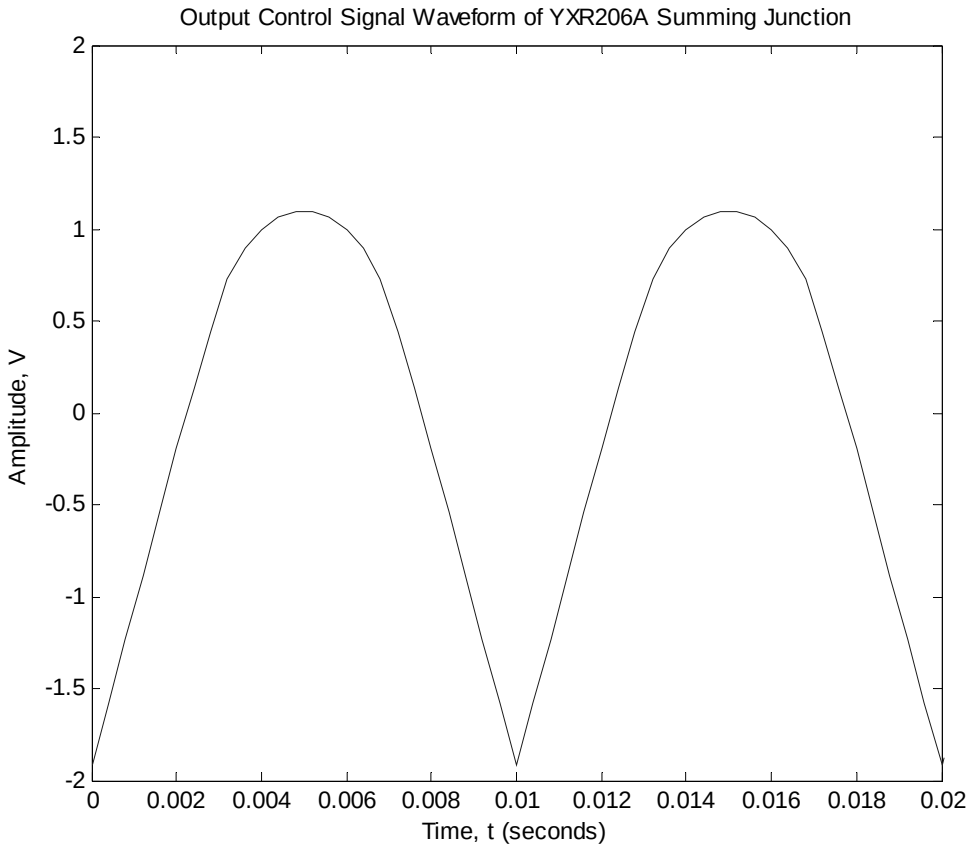

Figure 5.14: One cycle simulation of YXR 206A test point TP12.

As the measured and SVC set voltage are identical, the average value of test point TP12 should be zero. The simulation output was configured to determine the average of the summing junction output (TP12) and was calculated as

```
Average of Summing Junction output = -0.004283.
```

This is sufficiently close to zero considering errors introduced by the coarse sampling rate as discussed in the MATLAB code documentation in Appendix H.3. As observed previously in Figure 5.14, rectification of the control system voltage inputs introduces 100 Hz ripple into the control signal voltage input to the voltage regulator and the elimination of this ripple is the purpose of the integrator, and sample and hold circuitry (ASEA 1984, p. 16).

Simulation of the theoretical operation of the integrator and sample and hold circuits of the SVC voltage regulation card YXR 206A obtained the waveform in Figure 5.15. Variation in amplitude is sufficiently small that it cannot be displayed accurately on the graph axes.

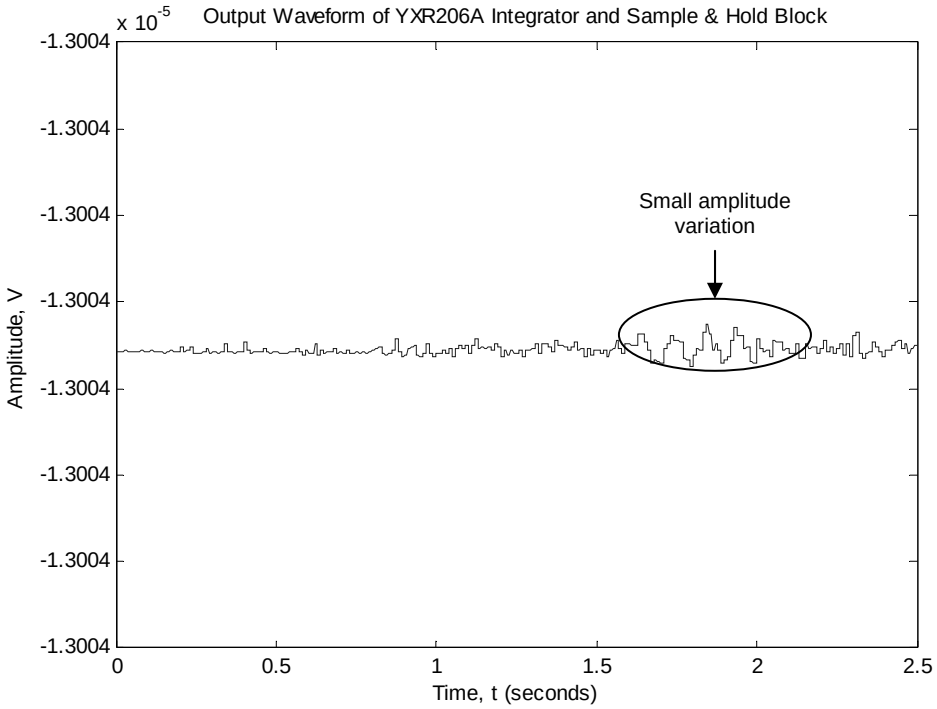

Figure 5.15: One cycle simulation of YXR 206A test point TP13.

The control signal voltage input to the PI controller, measured at test point TP13, should be equal to zero as the SVC set and measured voltages are the same. This was calculated as

```
Average of Integrator and S&H output = -0.000013.
```

which is deemed of acceptable accuracy. Therefore the voltage response simulation of the SVC control system voltage regulation card YXR 206A produces the expected results.

5.4.2 Unbalanced Load Response

As determined in section 5.3.1, an unbalanced load of 0.5, 0.2 and 0.2 per unit was connected to the control system model, representing load on A-B, B-C and C-A phases respectively. Step unbalanced load input to the control system model indicates that for a 50 Hz frequency power system, that is, a sinusoidal waveform cycle time of 20 ms, the SVC control system should exhibit a 2 cycle response time with minimal overshoot and no instability. Figure 5.16 demonstrates the response of the voltage regulator card YXR-206A calculated susceptance response to the application of step unbalanced loading.

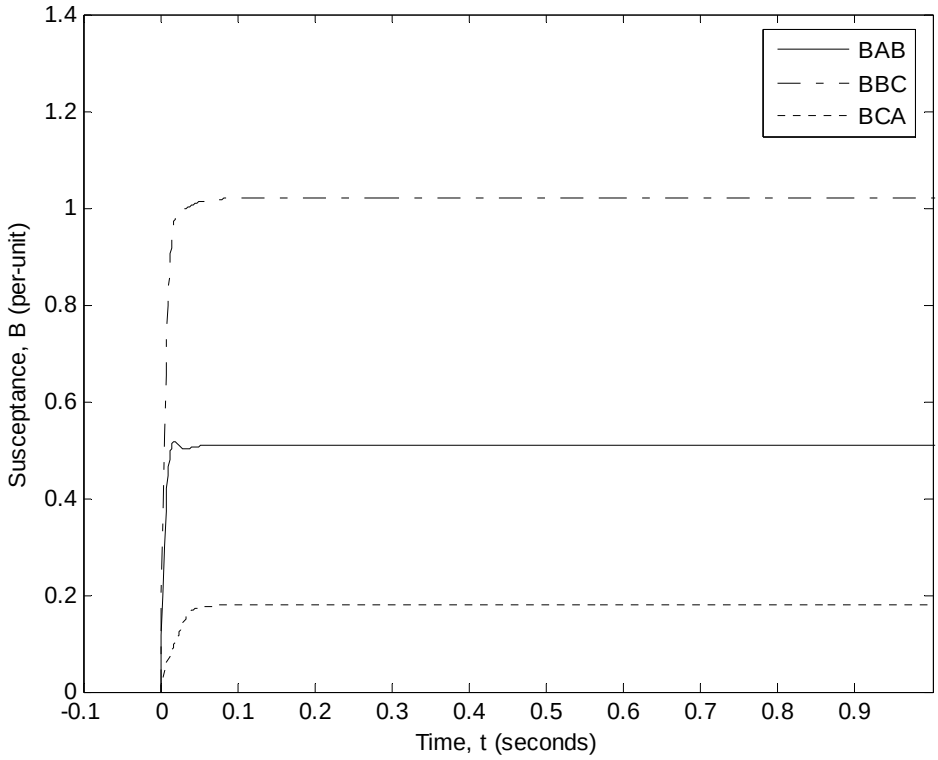

Figure 5.16: Voltage regulator calculated susceptance response to step unbalanced loading.

Figure 5.17 demonstrates the response of the control signal voltage U_S representative of the desired SVC output susceptance after all phase shift transformations and fixed capacitor offset have been applied. This signal determines the firing angle of the thyristors and thus the TCR current.

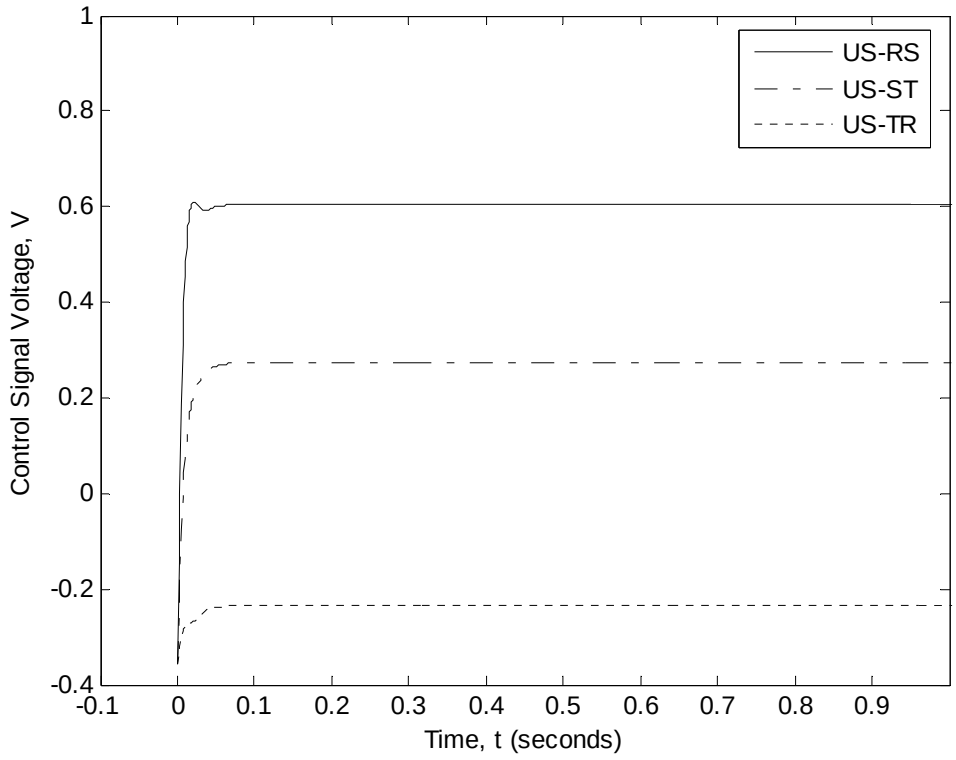

Figure 5.17: Control signal voltage U_S response to step unbalanced loading.

Other waveforms representing theoretical responses to step unbalanced loading, and the effect of alteration of PI controller parameters on response, are contained in Appendix F.

The control system model developed is very basic in function and could not simulate initial unbalanced conditions. This is a major difference between theoretical and experimental results, as the real world is rarely balanced. In addition, measuring element transmission delay was not incorporated for many of the minor components, contributing to possible inaccuracy of response.

Therefore validation of the model or identification of modifications to improve accuracy of theoretical responses required comparison with actual control system responses to step unbalanced loading.

6. Experimental Results

To validate the response to step unbalanced load obtained from the developed control system model, and thus the model itself, it was determined that comparison of the theoretical responses with actual SVC control system response to identical load conditions was to be performed. Access to the SVC for control system testing was rescheduled from the anticipated June 20th to May 31st by the Network Switching Centre (NSC) due to forecast system load. This necessitated a change in project sequence as activities associated with control system modelling were not yet complete.

On the 26th of May 2005 the SVC thyristor control circuits developed a fault, resulting in SVC failure and reducing the allocated testing period from the original four days, to one day after the necessary repairs were performed. Measurement of the Blackwater SVC control system response to unbalanced loading was performed on the 2nd of June 2005.

6.1 Measurement of Control System Response

Figure 6.1 shows the connections made to the control system during measurements. The connections to the control system were made through 2mm pin connectors to the buffered measurement points located on the front interface of the individual control system modules.

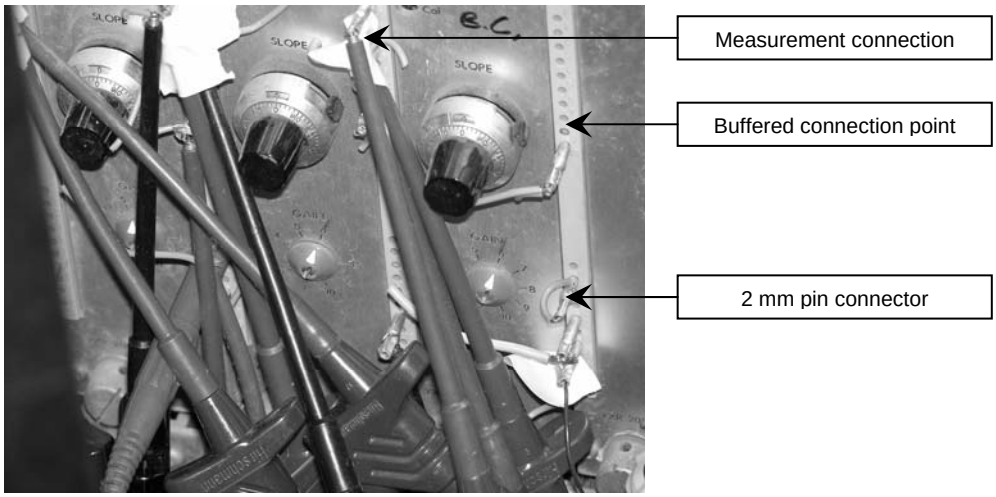

Figure 6.1: Connection of measurement leads to voltage regulation card YXR-206A.

Upon inspection, the buffered measurement points consisted of a light plastic clamp pressing the test connector against a piece of circuit track, resulting in test connections of unpredictable integrity. This resulted in loss of channel data numerous times during testing.

Response measurement required the input of voltages and currents to the measuring elements of the control system such as to replicate the unbalanced load used in the model simulation. This was accomplished using the ABB simulation test set, capable of replicating the single phase traction loading effect on the power system as detected by the SVC measurement systems, that is, the current and voltage transformer secondaries with load magnitude specified as a per-unit quantity. The test was configured so that a balanced three phase load was applied, and SVC control system steady state achieved, prior to application of the unbalanced load. The load simulator is connected at the rear of the control system panel as shown in Figure 6.2 to inject current and voltage to simulate unbalanced load.

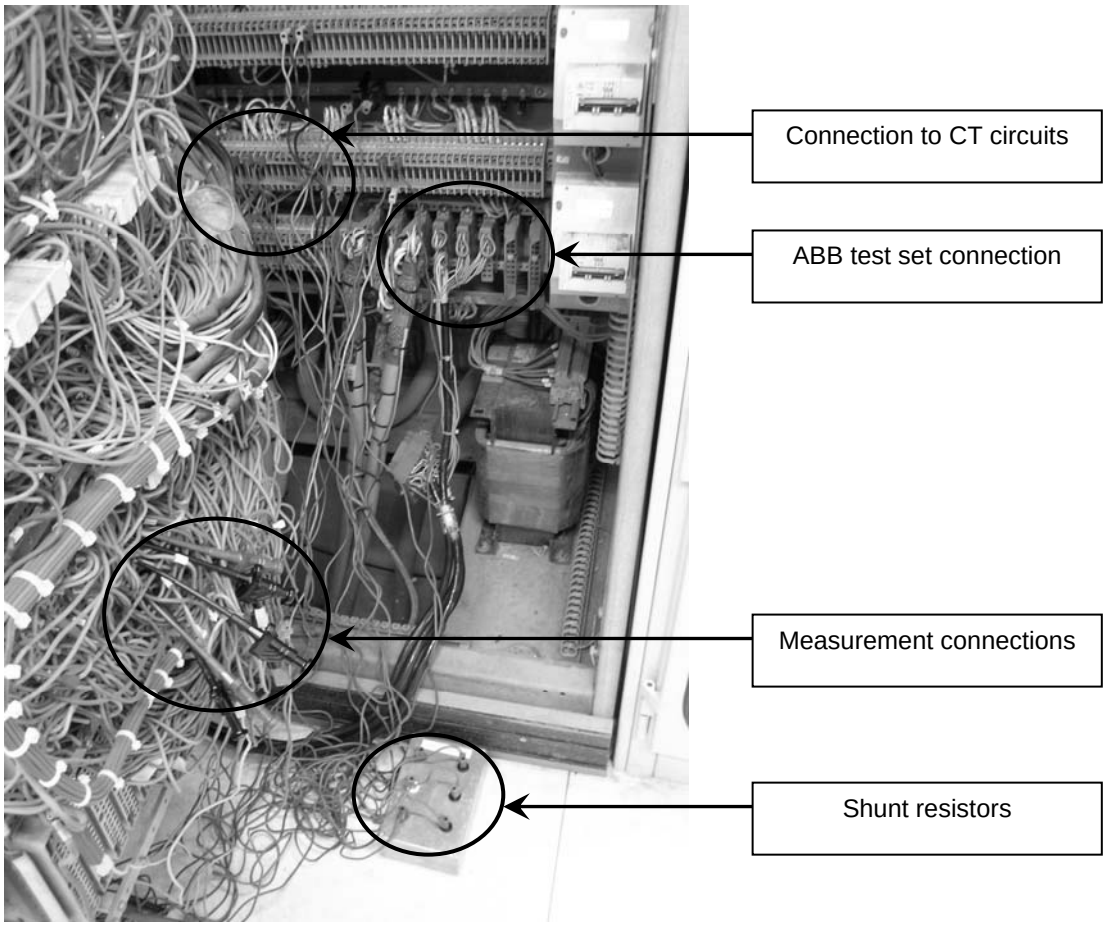

Figure 6.2: Connection of ABB test set to SVC control system.

It was identified that 29 individual measurement points were required to record all response details necessary to perform model validation or to determine control system settings and parameters for those elements for which information was unavailable, such as the PI controller. These measurement points are identified in Appendix C, Table C.1.

To capture the waveform information required on a common time base, a 32 channel Hioki high speed chart recorder was utilised as shown in Figure 6.3. The Hioki model 8826 chart recorder used is provided with software allowing import and viewing of waveform data on a computer.

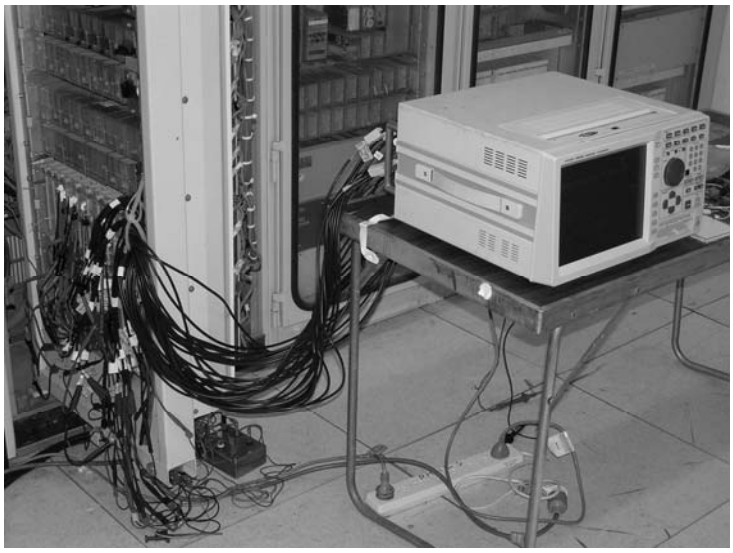

Figure 6.3: Connection of Hioki chart recorder to the SVC control system.

Control system response waveform information was recorded for a period of two seconds, incorporating a half second of pre-fault information. This allowed the steady state, unbalanced loading and de-loading conditions to be observed and recorded. Triggering was chosen as 5 % of the C – A phase voltage regulator susceptance waveform BCA, measured at YXR 206A card 3 test point 1 (Appendix C, Figure C.3), as it provided more consistent triggering at a lower waveform percentage.

Fixed capacitor offset is determined by the setting of the potentiometer unit QAPG 212. This is a DC voltage level, measured using a Fluke 87 series III multimeter at test point 17 on QAPG 212 card A and test points 4 and 17 on QAPG 212 card B as indicated in Appendix C, Figure C.6.

Initial measurements of the fixed capacitor offset gave results differing by up to 0.3 Volts. This was incorrect as the fixed capacitor installation at Blackwater SVC is balanced, therefore all three values should be identical.

As no information was available to indicate the correct offset value, it was adjusted so that all three values assumed the midpoint of the measured range, and the change noted in the maintenance records.

After adjustments, the fixed capacitor offset DC voltage levels were measured as:

- - 3.545 Volts for A-B phase;
- - 3.544 Volts for B-C phase, and
- - 3.545 Volts for C-A phase.

However, it remains for the adjusted fixed capacitor offset levels to be approved by the Powerlink Queensland Transmission Grid Planning division, as no documentation was available on site to verify the choice of setting.

6.2 Waveforms

Step unbalanced loading to the SVC control system was simulated and the resultant control system response measured. An example of the waveform obtained for the voltage regulation card output susceptance is displayed in Figure 6.4.

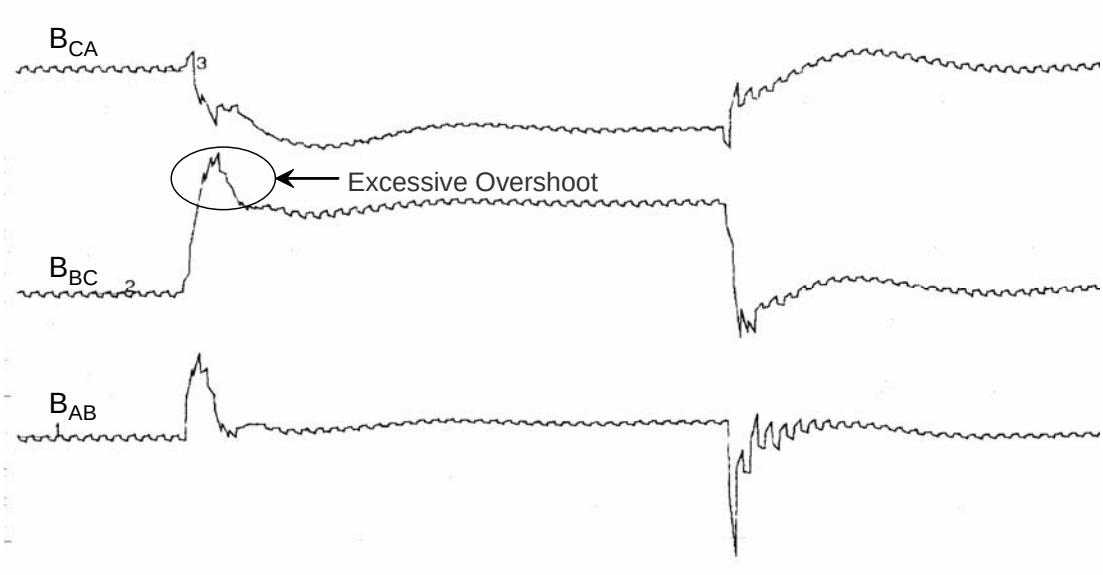

Figure 6.4: SVC control system measured susceptance response to load imbalance.

Prior to and after the SVC was returned to service, several manually triggered waveform measurements were captured and the data saved to magnetic disk for retrieval and processing during the model validation process, for ease of comparison with theoretical responses.

The waveforms obtained in response to step unbalanced loading indicate that using the specified settings, unstable control system response may occur. Figure 6.5 shows an example of the excessive overshoot and oscillation that occurred during some of the testing. Instability of control system response was more clearly observed during the removal of load. This phenomenon assists in explaining why SVC instability was observed during the system disturbance detailed in section 5.1. The fault at Nebo substation resulted in load shedding due to a drop in system frequency, separating the Northern and Central regions. This effectively de-loaded the Blackwater SVC which only then exhibited instability.

Although response time was measured as approximately 20 ms or one cycle, excessive overshoot was observed indicating that the control system gain is set too high.

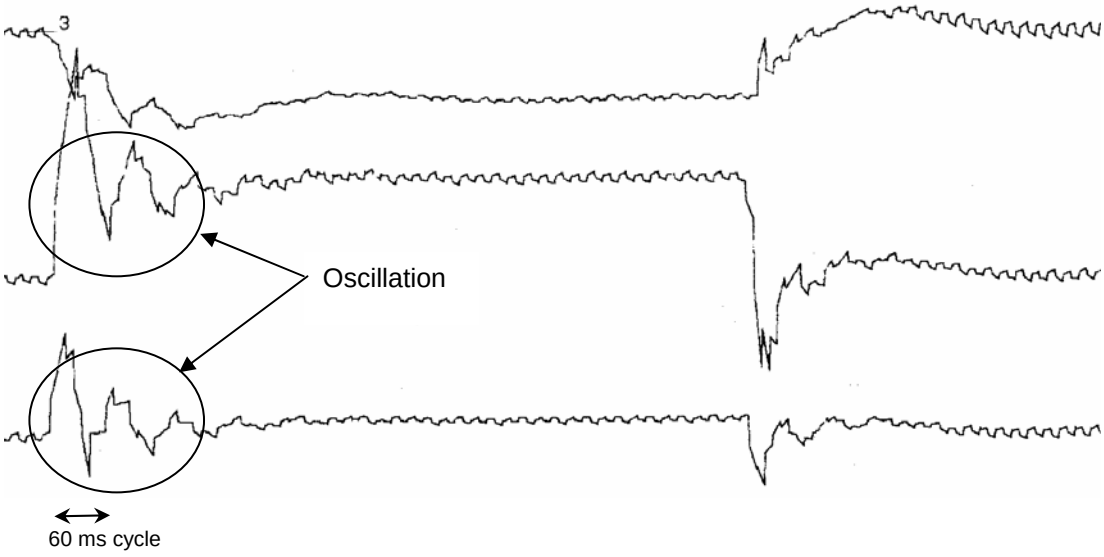

Figure 6.5: SVC control system load imbalance response oscillation.

As the sampling frequency of the chart recorder was set at 2 kHz, it is possible that aliasing has occurred during waveform measurement and the frequency of oscillation is higher than the 16.67 Hz oscillation observed in Figure 6.5.

Sub-harmonic instability in this frequency range has been observed historically at Blackwater substation during transmission system switching operations (Harvey, P. 2005, pers. comm. 17 Feb). The investigation concluded that this was attributable to system configuration and mine dragline load at the time and the phenomenon has not been observed within the past five years. However, if the SVC control system response to step input contains an oscillatory element in the sub-harmonic frequency range, it is possible that the response to a DC step type switching transient would exhibit the same response and have contributed to the system instability observed. This could not be investigated in more detail due to project time constraints.

Additional waveforms obtained during the SVC control system testing are contained in Appendix G.

6.3 Waveform Processing

6.3.1 Data Acquisition

The Hioki model 8826 chart recorder has the facility to record up to 32 channels of waveform information to magnetic (MO) type disk. This can then be read to a computer through a magnetic disk reader and saved as a .mem extension file. Hioki proprietary software, Hioki Wv version 1.17, possesses the capability of viewing the waveforms and exporting the data as either as comma separated data (.csv file) or a space separated text file. All title, time and channel label information is also exported as defined on the chart recorder by the user, so that the data may be later identified. The .csv files may be opened in Microsoft excel or imported into MATLAB as a data file.

Issues were discovered with exporting data from the Hioki Wv application. All data is exported in scientific notation but truncated at two decimal places by the Hioki software. This resulted in the loss of time base information, as increments were in the order of 0.4 ms, and a consequential loss of accuracy of waveform data for small scale signals. It was also discovered that if an offset had been introduced to a waveform trace for viewing purposes, when the data was exported this offset was also incorporated into the waveform values. Therefore all offsets had to be removed and data sets re-exported to correct this issue.

6.3.2 MATLAB

The most efficient approach to import of data was to firstly open the .csv file in Microsoft excel to remove extraneous information from the first lines of the file. This extraneous information made import of data to MATLAB very difficult. Once the .csv file was re-configured as columns of data with the first row containing the waveform label, the waveforms could be imported to MATLAB using the load data feature. The imported data was then saved as vectors identified with the column labels.

With the required data imported to MATLAB and the workspace saved, the time base information could be reconstructed given the length of the time vector and the time increment. The waveforms could then be plotted against a time scale for comparison with theoretical responses. Direct comparison must allow for the conversion of the voltages measured to per unit quantities, where 10 V equals 1.0 pu (ASEA 1986, p. 18).

7. Model Validation

7.1 Introduction

Validation of the developed SVC control system model for the Blackwater site requires comparison of the predicted responses with the actual responses measured. The worst case loading of the SVC was calculated and input to both the theoretical model and actual SVC control system to allow direct comparison of the responses obtained.

Project activity sequence was altered due to the rescheduling of SVC access for control system testing. As modelling was not yet complete, it was proposed to use experimental data obtained to modify PI controller parameters if time permitted. The settings used for initial comparison of predicted and measured responses were $K_p = 10$ and $K_i = 1000$.

The results obtained from the control system model were exported from Simulink to the MATLAB command space as structures with time, where the waveform and time scale information could be extracted and saved as vectors. Waveform information obtained during experimental testing was imported into MATLAB from the chart recorder software and the data also saved as vectors. Therefore, direct comparison of the predicted and measured control system response to step unbalanced load could proceed.

Experimental measurements were configured to capture 250 ms of waveform prior to the application of the step unbalanced load. As the theoretical model response is initialised at time zero and can not make allowance for initial system conditions, it was expected that considerable difference between predicted and measured responses during the early stages of model development would be observed.

It was anticipated that a second period of access to the Blackwater SVC could be arranged to rectify the deficiencies found in the experimental results and allow for additional refinement of the control system model. However, transmission system load in the Central Queensland region has not permitted the removal of the Blackwater SVC from service and further experimental work could not be performed.

7.2 Initial Comparison

Initial comparison of theoretical and measured control system response to step load imbalance exhibited considerable disparity as indicated in Figure 7.1. The SVC control system response measurements were performed with a steady state load applied prior to application of the step unbalance. Therefore the DC offset observable will be due to the SVC output susceptance required to regulate system voltage under the steady state conditions.

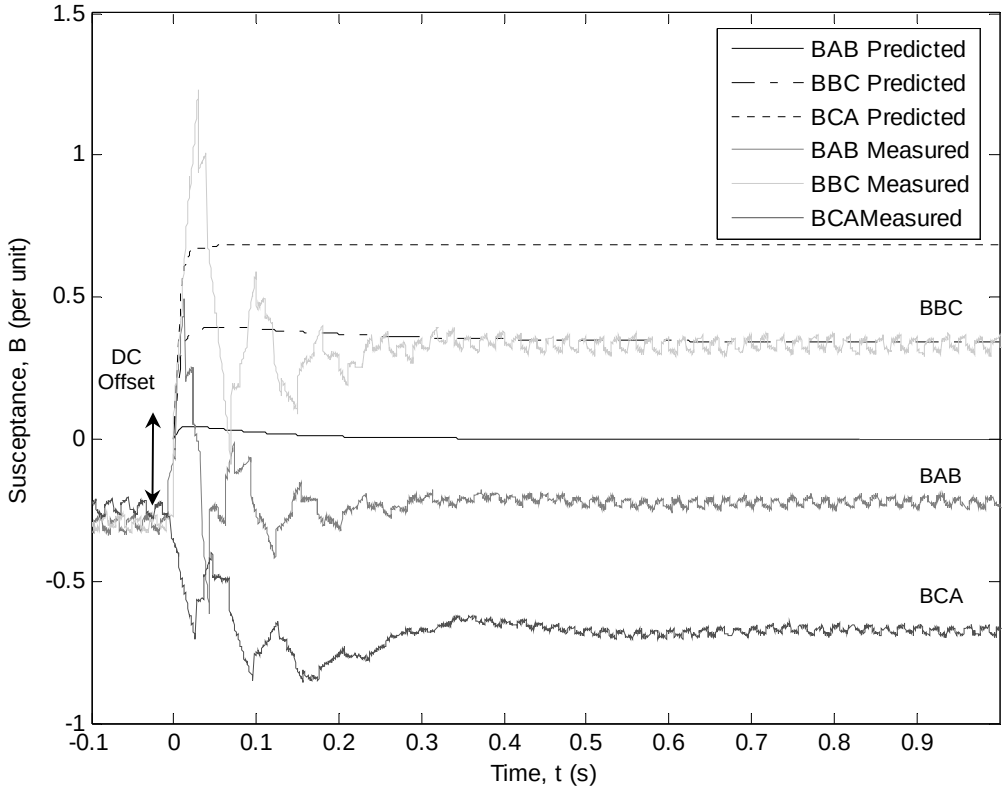

Figure 7.1: Comparison of three phase control system theoretical and measured response to load imbalance.

The actual control system response measurements displayed in Figure 7.1 also indicate that there is a slight discrepancy in the individual regulator susceptance levels in the region prior to the step unbalance load application. As the individual voltage regulator response should be identical under balanced three phase load, this disparity requires further investigation.

The DC offset observed in Figure 7.1 was compensated for and results compared on a phase by phase basis. For a step unbalanced load applied on A-B phase and offset compensation applied, the results are as displayed in Figure 7.2.

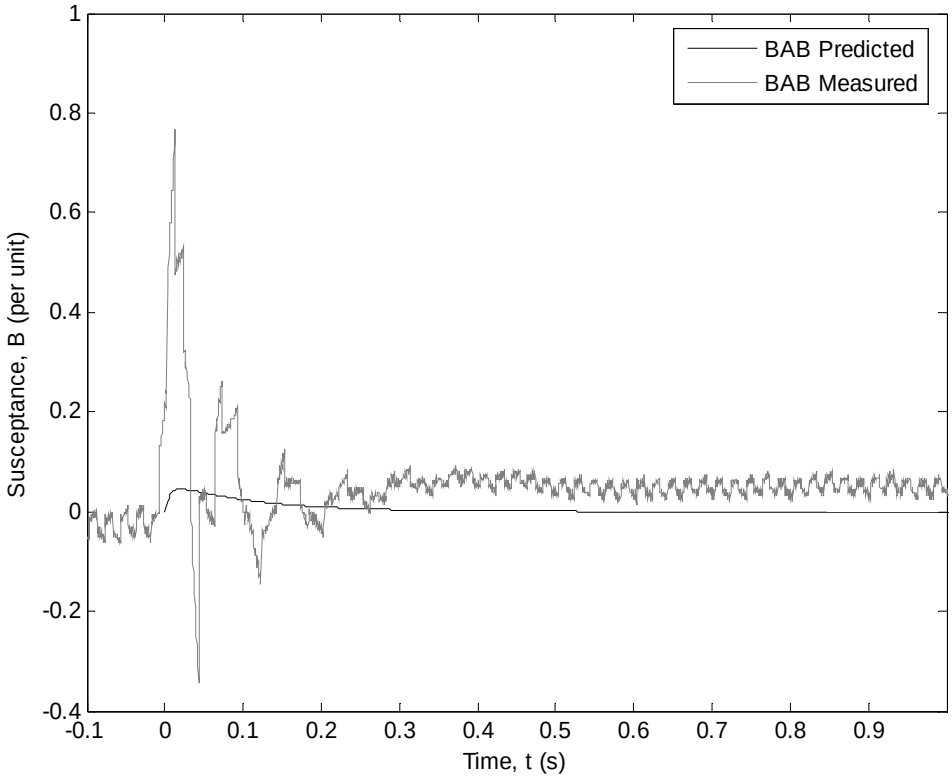

Figure 7.2: Comparison of A–B phase theoretical and measured response to load imbalance.

Neglecting overshoot and instability, the voltage regulator response of the phase input to which the step load is applied displays reasonable correlation despite. However, the remaining two phases exhibit considerable difference from the predicted responses. This pattern was observable for comparisons of step unbalance load response on each phase, indicating that the interconnection of the model voltage regulator blocks is incorrect. Some lag is observable between the measured and predicted response due to chart recorder triggering from the C- A phase regulator susceptance output BCA.

All additional waveforms obtained by comparison are contained in Appendix J.

7.3 Validation of Voltage Response

7.3.1 Signal Summation

The amplifier gains and linear combinations used to model the voltage regulator YXR 206A reference and response circuitry were simulated using the MATLAB script contained in Appendix H, and configured to accept the actual voltage waveforms measured. Therefore, the response simulated using the actual voltage inputs allowed direct comparison with the control signals measured at the voltage regulator card test points.

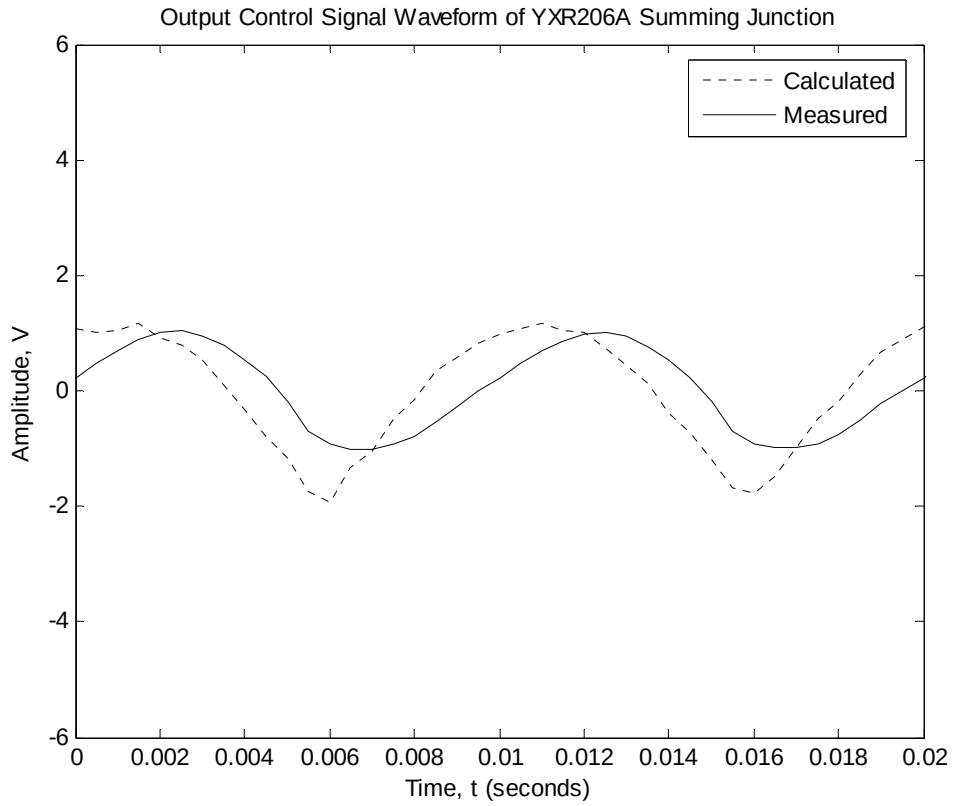

Figure 7.3: Comparison of calculated and measured summing junction waveform.

The comparison of the calculated and measured control signals at the output of the voltage regulator summing junction is displayed in Figure 7.3 and exhibits reasonable correlation. Some phase lag is apparent, which was anticipated as no transmission delays were incorporated into the simulation. The measured waveform also appears smoother indicating that the higher frequency components resulting from the rectification have been attenuated, and therefore low pass filtering has occurred within the circuit prior to test point 12.

To validate the simulation of the voltage regulator summing junction, the MATLAB simulation was configured to display the average of the calculated and measured outputs. The waveform data input to the simulation was acquired by manually triggering the chart recorder when the SVC was restored to service and thus should be approaching or at voltage set point. Therefore the averages of both the calculated and measured test point TP12 control signals should be similar and converging upon zero. The results obtained were:

```
Simulating voltage regulator function using measured values:

Average of Summing Junction output = -0.006672

Average of measured Test Point 12 = 0.009790
```

These values are reasonably similar and sufficiently close to zero to conclude that the voltage regulator summing junction simulation is correct.

7.3.2 Integration and Sampling

The integration and sample and hold block is stated with the manufacturer's documentation as having a sample time of 10 ms. A comparison of the calculated and measured waveforms at the voltage regulation card test point TP13 is displayed in Figure 7.4.

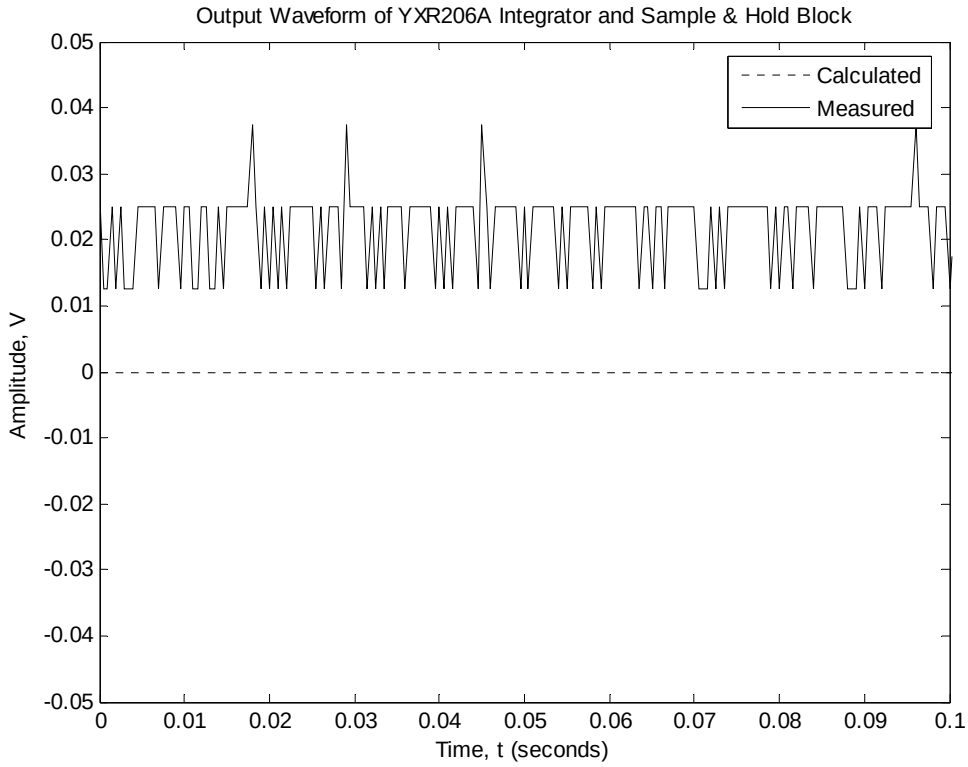

Figure 7.4: Comparison of calculated and measured control system signals at TP13.

There is considerable discrepancy between the measured control system signal and the simulated response, displayed in Figure 7.5. It may be concluded that the measured waveform at TP13 is high frequency noise. The expected 10 ms period is not observable and when checked the chart recorder channel input attachment was discovered to be faulty.

As this measurement was faulty, it was not possible to use the input and output control system waveform data of the PI controller to extract the system parameters.

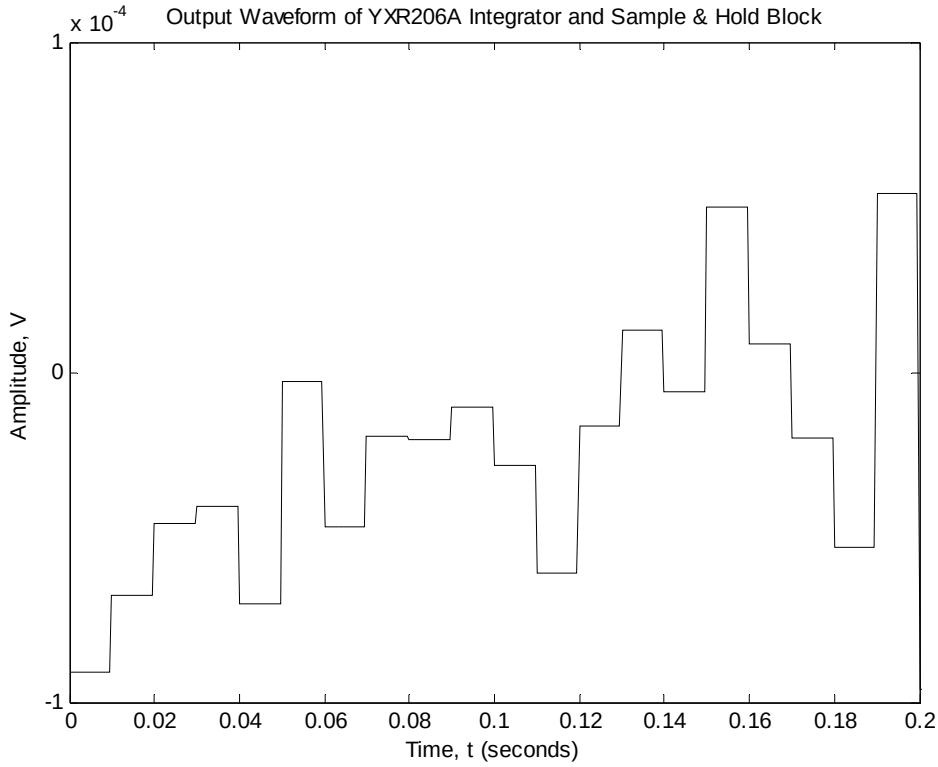

Figure 7.5: Calculated YXR 206A test point TP13 waveform exhibiting 10 ms period.

7.3.3 Conclusion

The modelling gains and linear combinations utilised up to the PI controller within the voltage regulation circuits are sufficiently accurate.

As the reduction in permitted access and testing time at Blackwater SVC did not allow sufficient time for validation of data, the faulty chart recorder channel was not identified. The faulty data precludes the possibility of using the input and output voltage waveforms of the PI controller to extract the system parameters.

Therefore the PI controller cannot be accurately modelled from the available data without performance of further SVC control system testing.

7.4 Theoretical Model Adjustment

The fixed capacitor offset was adjusted to reflect the actual settings discovered at the Blackwater SVC control system. In addition, analysis of the VREF signal determined by the SVC target voltage setting revealed that the average value was not the anticipated 1.5 V corresponding to the given reference voltage set point of 1.015 per unit (Appendix E). The actual average value of the VREF signal was measured as 3.25 V, indicating that the SVC target voltage has been altered to 1.03 per unit at some time since the settings were commissioned.

These parameters were adjusted and the adjusted theoretical control system response compared with the measured response with the results displayed in Figure 7.6.

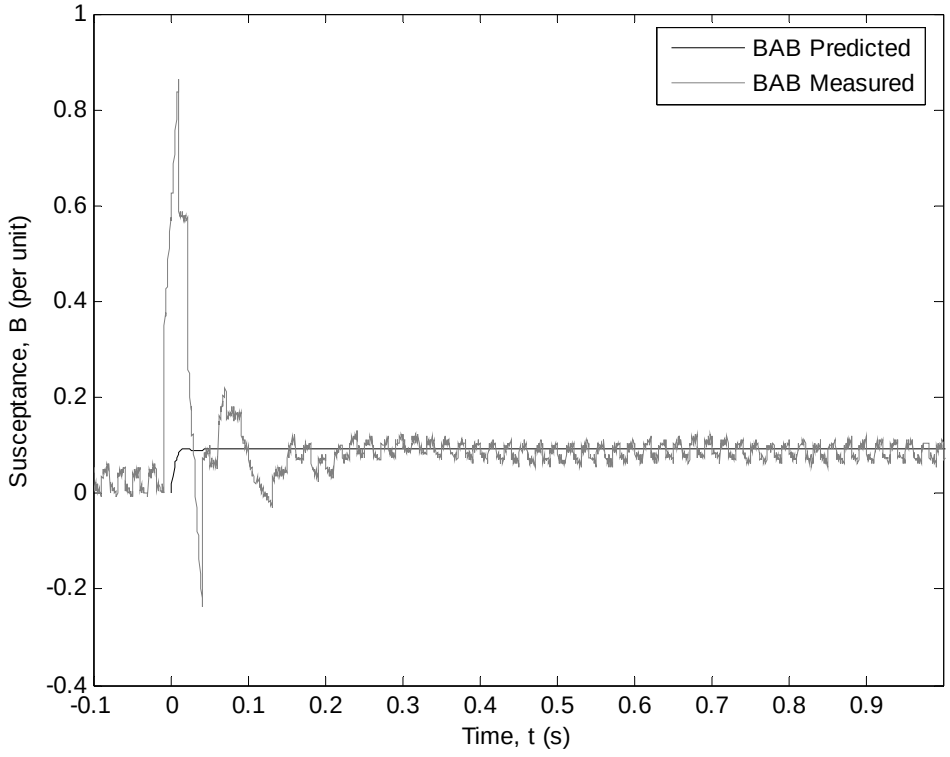

Figure 7.6: Comparison of revised control system model and measured response to load imbalance.

Improved steady state correlation between theoretical and experimental results was obtained from the modifications. However, the measured responses of the other phases still do not conform to predicted responses after initial control system model modifications.

7.5 Validation of Results

As use of the generic SVC control system model was never anticipated for system modelling applications, it was anticipated that very little correlation between theoretical and actual responses would be obtained initially. As a method of establishing the anticipated control system responses has been accomplished during the project and reasonable correlation observed between theoretical and actual responses on the unbalanced load phase regulator, a positive outcome has been achieved.

The comparison of the predicted and measured control system response indicates that the control system model developed does not yet generate theoretical results of acceptable accuracy. Lack of manufacturer's documentation and circuit diagrams has contributed to the inaccuracy of results. As multiple amplifier gains are applied throughout the SVC control system voltage regulation circuits to ensure that all voltages input to and output from the operational amplifiers remain within the permissible voltage range it is possible that some circuitry not noted in the manufacturer's documentation has been excluded from the model.

Measured fixed capacitor offset values differed from calculated quantities. As no records could be located stating the manufacturer's recommended setting at commissioning, the Transmission Grid Planning division of Powerlink Queensland should be consulted to determine the required offset value. If the fixed capacitor offset value applied to the SVC control system is too high, the negative response displayed by the C – A phase voltage regulator susceptance signal in Figure 7.1 will be due to the voltage regulator encountering the SVC capacitive limit (ASEA 1986, p. 21).

The PI parameters used are incorrect as response to the step unbalanced load is too slow although settling time appears acceptable. Suitable proportional and integral gains must be determined and the control system adjusted. However, the PI controller system parameters can not be calculated until valid input and output data is obtained. Therefore further development is required to achieve acceptable theoretical response.

SVC control system voltage regulator susceptance is not balanced when balanced three phase load is applied. Therefore, it is possible that some components have failed or drifted away from nominal values, resulting in uneven response between the individual phase voltage regulators. SVC response to balanced load could possibly cause some degree of system voltage unbalance and consequential generation of NPS voltage.

Instability observed in the voltage regulator control signals measured makes direct comparison of responses less meaningful. The lack of transmission delay incorporated into the developed SVC control system model has also contributed to inaccuracy of predicted responses.

It was determined that conditions exist where the dynamic response of the SVC may cause system instability as observed historically. Experimental data indicated that the Blackwater SVC control system voltage regulator gain was set too close to the limits of stability. The recommendation was made to Powerlink Queensland's Transmission Grid Planning division to consider a revision of the control system settings based on the experimental data obtained, as a decrease in gain might be beneficial in avoiding unstable system voltages. Therefore the issue necessitating the development of the control system model has been resolved.

8. Conclusions

8.1 Achievement of Project Objectives

The specific project objectives have been met as follows:

The regulatory and operational requirements for voltage regulation and load balancing of power systems were evaluated, with reference to Australian Standards and the National Electricity Code (NEC). The concept of power quality was introduced and the requirements to be met by electricity utilities to comply with regulatory limits requirements defined.

The cause of voltage imbalance and its impact on the power supply system and connected equipment were identified and reported. Impact of the Negative Phase Sequence (NPS) voltages resulting from unbalanced power supply system voltages was researched and the legislative limits of no greater than 2% for one minute peak loads identified, due to the potential damage to motors and generators connected to the system.

Information relating to SVC control system operation was researched and presented. This was performed first for general principles of operation and then in more detail for the load balancing type SVC, as it was the focus of the project. The overall effect of SVC operation on power systems was also discussed and their use in power system compensation justified.

The mechanisms by which Static Var Compensation systems achieve voltage regulation, load balancing and minimisation of Negative Phase Sequence voltages were evaluated. As obtaining experimental data was given precedence over this objective due to time constraints, and due to the complexity of SVC control systems, the extent of the critical evaluation of these mechanisms was limited. Identification and discussion of the key mechanisms was achieved, with these aspects analysed in some detail.

As a generic control system model was available, this was further developed and adapted to simulate the action of a load balancing type SVC system in MATLAB (Simulink) based on information obtained from manufacturer's documentation and component measurements.

Worst case load conditions were identified and input to the control system model utilising step load imbalance. In this manner the theoretical control system response to voltage and load imbalance was obtained.

Access to the Blackwater SVC was arranged and measurement of actual control system response to load and voltage imbalance performed. The waveform data obtained during control system measurements was then exported electronically for further processing and for comparison with theoretical responses.

Comparison of the SVC control system response predicted by theoretical modelling and those obtained by measurement of actual responses was performed and results indicated that the developed model had not yet achieved an acceptable level of accuracy. Several factors contributed to this including the lack of manufacturer's documentation, unsuitable assumptions regarding system parameters that were required to be recalculated using the experimental results obtained, lack of transmission delay incorporated into the control system response and incompleteness of the control system model. Modifications and further development are required to achieve an acceptable accuracy of theoretical response.

It was determined that conditions exist where the dynamic response of the SVC may cause system instability. The experimental data obtained clarified the cause of the system voltage instability observed historically at the Blackwater SVC, especially during load shedding situations. The cause was identified as unsuitable voltage regulator gain. Also contributing to unbalanced SVC control system response were fixed capacitor offset deviation from set values and unbalanced control system signal voltages under balanced load, due to component deterioration.

A report was written documenting the development of the Blackwater SVC control system model, including the adaptation required to conform to manufacturer's specifications and the validation process. The report also documents the experimental work performed to aid in the validation process.

Therefore all the aims of the project were accomplished, and a solution discovered to the problem that necessitated the development of the load balancing type control system model for Blackwater SVC.

8.2 Project Outcomes

The aim of this project was to determine the control system response of Static Var compensation systems, predicting response to unbalanced supply system loading. This has been almost entirely achieved, with the exclusions arising from failure to achieve the desired accuracy of theoretical model results. It can be concluded that it was unrealistic to expect to develop and validate a theoretical model of the size and complexity required in the time available.

As the generic model was never intended to be used in a system modelling application, it was anticipated that very little correlation between theoretical and actual responses would be obtained initially. The model function was never previously validated as the anticipated response was never identified. This has been accomplished during the project and all theoretical responses obtained by future modification of the control system model may be compared against a set of anticipated responses. Although the developed control system model is not yet suitable for use to accurately predict SVC response to unbalance load, correlation between theoretical and measured responses has been accomplished providing a positive outcome.

Therefore, it may be concluded that Blackwater SVC control system model developed is viable, although further work is required to achieve an acceptable level of accuracy.

Experimental data obtained indicated that the Blackwater SVC control system voltage regulator gain was set too close to the limits of stability. The recommendation was made to Powerlink Queensland's Transmission Grid Planning division to consider a revision of the control system settings based on project findings, as a decrease in gain might be beneficial in avoiding unstable system voltages as observed historically. A successful project outcome was achieved as the major issue that instigated the project has been solved.

8.3 Further Work

The desired accuracy of control system model response to unbalanced load was not achieved. Many factors contributed to this, including the difficulty in gaining access to an actual SVC control system to perform the measurements necessary for model validation. As testing time was restricted due to SVC repairs, it was not possible to revisit any experiments where test connections were faulty, resulting in loss of channel data, or that provided unexpected results.

Additional experimental work is required to continue adaptation and validation of the control system model. Due to the reduction in available testing time it was not possible to identify those model parameters that required specific attention and perform specific tests to aid in parameter identification.

Alteration of the model to provide initial load conditions prior to application of unbalanced load conditions would be an advantage. Due to time constraints it was not possible to incorporate this feature in the control system model, but its inclusion would avoid the control signal DC offset observed during the comparison of theoretical and experimental responses.

Instability of SVC control system response measured during experimental testing is not obtainable from the theoretical model at present. This may be attributed in part to the lack of transmission delay incorporated in the measuring and feedback elements of the model. Due to time constraints it was not possible to identify the transmission delay requirements and modify the model to more accurately reflect the actual control system response.

Inclusion of the thyristor control circuitry and power electronics elements of the SVC is required to accurately model control system response and also to aid in simulating the unstable control system responses. At present, the feedback loop is incomplete as the model only represents the portion of the control system up to the control signal generation.

Further work is required to obtain the parameters of the PI controller. Failure to obtain valid waveform information for the measurement point just prior to the controller resulted in an inability to analyse the transfer function and hence obtain the PI controller parameters. If the control system gain is reduced as per recommendations, the PI controller gain will be altered and require recalculation.

As the measured fixed capacitor offset significantly differs from the value calculated, consultation is required with Powerlink Queensland to verify the suitability of the measured fixed capacitor offset value. No record of the original setting of this value was found. Fixed capacitor offset is set during the manufacturer's control system commissioning process and the possibility exists that the value has drifted during the eighteen years elapsed since then. A fixed capacitor offset that is too high will limit the operational range of the SVC.

Under current system configuration, SVC control system response to balanced system conditions could possibly generate NPS voltage. Investigation into the causes of the unbalanced SVC control system response when balanced three phase load is applied should be instigated.

It is anticipated that the control system model will be incorporated into a larger model reflecting the entire behaviour of the SVC, although this future work will not proceed until the core control system model function is validated.

The addition of a graphical user interface (GUI) to allow for easier alteration of control system settings would be an advantage, allowing adaptation of the model to represent other load balancing type SVC control systems. At present the control system model is customised specifically to represent the Blackwater SVC system.

It would be an advantage to produce documentation detailing the function of the control system model to allow for easier use and adaptation. At present the model is undocumented, although some annotations were added to critical function blocks during the development process. Time constraints did not permit the development of appropriate model documentation, and this will be performed as future work.

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Appendix A

Approved Project Specification

University of Southern Queensland

FACULTY OF ENGINEERING AND SURVEYING

ENG4111 / 4112 Research Project
PROJECT SPECIFICATION

FOR:	**Kim Maree DAWSON**
TOPIC:	MODELLING LOAD BALANCING TYPE STATIC VAR COMPENSATION CONTROL SYSTEM RESPONSE.
SUPERVISOR:	Ron Sharma
ASSOCIATE SUPERVISOR:	Phil Harvey, Ergon Energy Corporation;
SPONSORSHIP:	
ENROLMENT:	ENG 4111 – S1, X, 2005; ENG 4112 – S2, X, 2005.
PROJECT AIM:	The aim of this project is to determine the control system response of Static VAR compensation (SVC) systems and predict their response to supply system voltage imbalance. This proposal is to devise a model, gather data and evaluate the model against the measured responses. As SVC control systems incorporate Proportional-Integral-Derivative (PID) controllers or similar, a second order model should achieve an acceptable model.
PROGRAMME:	**Issue B, 17th September 2005**

1. Evaluate the regulatory and operational requirements for voltage regulation and load balancing of power systems.
2. Analyse causes and impact of voltage imbalance and resultant Negative Phase Sequence voltages on high voltage plant and power system operation.
3. Research information on Static VAr Compensation control system operation and its overall effect on power systems.
4. Critically evaluate mechanisms by which Static VAr Compensation systems achieve voltage regulation, load balancing and minimisation of Negative Phase Sequence voltages.
5. Develop or adapt a model to simulate the action of a load balancing type SVC system in MATLAB (Simulink) based on information obtained from manufacturer's documentation and component measurements.
6. Simulate model response to voltage imbalance utilising step load imbalance to simulate worst case conditions.
7. Measure actual SVC control system signals and record response to power system voltage or load imbalances.
8. Determine if the developed model is acceptable by comparison of predicted responses with measured values and thus validate or otherwise the assumptions made.
9. Write a report documenting the development, adaptation and validation of the control system model.

As time permits:

10. Determine if any power system conditions exist where the dynamic response of the Static Var Compensator may cause instability.

AGREED:

_____ (Student) _____, _____ (Supervisors)

(Dated) 20 / 10 / 05 20 / 10 / 05 __ / __ / __

Appendix B

Voltage Excursion Waveforms

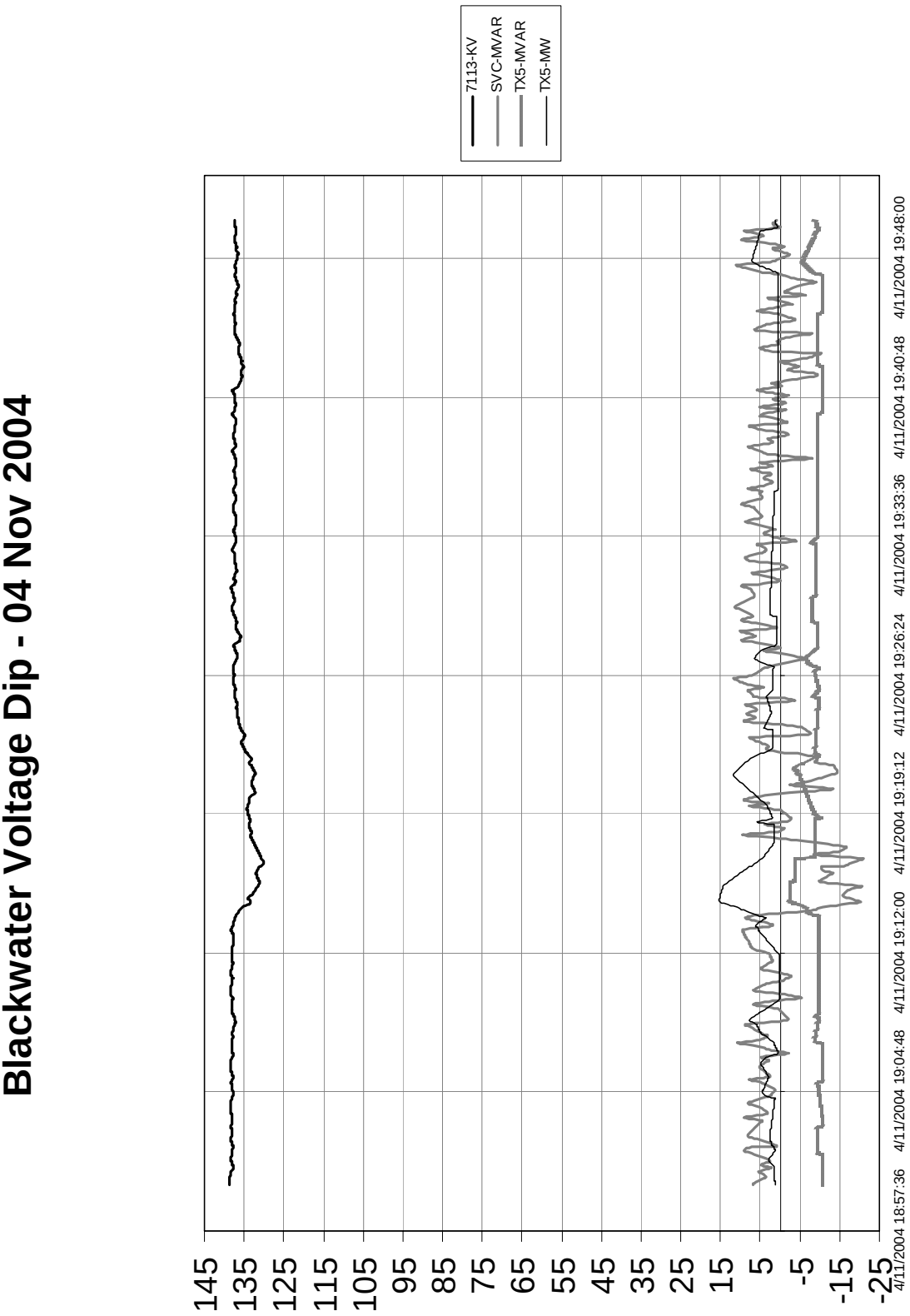


Figure B.1: T032 Blackwater load and voltage profile

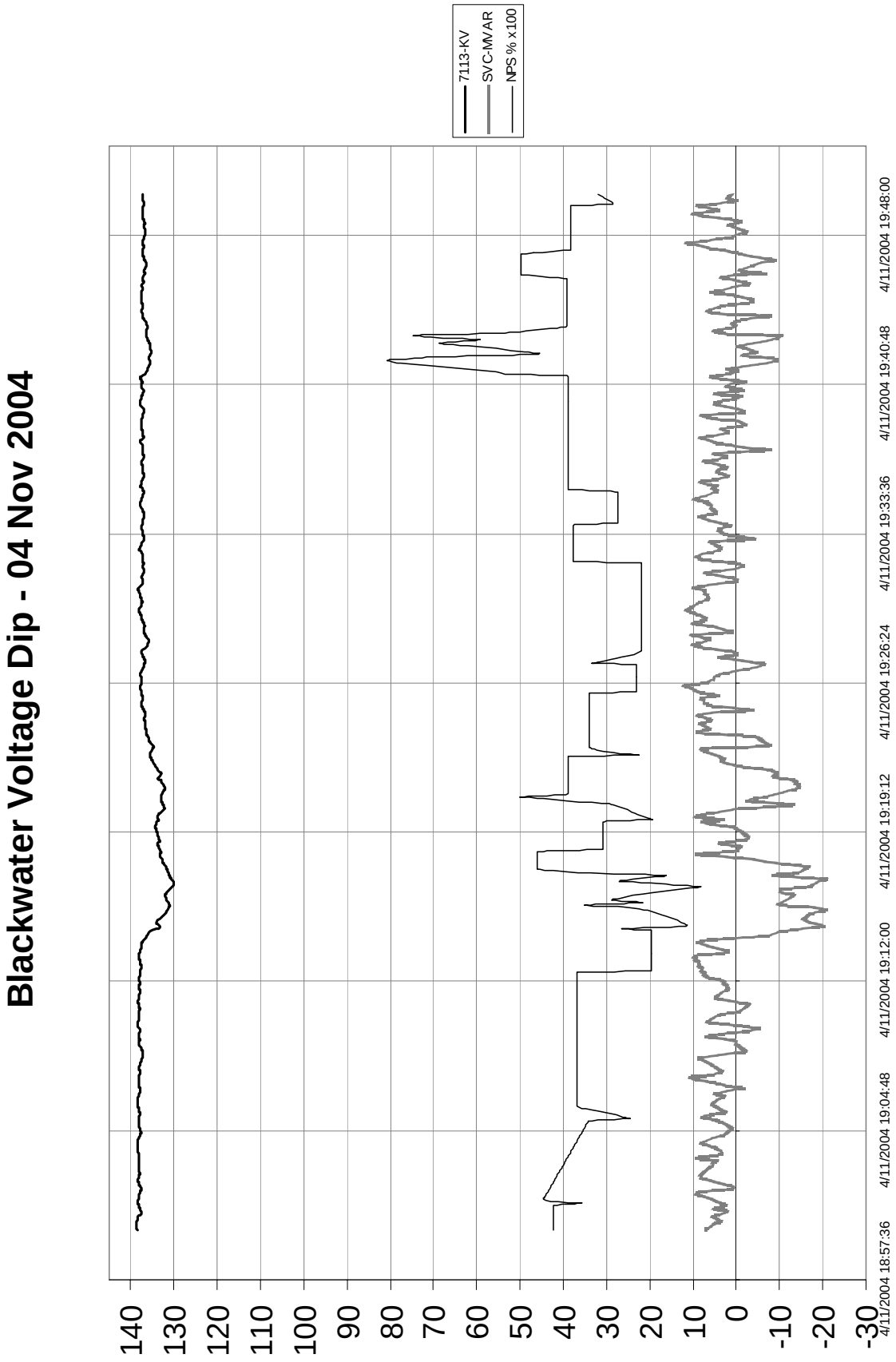


Figure B.2: T032 Blackwater NPS and voltage profile

Appendix C

C.1: Nomenclature

C.2: Manufacturer's abridged schematics

(Source: ASEA 1986, *'QR Electrification SVC control systems Technical reference'*)

C.3: Table of experimental test measurement points

C.1 Nomenclature

The table C.1 provides an interpretation of selected symbols used in ASEA SVC control system abridged schematics. This table has been devised by a comparison of abridged schematics, the circuit diagrams available and inspection of the control system card circuitry.

Table C.1: Identification of ASEA abridged schematic non-standard symbols

Symbol	Interpretation
	Integrator
	Constant multiplier
	Proportional Integral controller
	Inverting rectifier
	Variable
	Variable limit
	Summing junction
	Sample and Hold

C.2 Schematics

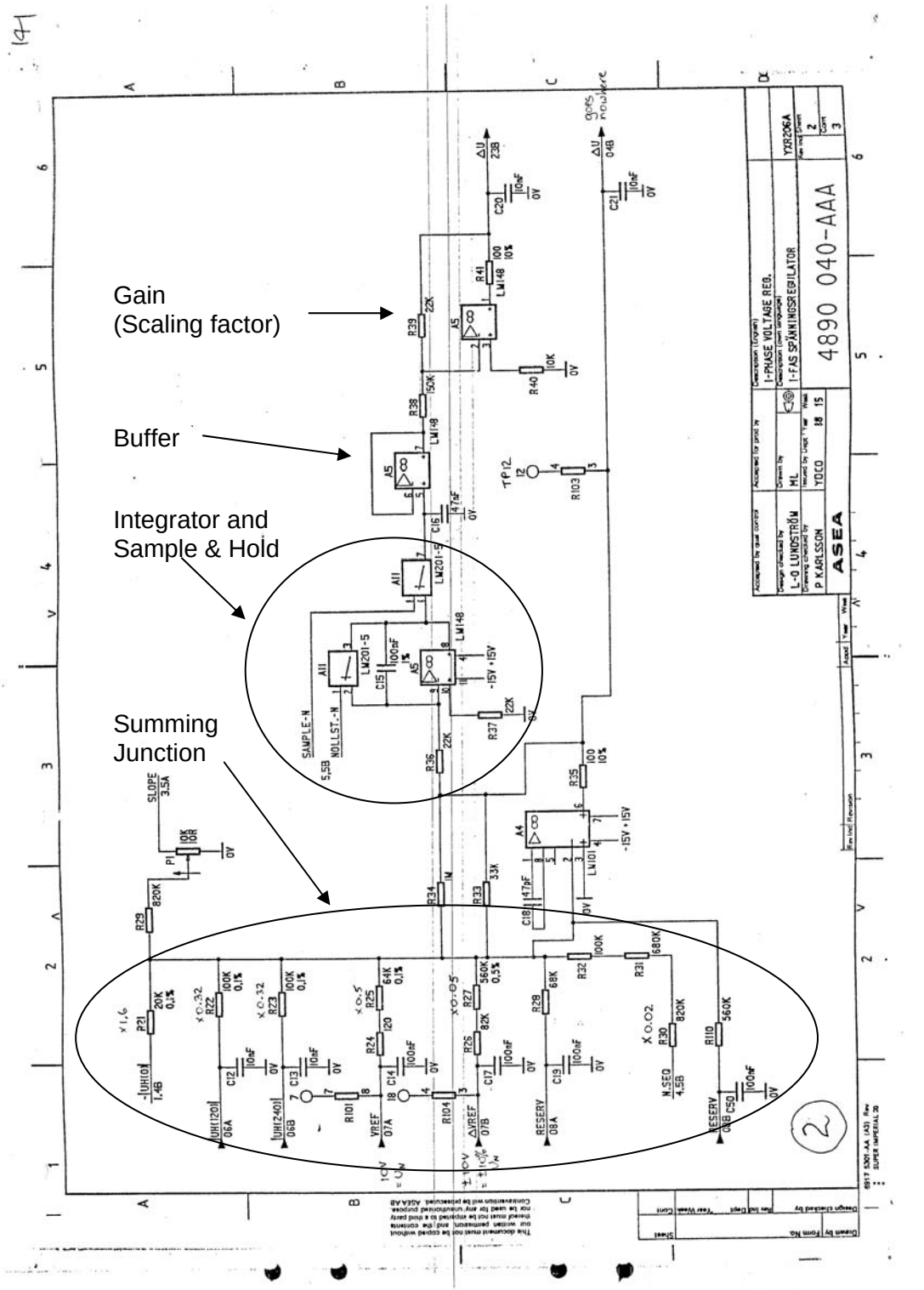


Figure C.1: Voltage regulation card YXR 206A partial circuit diagram (ASEA schematic 4890 040-AAA, sheet no. 3)

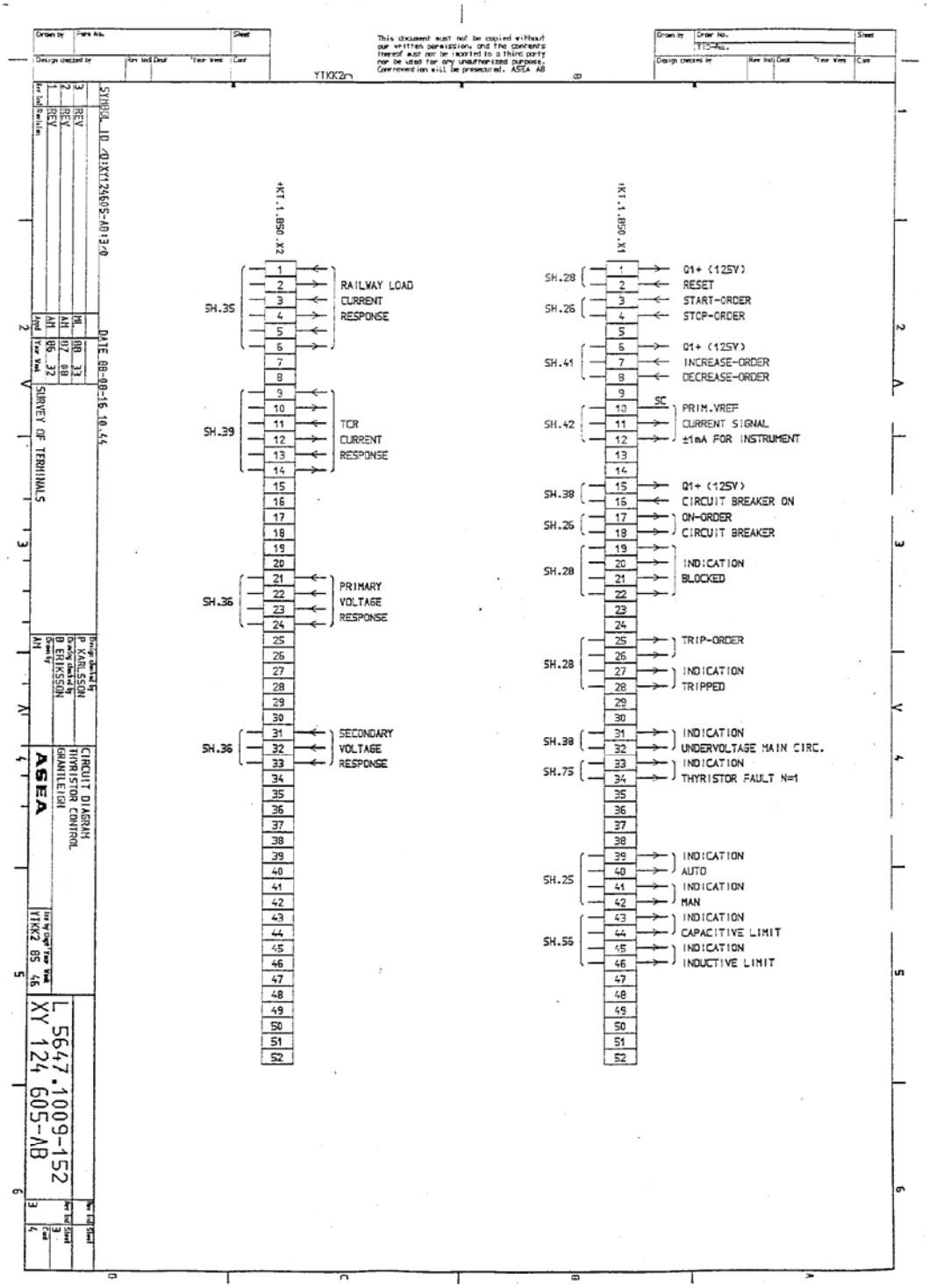


Figure C.2: SVC control system terminal strip layout

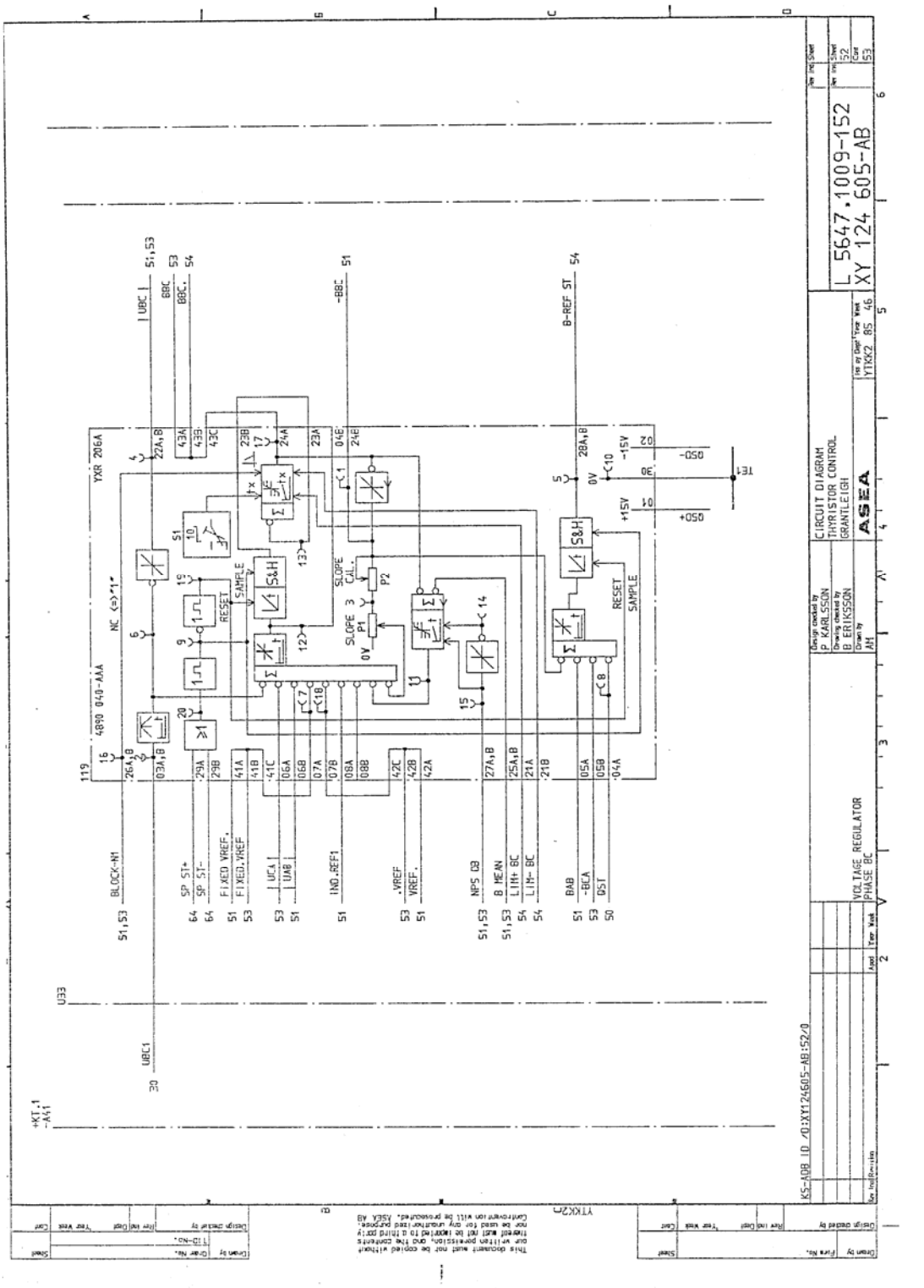


Figure C.3: Voltage regulation card YXR 206A abridged schematic

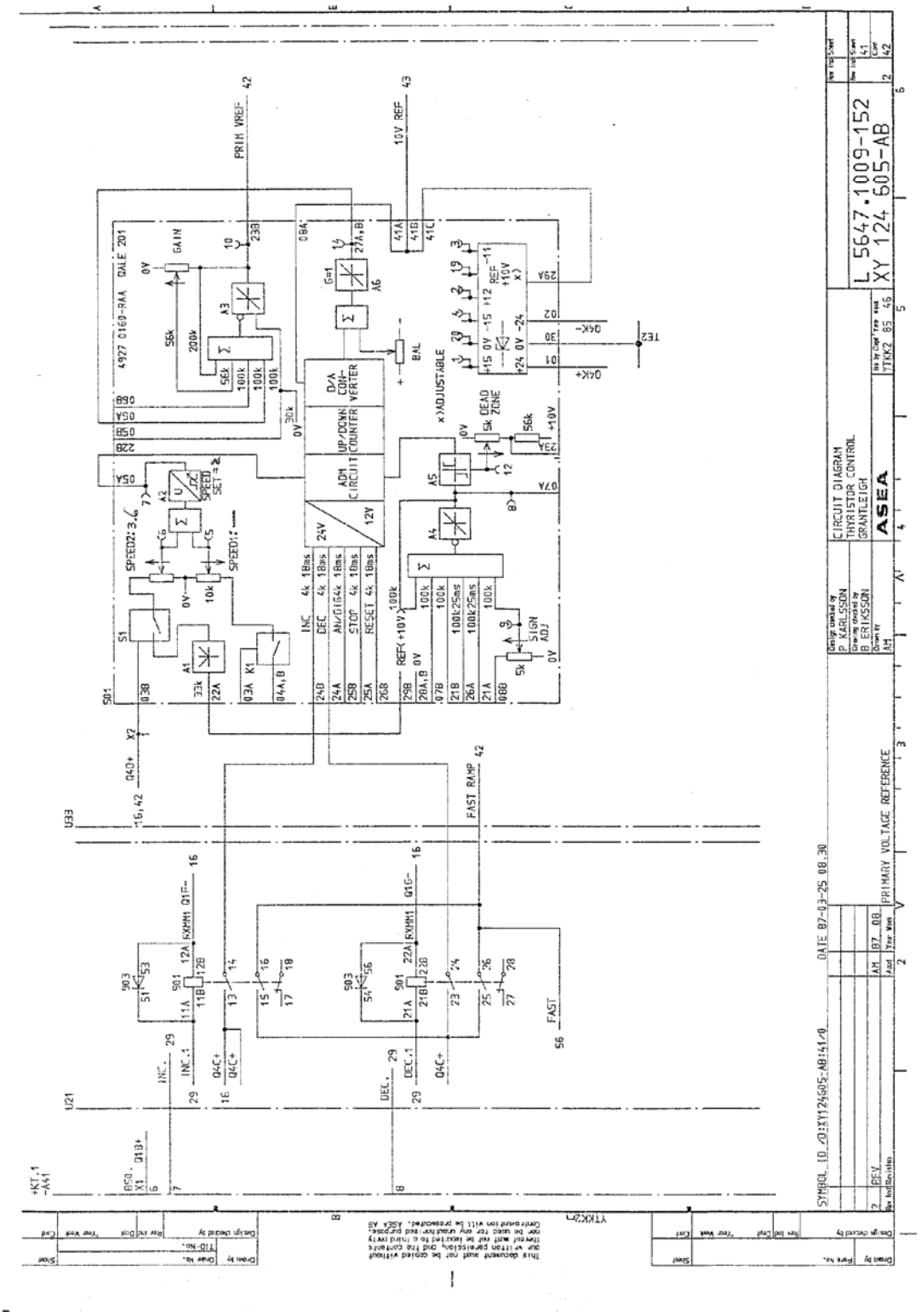


Figure C.4: QALE 201 Ramp unit No. 1 abridged schematic

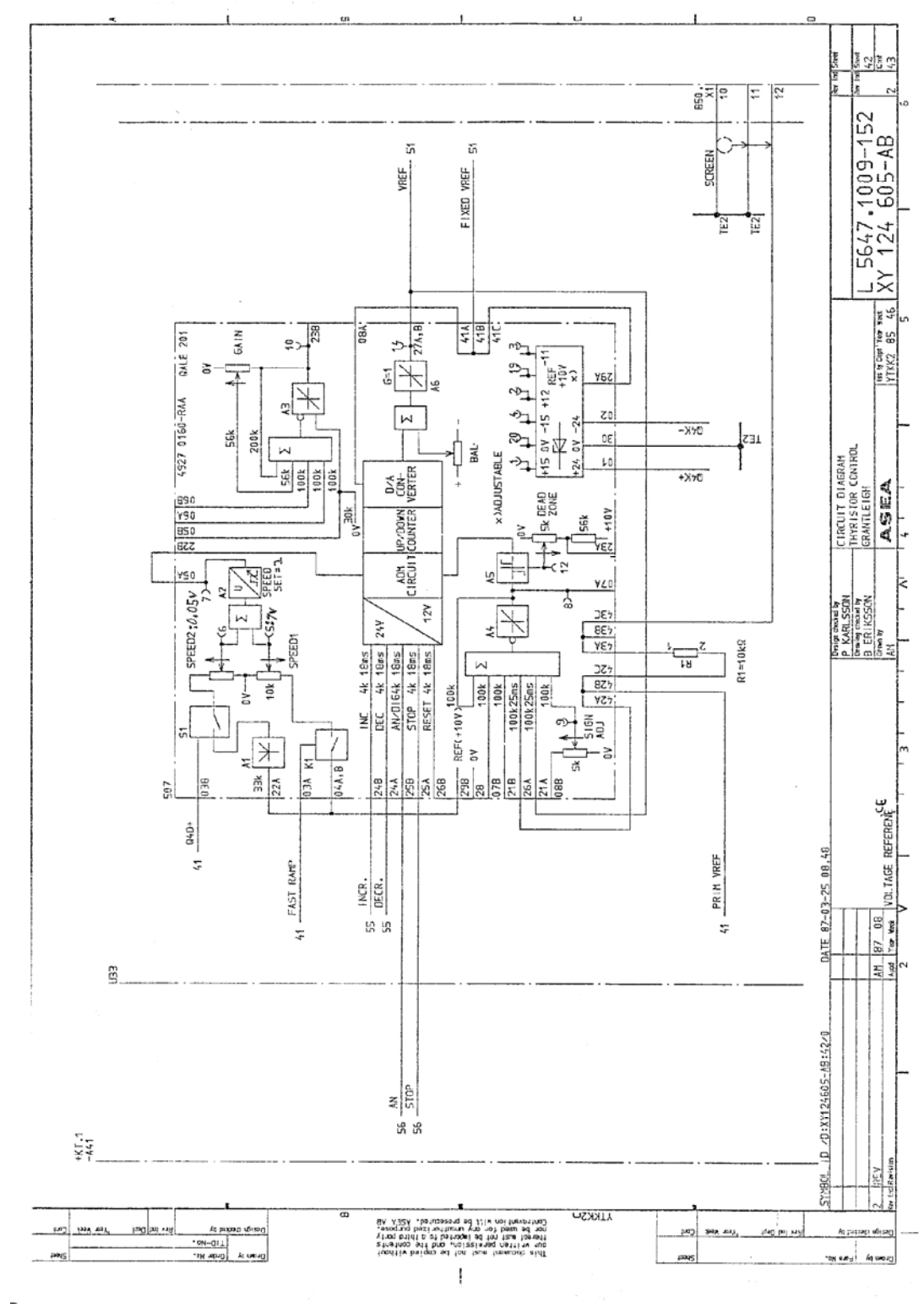


Figure C.5: QALE 201 Ramp unit No. 2 abridged schematic

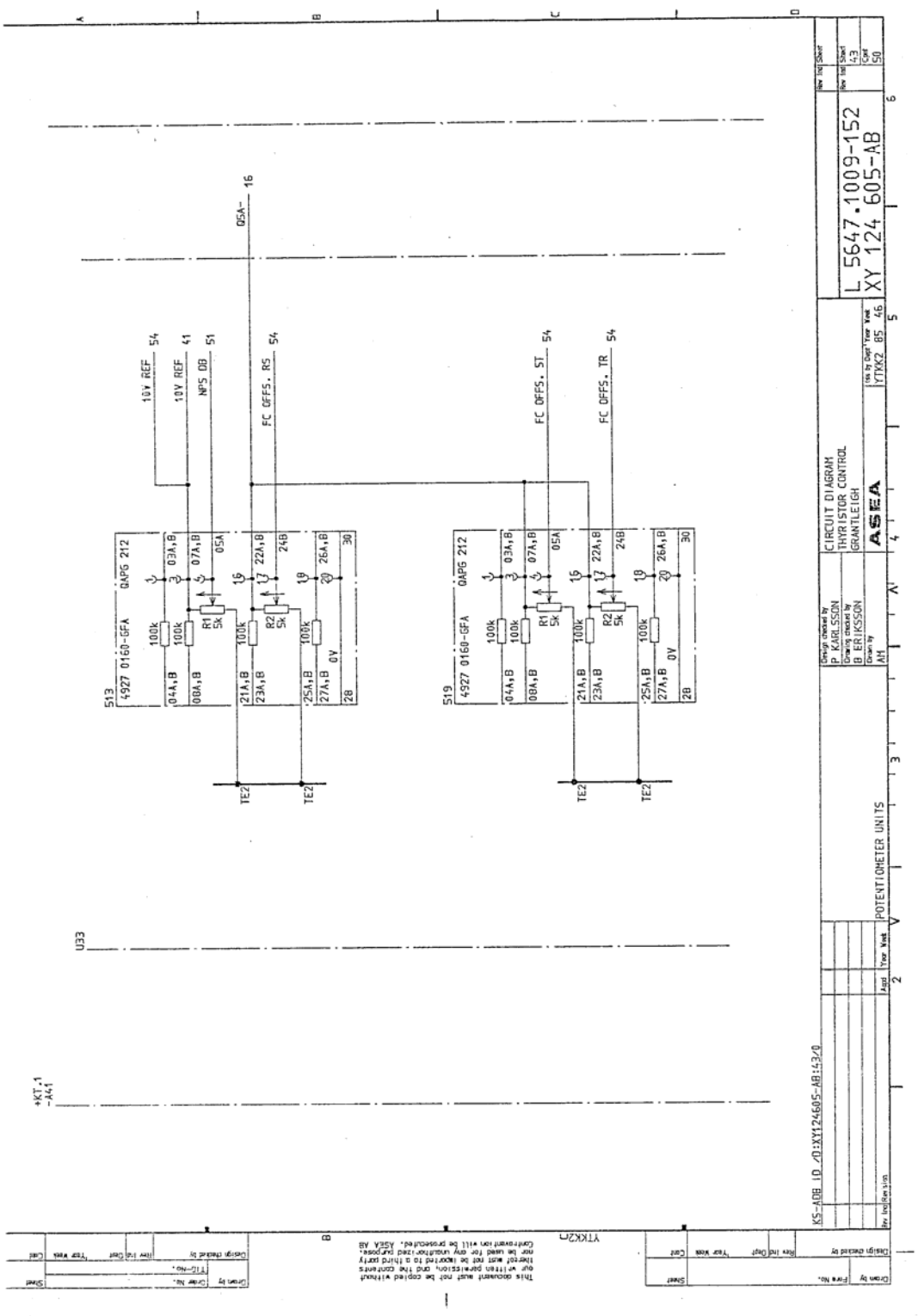


Figure C.6: Potentiometer unit QAPG 212 abridged schematic

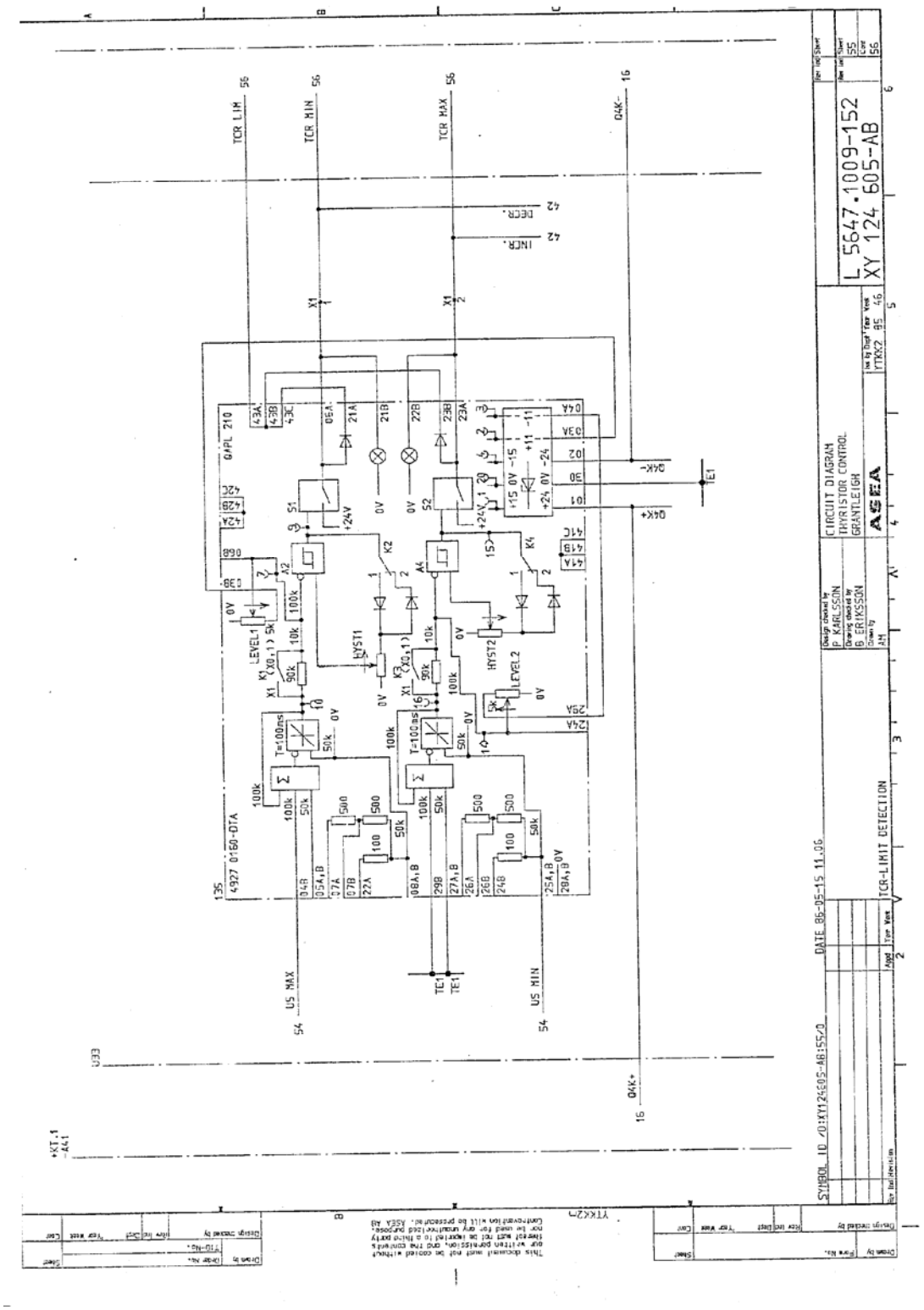


Figure C.7: Level detector circuit board QAPL 210 abridged schematic

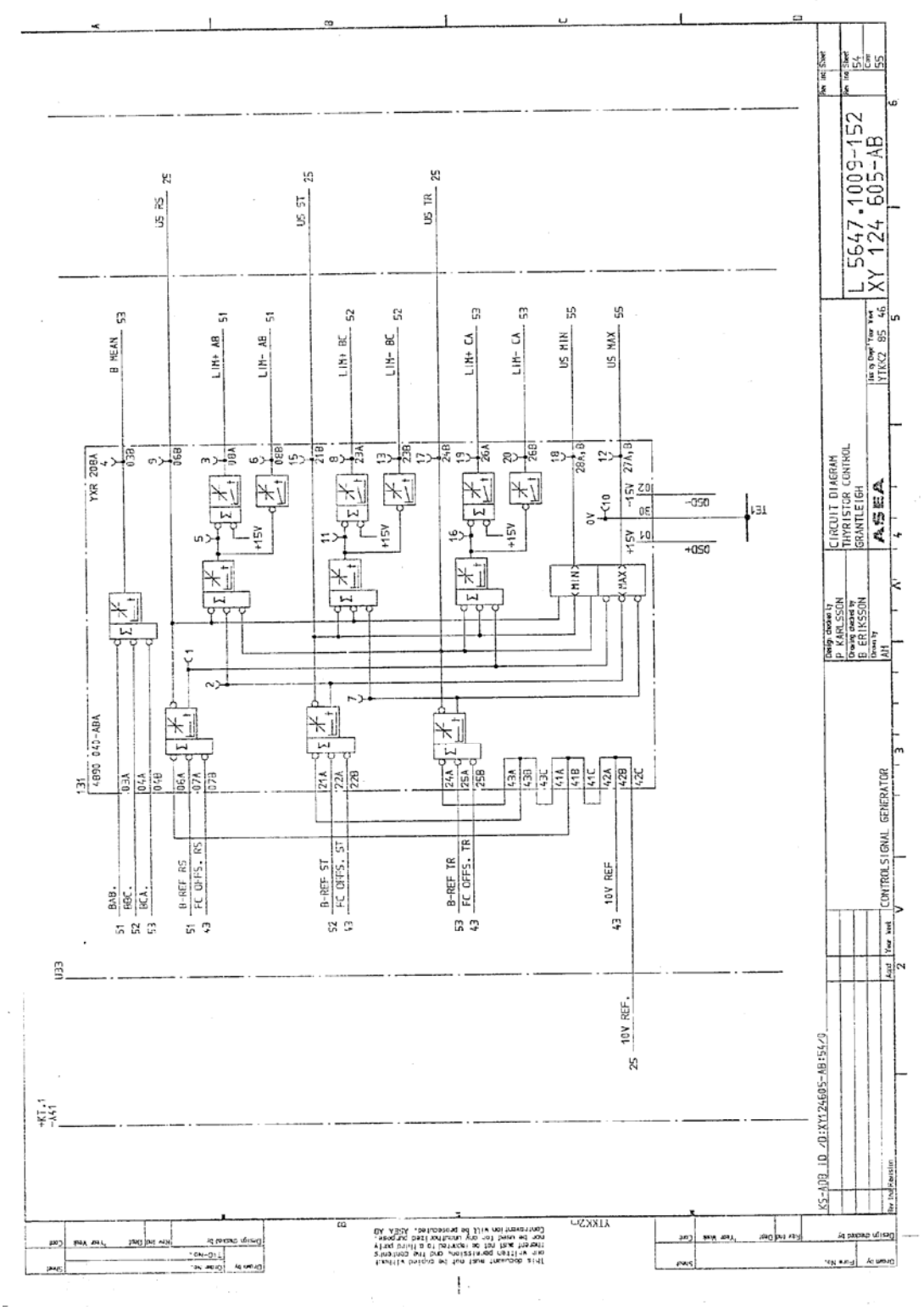


Figure C.8: Control signal generation card YXR 208A abridged schematic

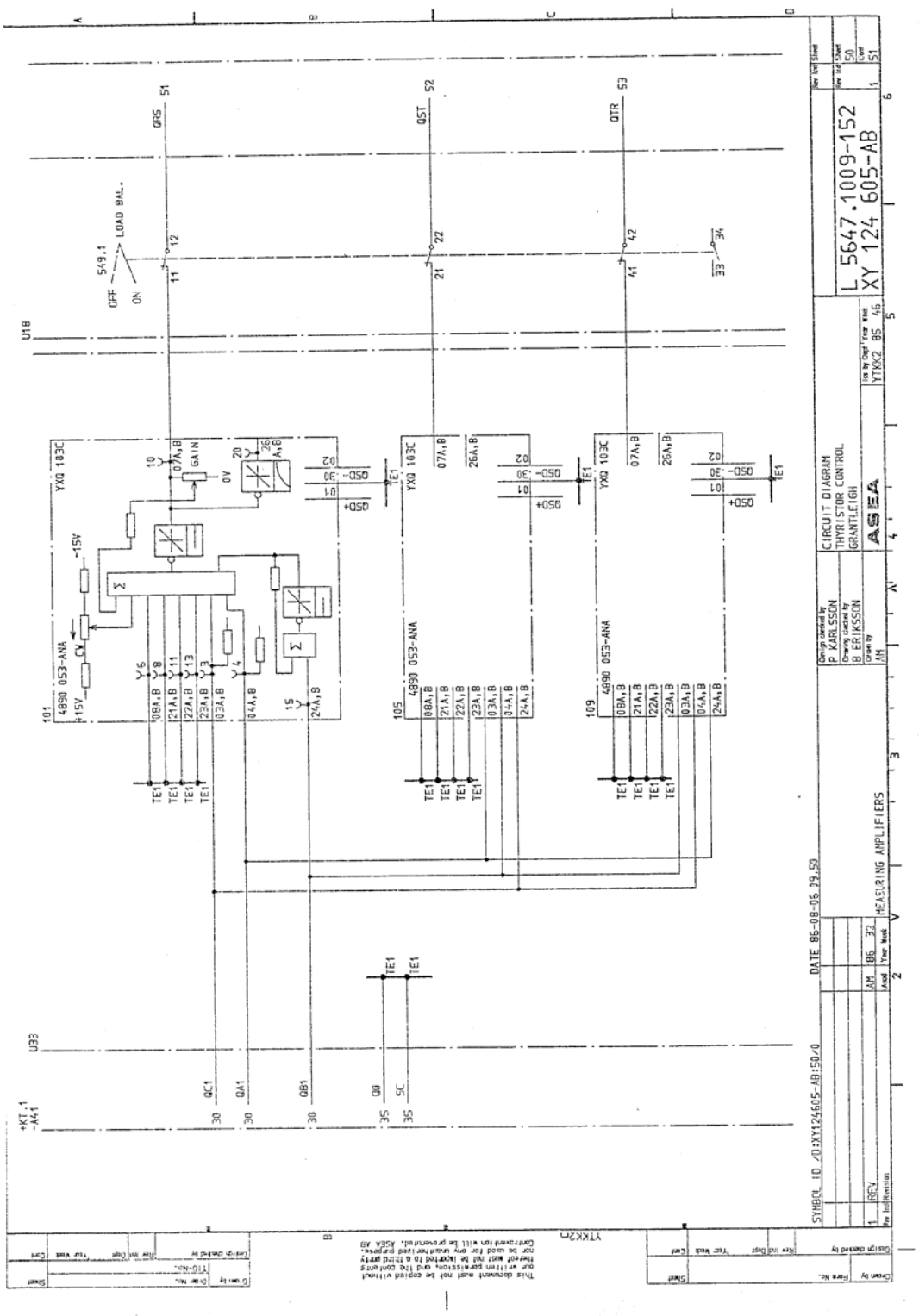


Figure C.9: Steinmetz controller card YXQ 103C abridged schematic

C.3 Experimental Measurement Points

Table C.2: Experimental test measurement points.

Card	Test Point	Signal Name	Channel No.	Signal Ground
YXR 206A – 1	5	B-REF RS	1	Test point 10
YXR 206A – 2	5	B-REF ST	2	Test point 10
YXR 206A – 3	5	B-REF TR	3	Test point 10
YXR 206A – 1	17	BAB	4	Test point 1
YXR 206A – 2	17	BBC	5	Test point 1
YXR 206A – 3	17	BCA	6	Test point 1
YXR 206A – 1	12	GAIN IN	7	Test point 10
YXR 206A – 1	13	GAIN OUT	8	Test point 10
QALE 201-1	10	PRIM VREF	9	Earth TE2
QALE 201-2	14	V REF	10	Earth TE2
QAPL 210	9	TCR MIN	11	Earth TE2
QAPL 210	15	TCR MAX	12	Earth TE2
YXR 208A	9	US RS	13	Test point 10
YXR 208A	15	US ST	14	Test point 10
YXR 208A	17	US TR	15	Test point 10
YXR 208A	18	US MIN	16	Test point 10
YXR 208A	12	US MAX	17	Test point 10
YXR 206A – 1	2	UAB1	18	Earth TE1
YXR 206A – 2	2	UBC1	19	Earth TE1
YXR 206A – 3	2	UCA1	20	Earth TE1
YXR 157	1	IRS1	21	Earth TE1
YXR 157	4	IST1	22	Earth TE1
YXR 157	7	ITR1	23	Earth TE1
YXQ 103C	3	QC1	24	Earth TE1
YXQ 103C	4	QA1	25	Earth TE1
YXQ 103C	15	QB1	26	Earth TE1
YXN 119H	3	URS1	27	Earth TE1
YXN 119H	4	UST1	28	Earth TE1
YXN 119H	5	UTR1	29	Earth TE1

Appendix D

Generic Control System Model

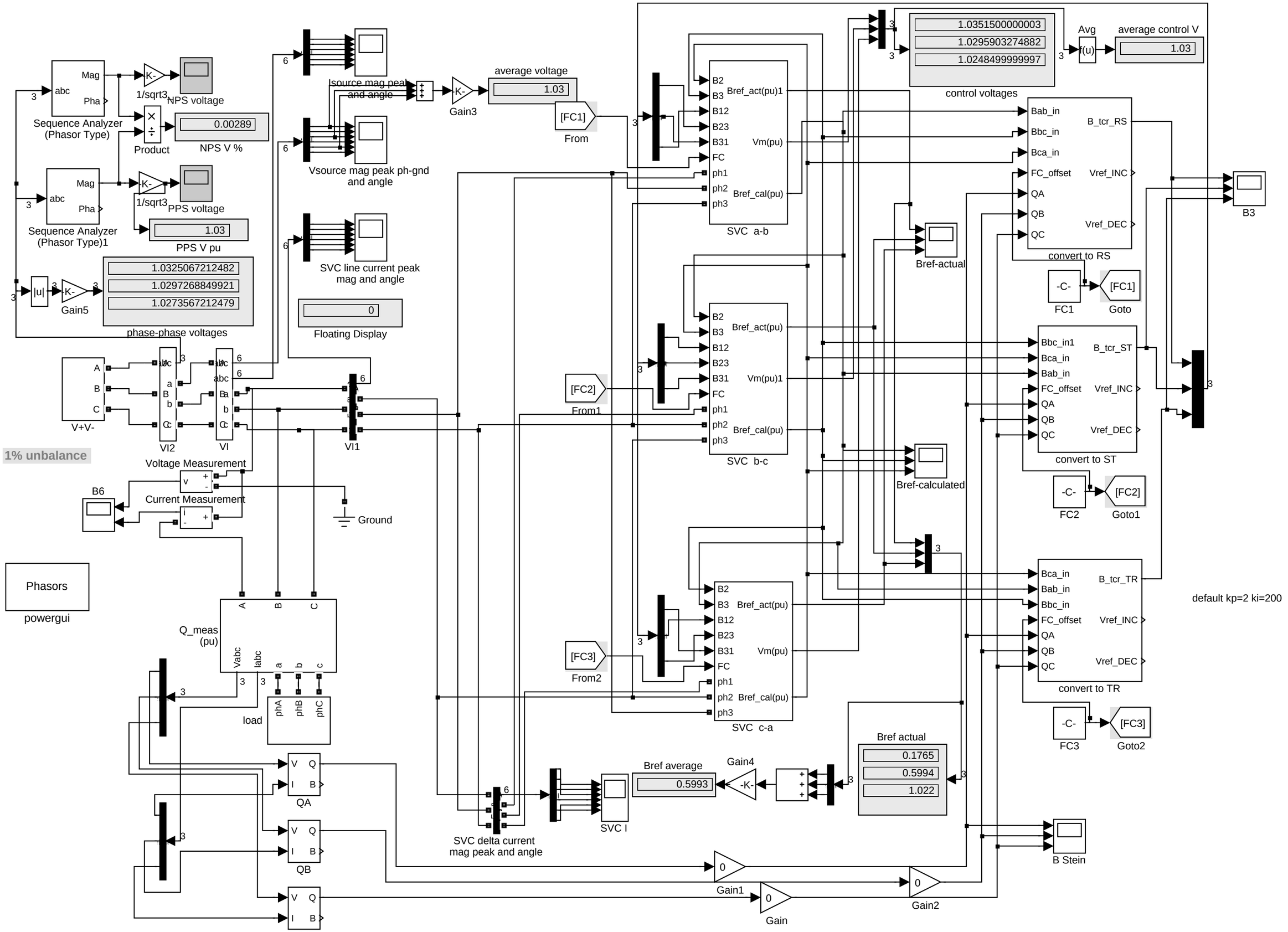


Figure D.1: Generic SVC Control System Model

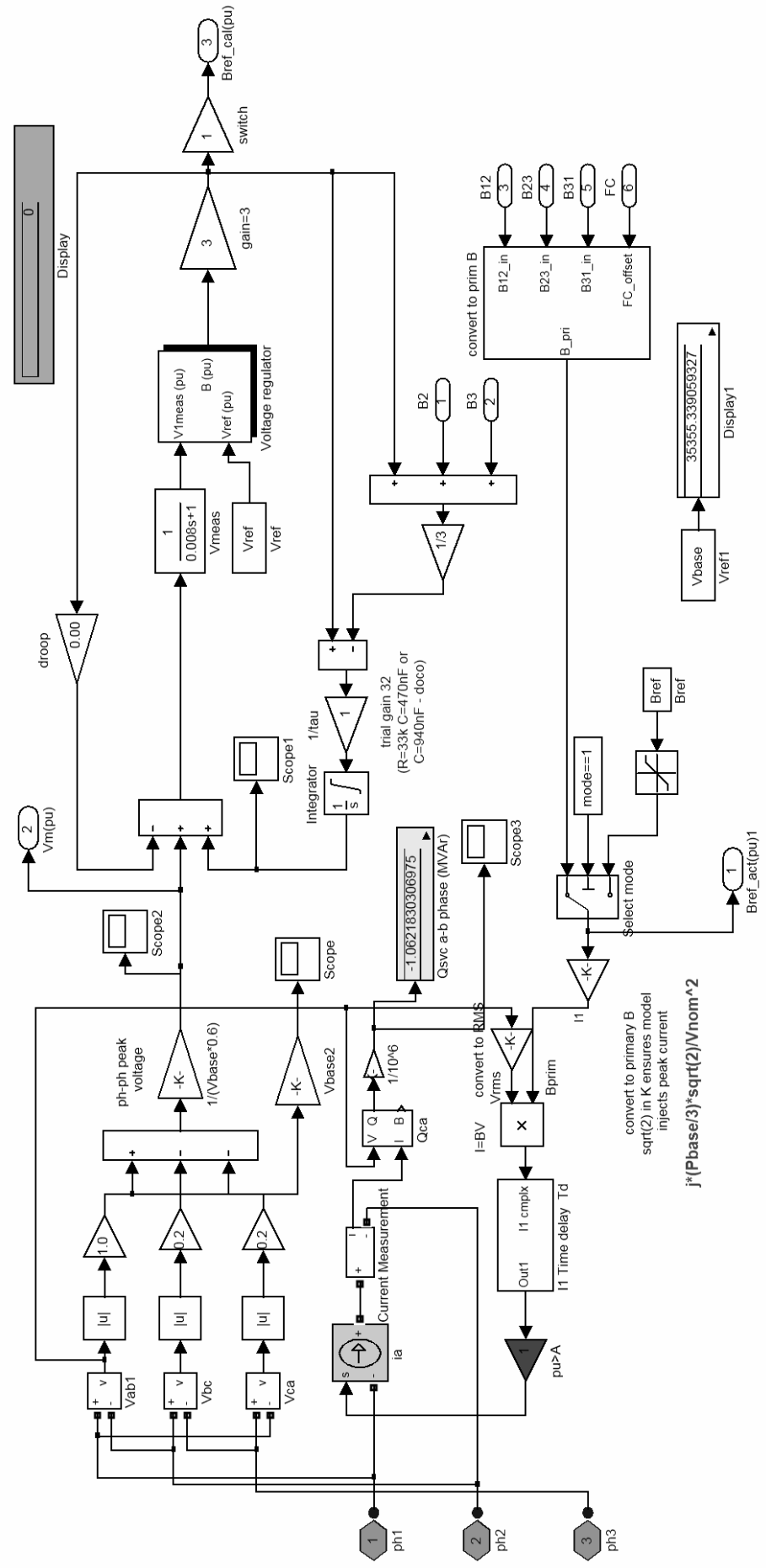


Figure D.2: A-B∅ voltage regulation model block detail

Appendix E

Blackwater SVC Control System Settings

QUEENSLAND SYSTEM OPERA

STATIC VAR COMPENSATOR - CONTROL SETTINGS

SUBSTATION: **T32 BLACKWATER**

Setting sheet number: 41 Dated: 15 July 1998

Instructions
1. Please check all existing settings and record any deviation.
2. Please change all settings marked with an asterisk (*) to the required value.
3. The **ORIGINAL** copy **must** be signed and returned to Manager Security Planning - Belmont
4. Enquiries to M. Stacey at Belmont on 07 32287966

CONTROL FUNCTION	ITEM LOCATION	ITEM DESCRIPTION	ITEM TYPE	EXISTING SETTING	REQUIRED SETTING
GAIN (1-10)	KT1.U33:113	VOLTAGE REGULATOR	YXR 206A	AB: 6 BC: 6 CA: 6	AB: 6 BC: 6 CA: 6
DROOP (0-10) = 4 %	KT1.U33:113	VOLTAGE REGULATOR	YXR 206A	AB: 0 BC: 0 CA: 0	AB: 0 BC: 0 CA: 0
NPS DEADBAND (0.00 - 10.00) (0 - 4 %)	KT1.U33:513	POTENTIOMETER UNITS	QAPG 212	1.25	1.25
VOLTAGE REF' SETPOINT (108 -156 kV)	KA1.D1:7	VOLTMETER	CEWE RC62	134kV	134kV
♦**Under voltage start inhibit relay**	SA1 B37 4	UNDERVOLTAGE PROTECTION		Not previously advised.	0.9 pu *
LOW VOLTAGE THRESHOLD for INDUCTIVE OPERATION (0 - 1.0)	KT1.U33:529	UNDERVOLTAGE PROTECTION UNIT	YXN 119H	0.5	0.5
LOAD BALANCING (ON/OFF)	KT1.U21:549. 1	SWITCH		POSN: OFF	POSN: OFF
AVR (ON/OFF)	KT1.U21:	SWITCH		POSN: ON	POSN: ON
PRIORITY Volt Control Ramp rate *FORWARD*	KT1.U33:50T	POTENTIOMETER UNIT & SWITCH	QALE 201	Speed 1 pot (TP5) SW POS: 2 POT SET: 6.92V Rate = 1kV/sec	SW POS: 2 POT SET: 6.92V Rate = 1kV/sec
RETURN	KT1.U33:50T	POTENTIOMETER UNIT & SWITCH	QALE 201	Speed 2 pot (TP6) SW POS: 2 POT SET:0.24V Rate=0.033kV/sec	SW POS: 2 POT SET:0.24V Rate=0.033kV/sec

APPLICATION of settings requested by MSP - R. Good **Date:** 15 July 1998

CONFIRMATION of settings applied by **Date:**

Please note any difficulty in applying required settings:-

QSO confirmation:- **Received by** **Date:**

Filed in BEL 660/42/8 by **Date:**

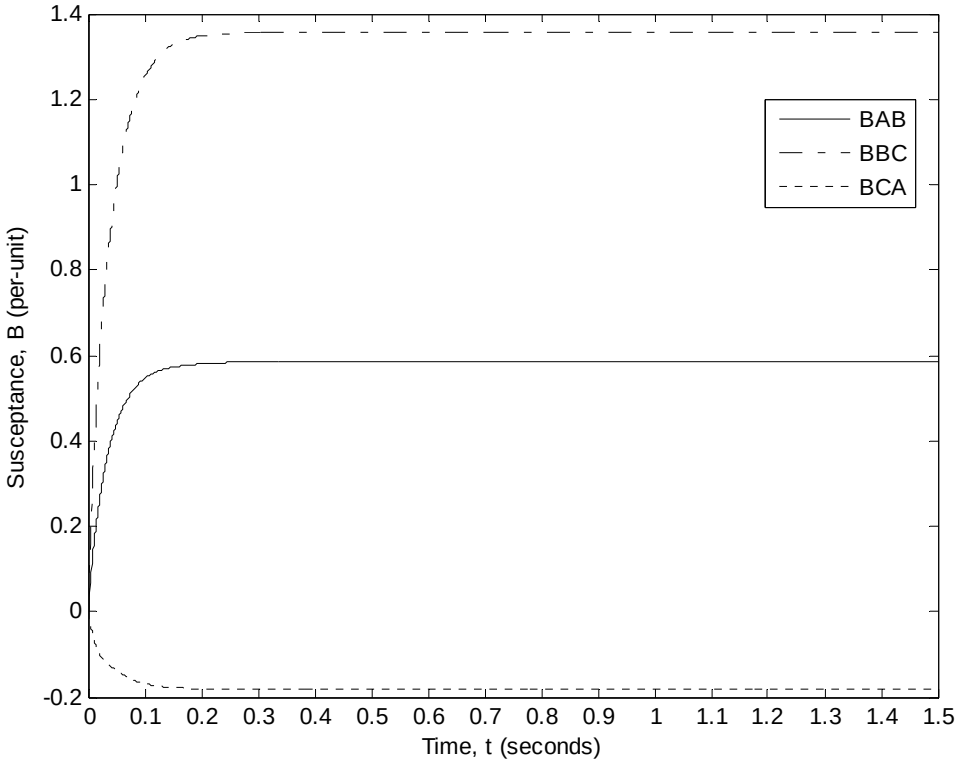
♦ Please note the new setting field for the Under voltage start inhibit relay.

\\htdj01\outage$\Networkautomation\SVC SETTINGS.doc

Appendix F

To demonstrate the sensitivity of the PI controller to parameter variations, the following plots have been included:

- Model Theoretical Response Waveforms (PI Controller: Kp = 1, Ki = 100)
- PI Controller transfer function bode plot
- Model Theoretical Response Waveforms (PI Controller: Kp = 10, Ki = 1000)



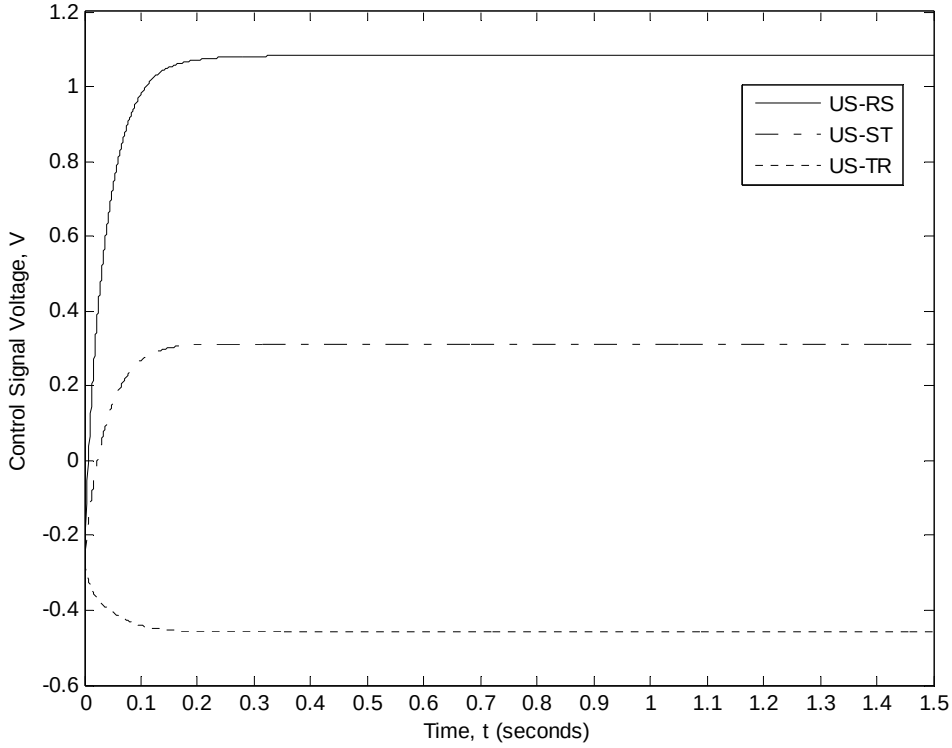
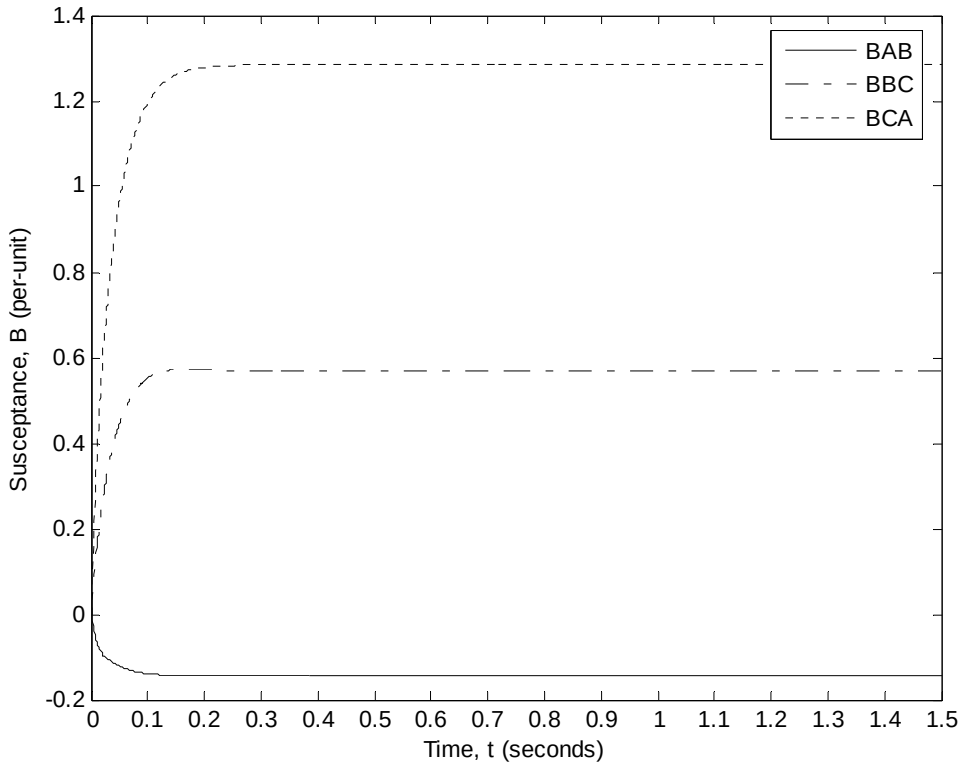


Figure F.1: Model response to 0.5 pu step load applied to A phase (Kp = 1.0, Ki = 100).



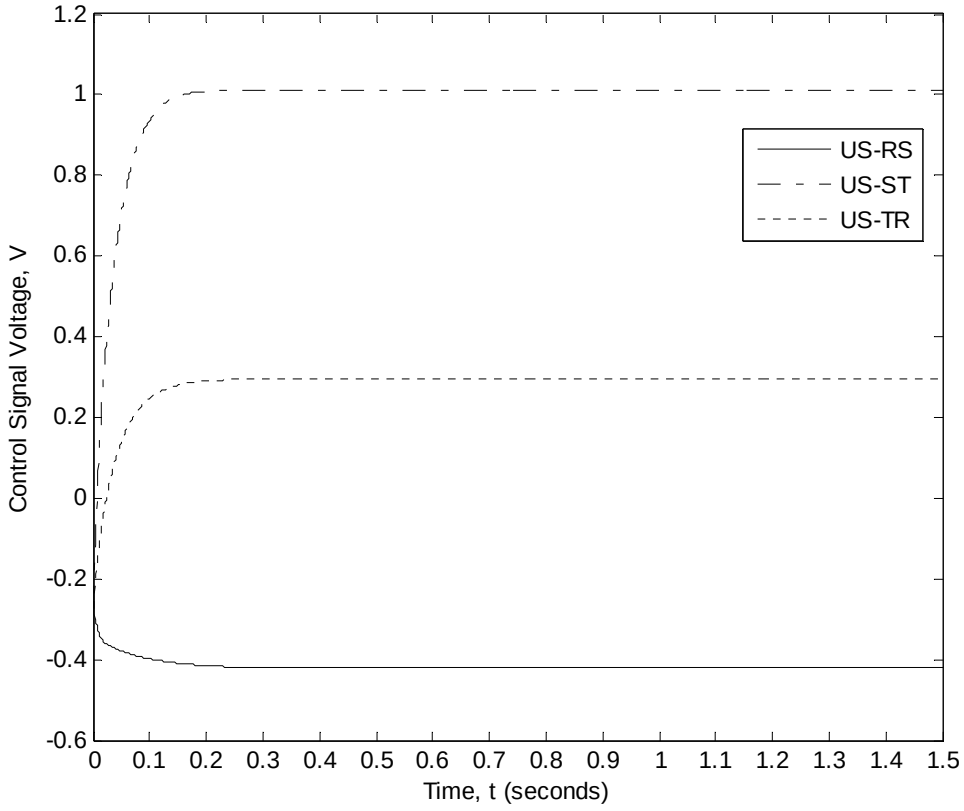
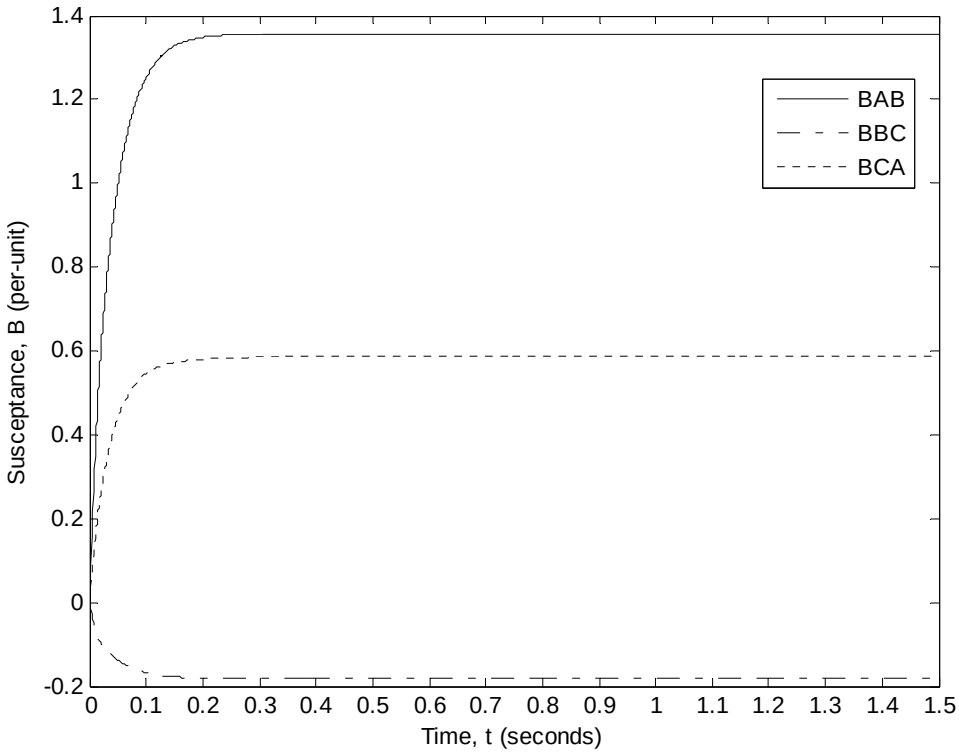


Figure F.2: Model response to 0.5 pu step load applied to B phase (Kp = 1.0, Ki = 100).



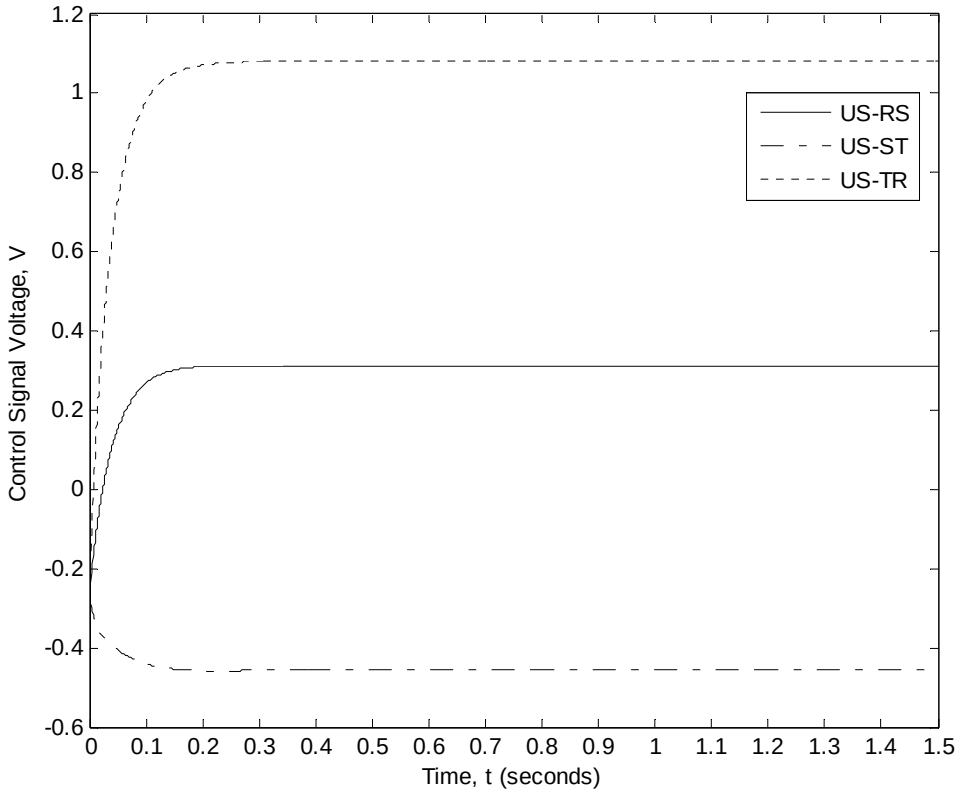


Figure F.3: Model response to 0.5 pu step load applied to C phase (Kp = 1.0, Ki = 100).

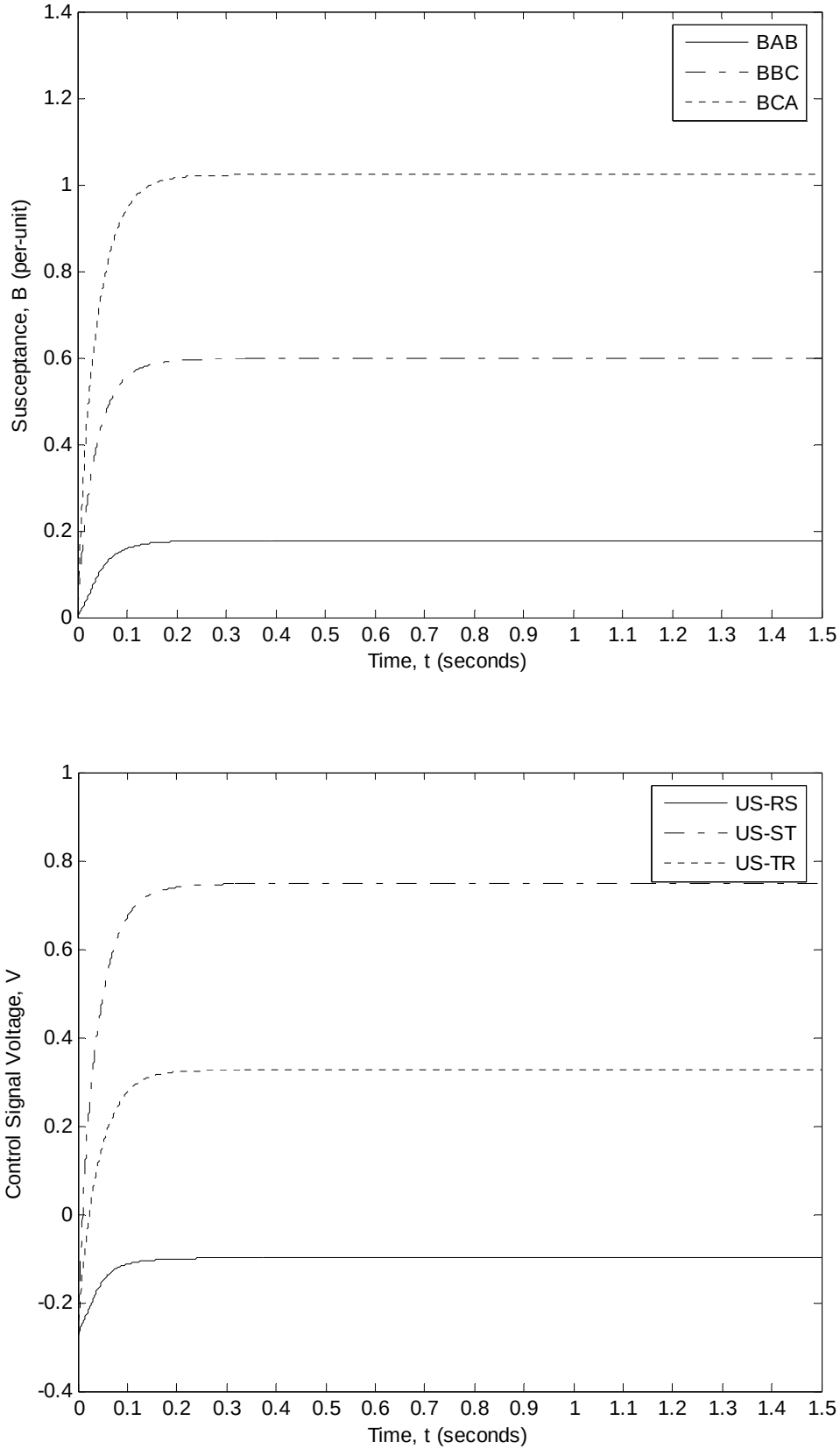


Figure F.4: Model response to step unbalanced load applied to B-C ∅ (Kp = 1.0, Ki = 100).

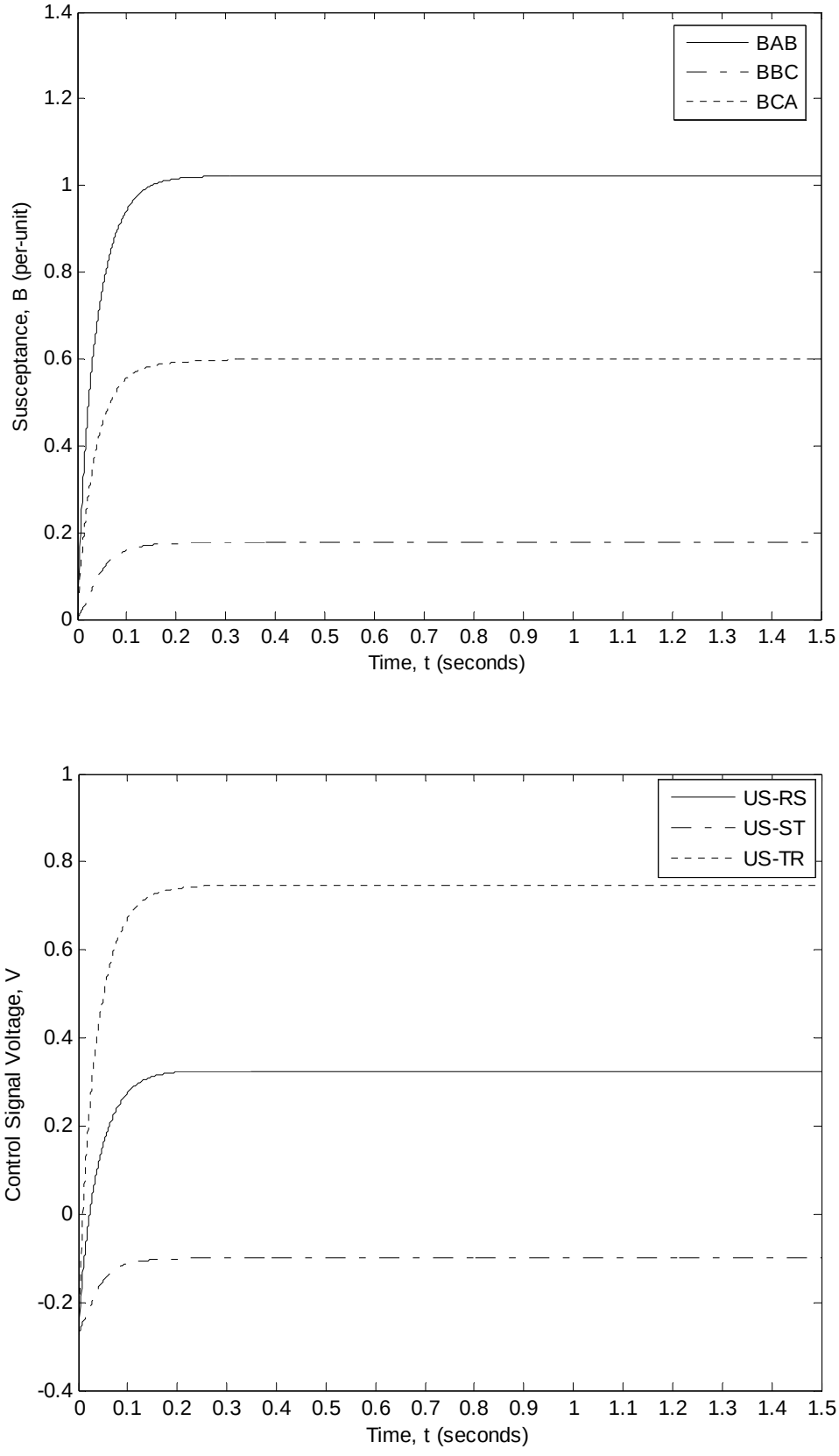
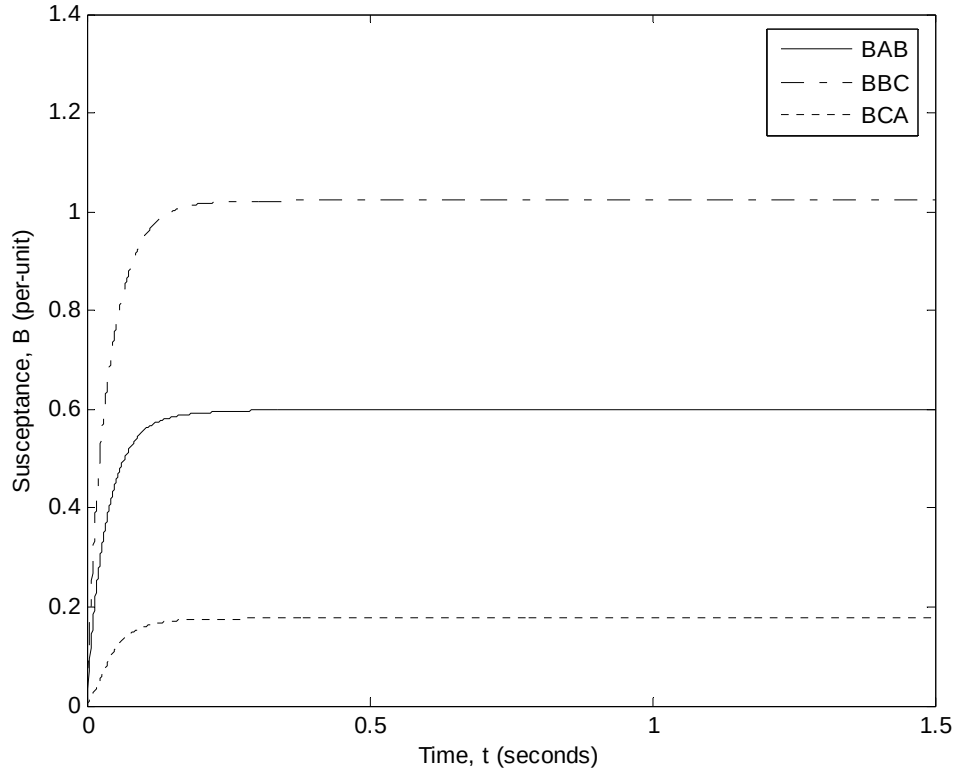


Figure F.5: Model response to step unbalanced load applied to C-A ∅ (Kp = 1.0, Ki = 100).



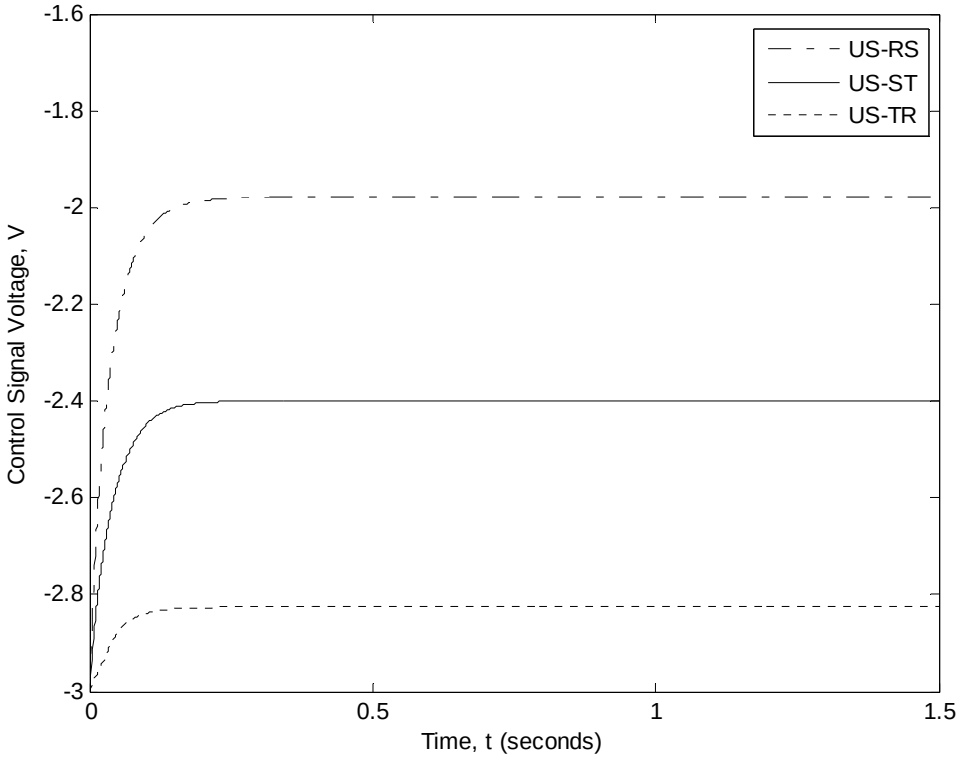


Figure F.6: Model response to step unbalanced load applied to A-B ∅ (Kp = 1.0, Ki = 100).

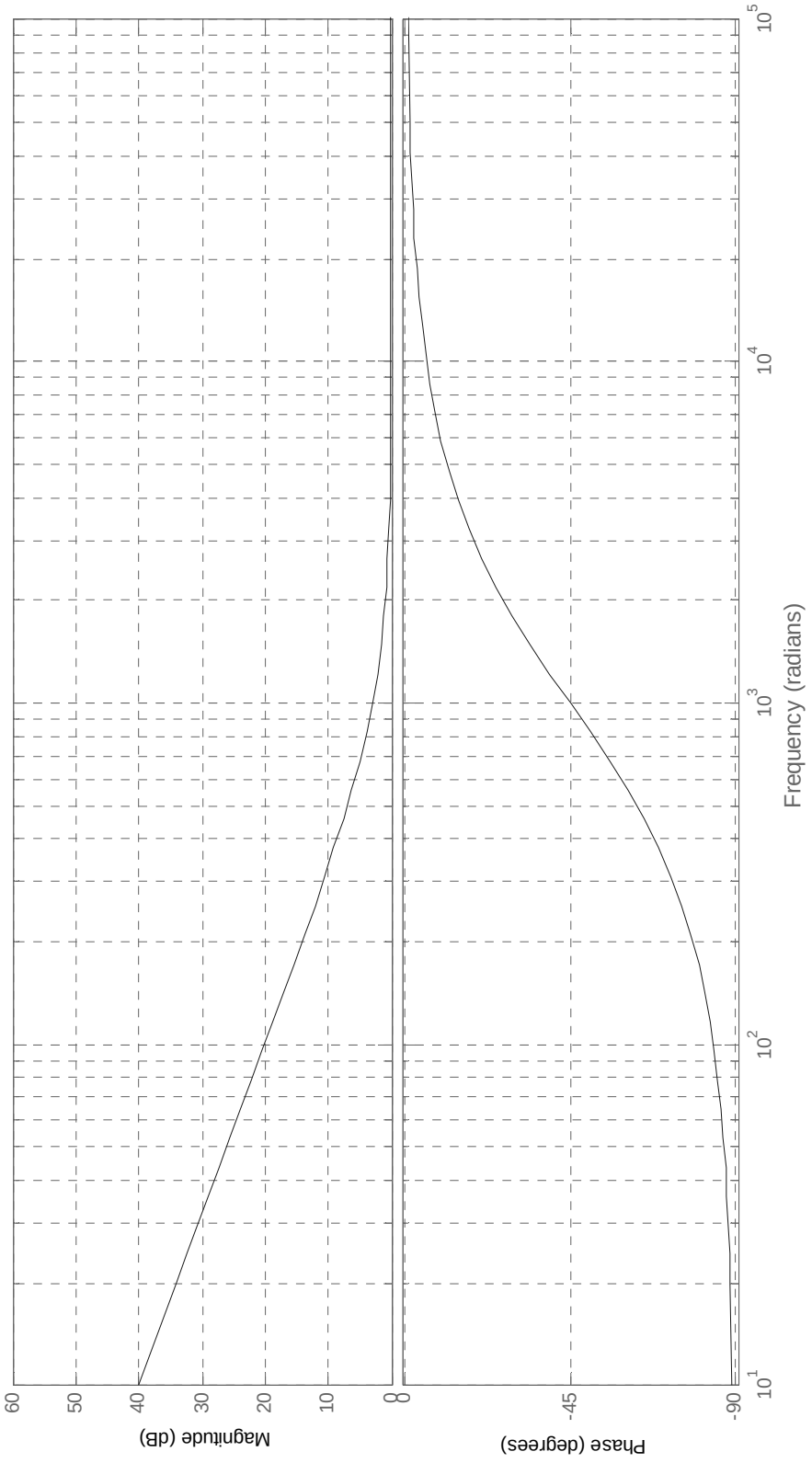


Figure F.7: PI controller transfer function bode plot.

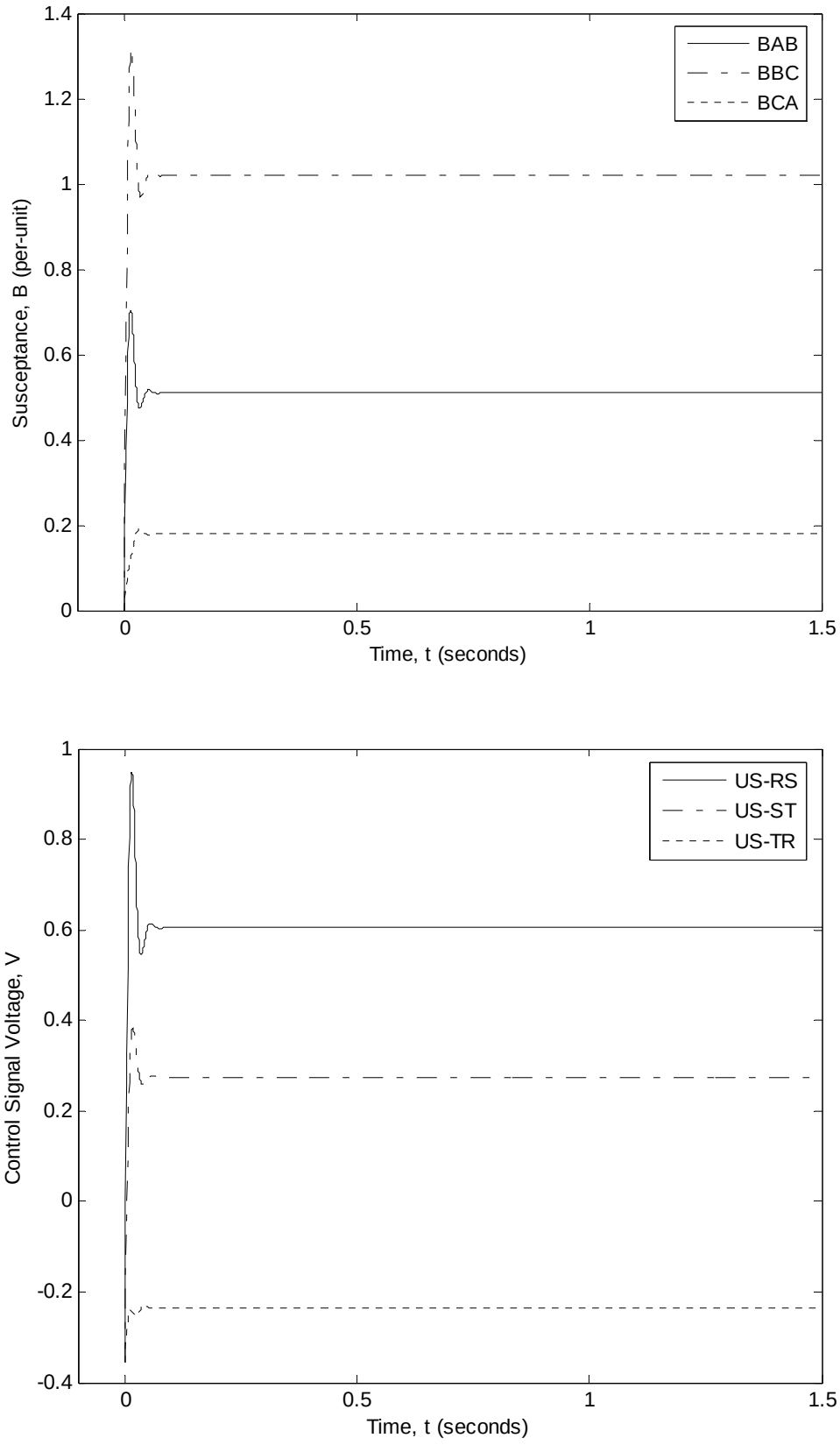


Figure F.8: Model response to step unbalanced load applied to A-B ∅ (Kp = 10, Ki = 1000).

Appendix G

Measured Control System Response Waveforms

Figure G.1: Control system calculated susceptance response to load imbalance, Gain = 5.
Figure G.2: Control system calculated susceptance response to load imbalance, Gain = 6.
Figure G.3: Control system calculated susceptance response to load imbalance, Gain = 7.
Figure G.4: Calculated susceptance response to 0.5 pu step input A-B∅, Gain = 6.
Figure G.5: Calculated susceptance response to 0.5 pu step input B-C∅, Gain = 6.
Figure G.6: Calculated susceptance response to 0.5 pu step input C-A∅, Gain = 6.
Figure G.8: Calculated susceptance response to unbalanced load input, Gain = 6.
Figure G.9: Calculated susceptance response to unbalanced load input, Gain = 7.
Figure G.10: Steinmetz calculated susceptance response to unbalanced load input.
Figure G.11: SVC start sequence.

Waveform trace information:

- Waveform traces marked 1, 2 and 3 are B-REF RS, ST and TR respectively.
- Waveform traces marked 4, 5 and 6 are UAB, UBC and UCA respectively.
- Waveform traces marked 7 and 8 are card YXR-206A TP12 and 13 respectively.

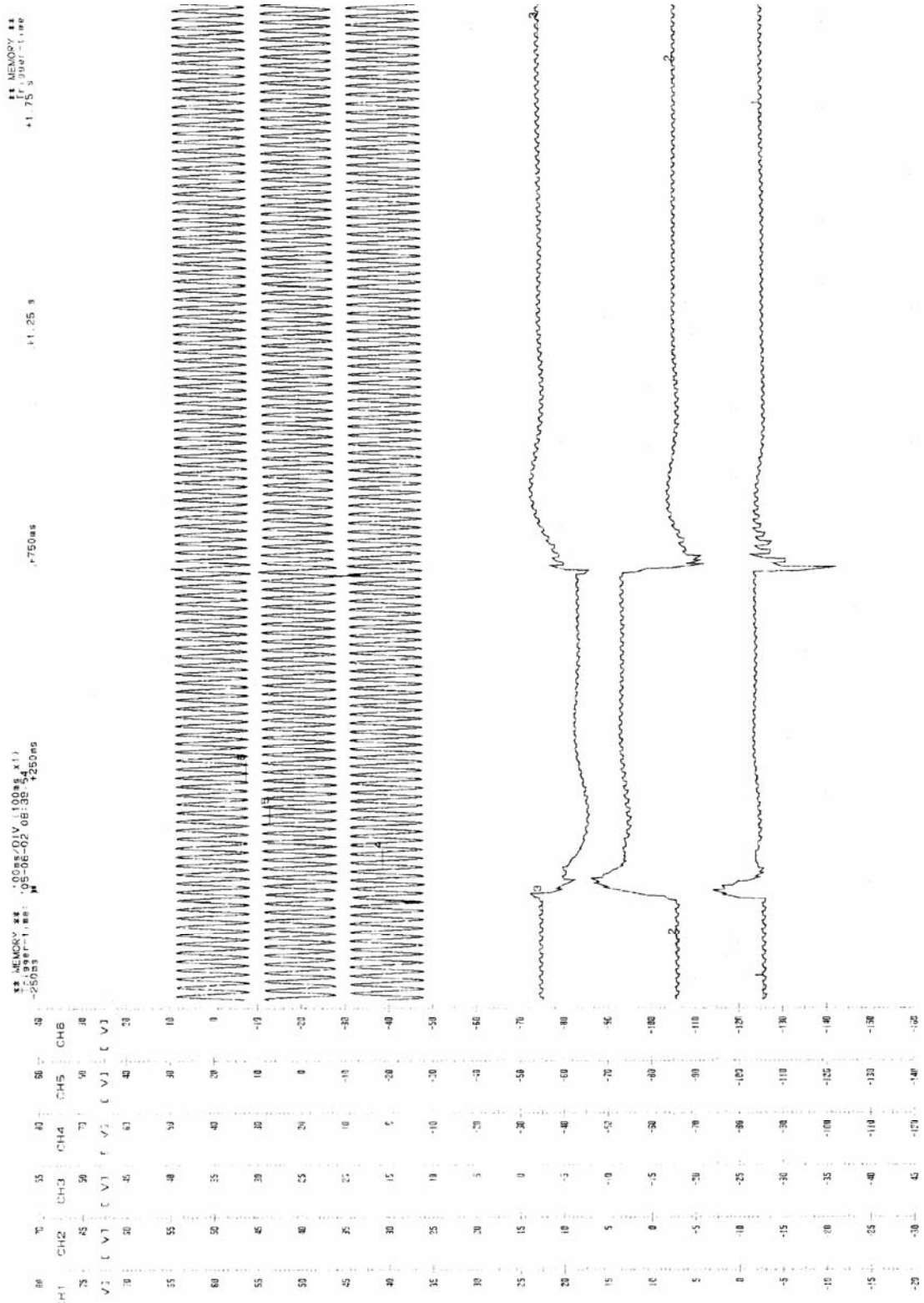


Figure G.1: Control system calculated susceptance response to load imbalance, Gain = 5.

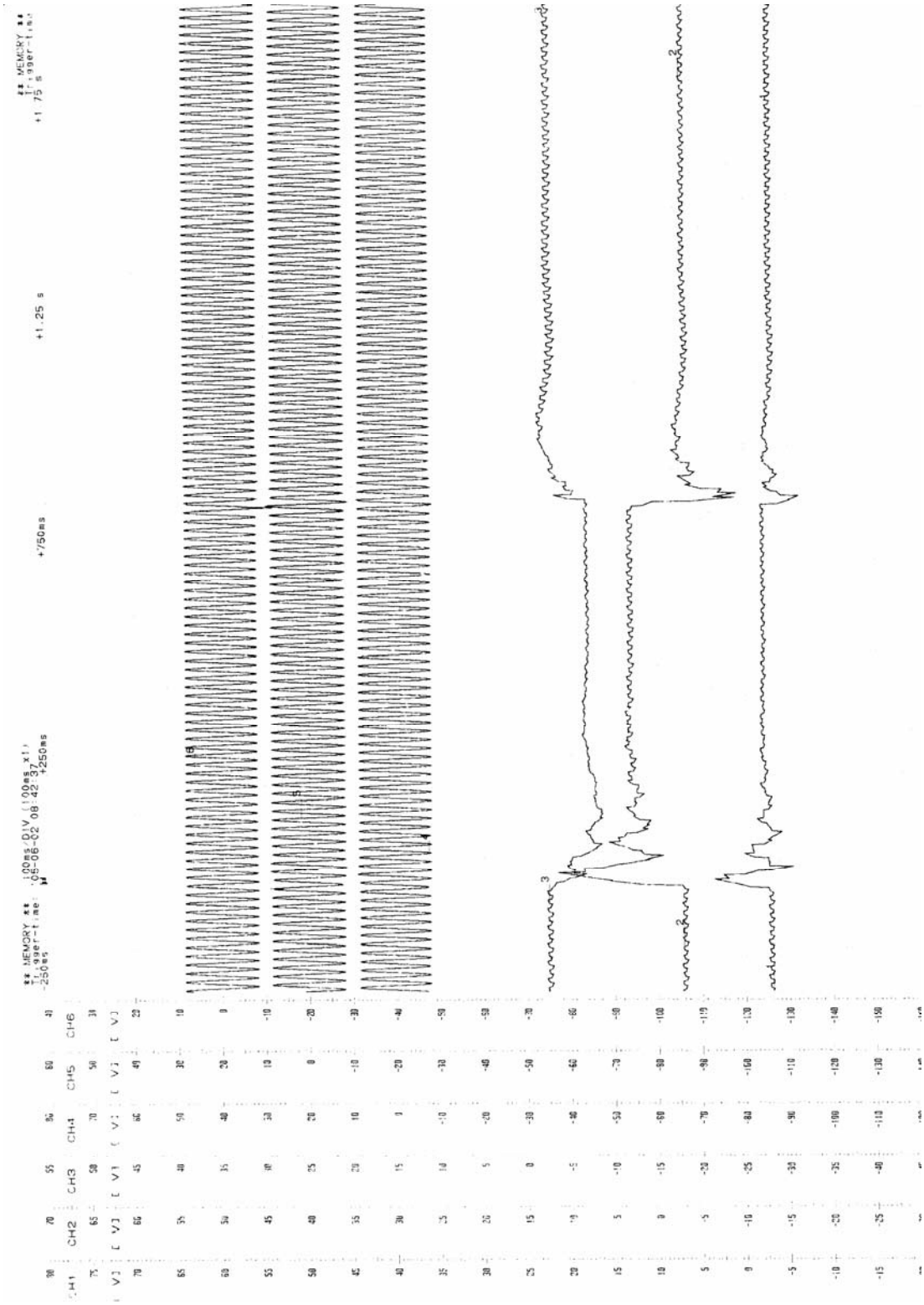


Figure G.2: Control system calculated susceptance response to load imbalance, Gain = 6.

Control system response verges on unstable during some measurements with a voltage regulator gain setting of 6.

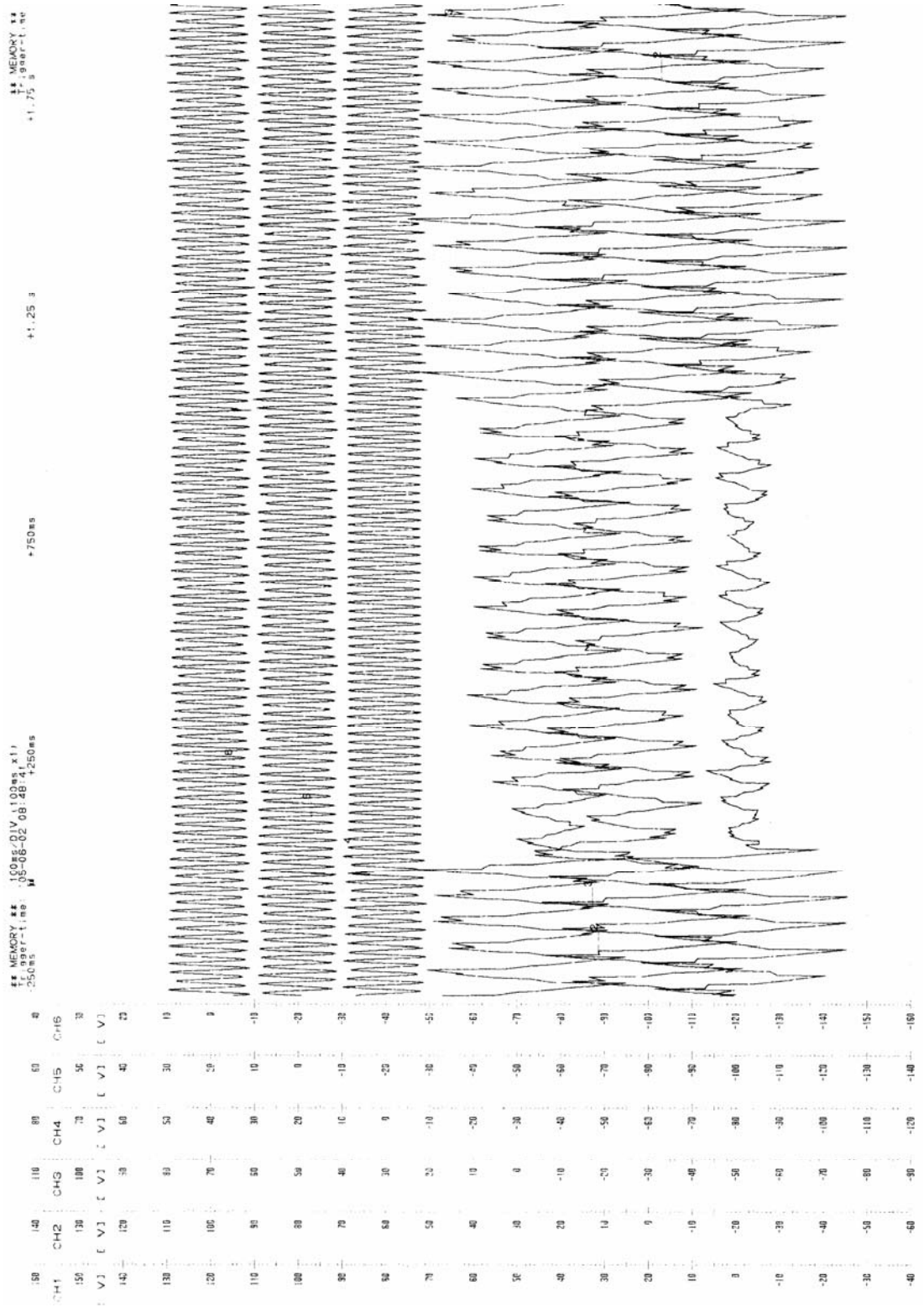


Figure G.3: Control system calculated susceptance response to load imbalance, Gain = 7.

Control system response is unstable.

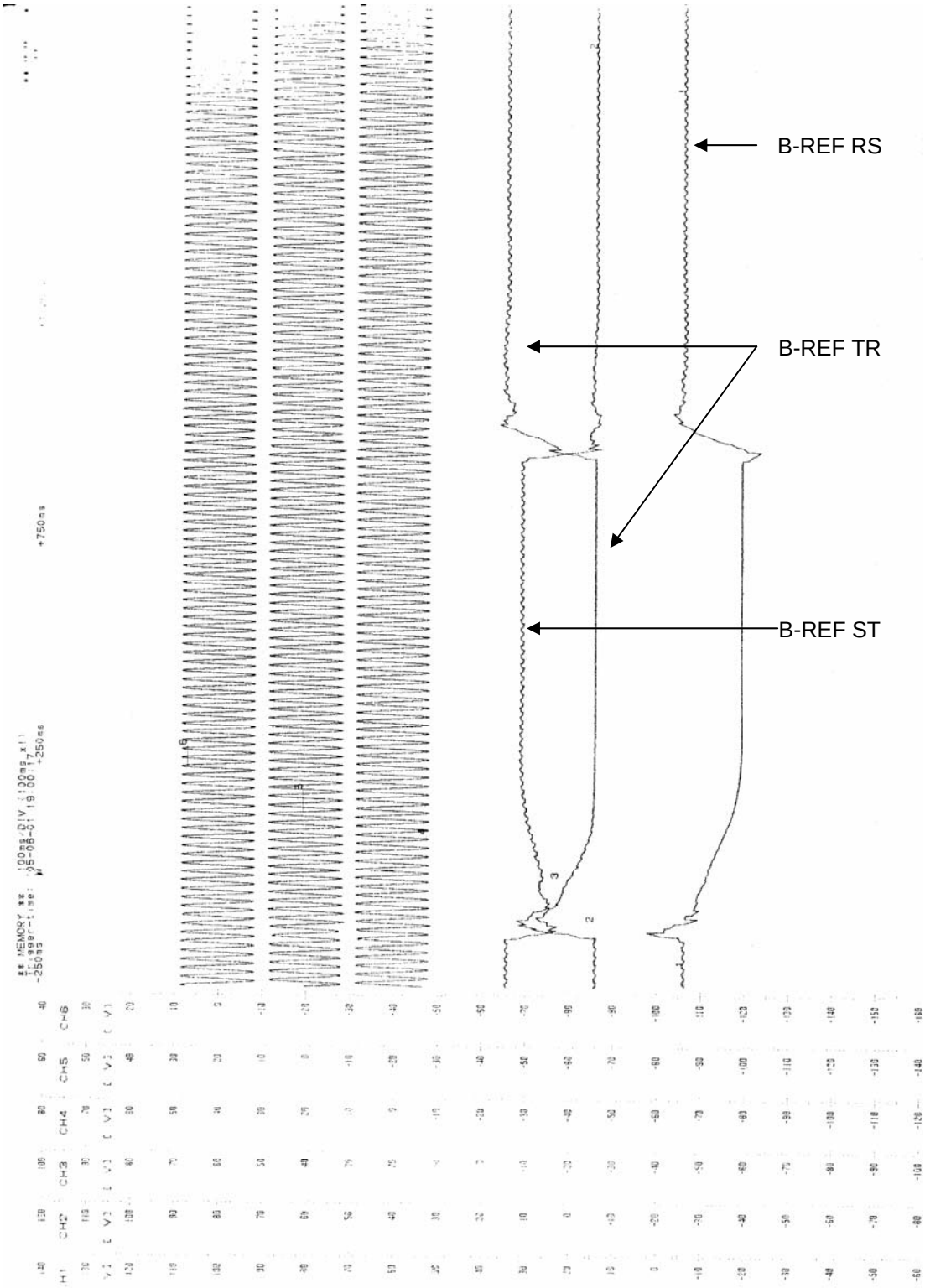


Figure G.4: Calculated susceptance response to 0.5 pu step input A-B∅, Gain = 6.

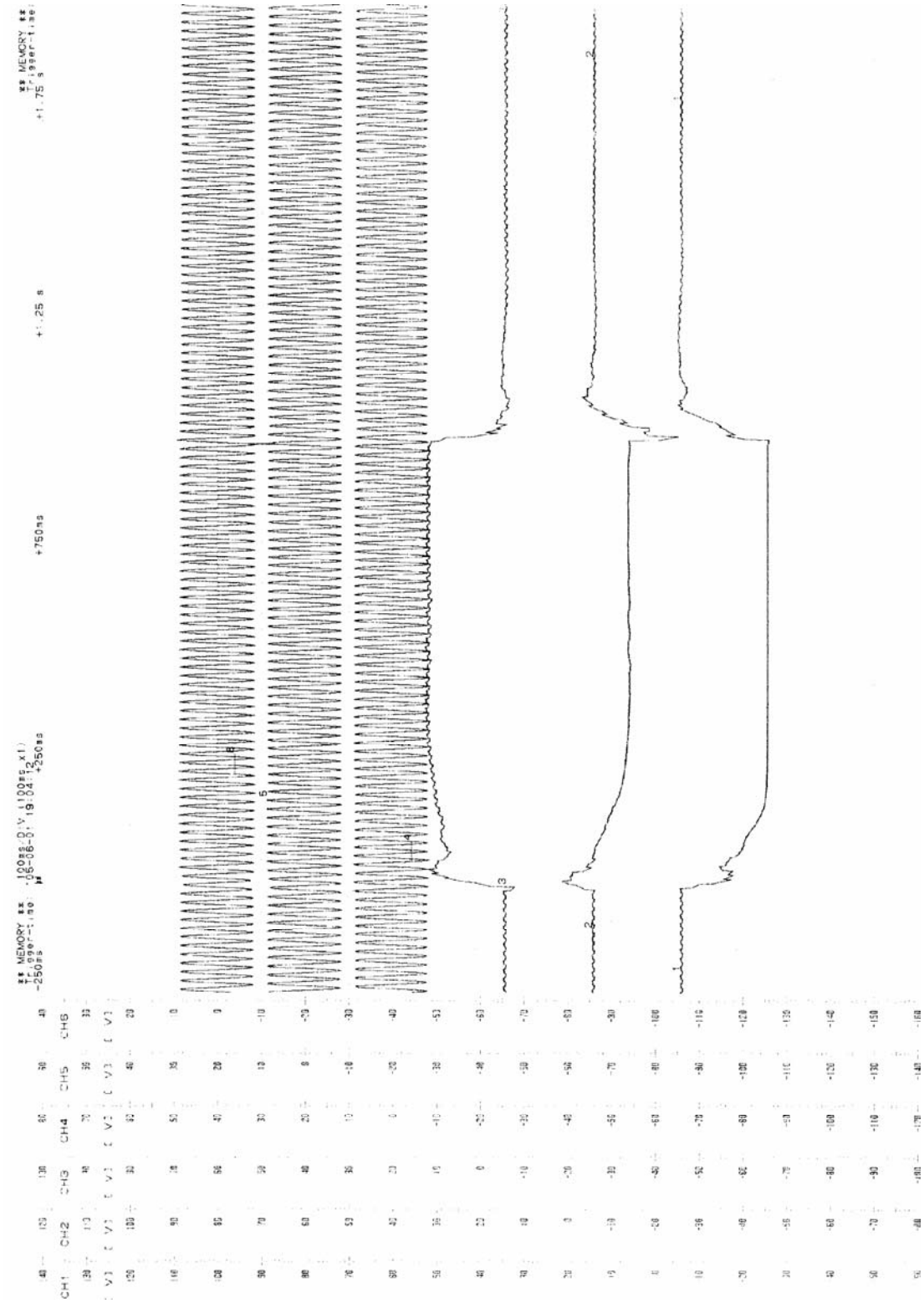


Figure G.5: Calculated susceptance response to 0.5 pu step input B-C∅, Gain = 6.

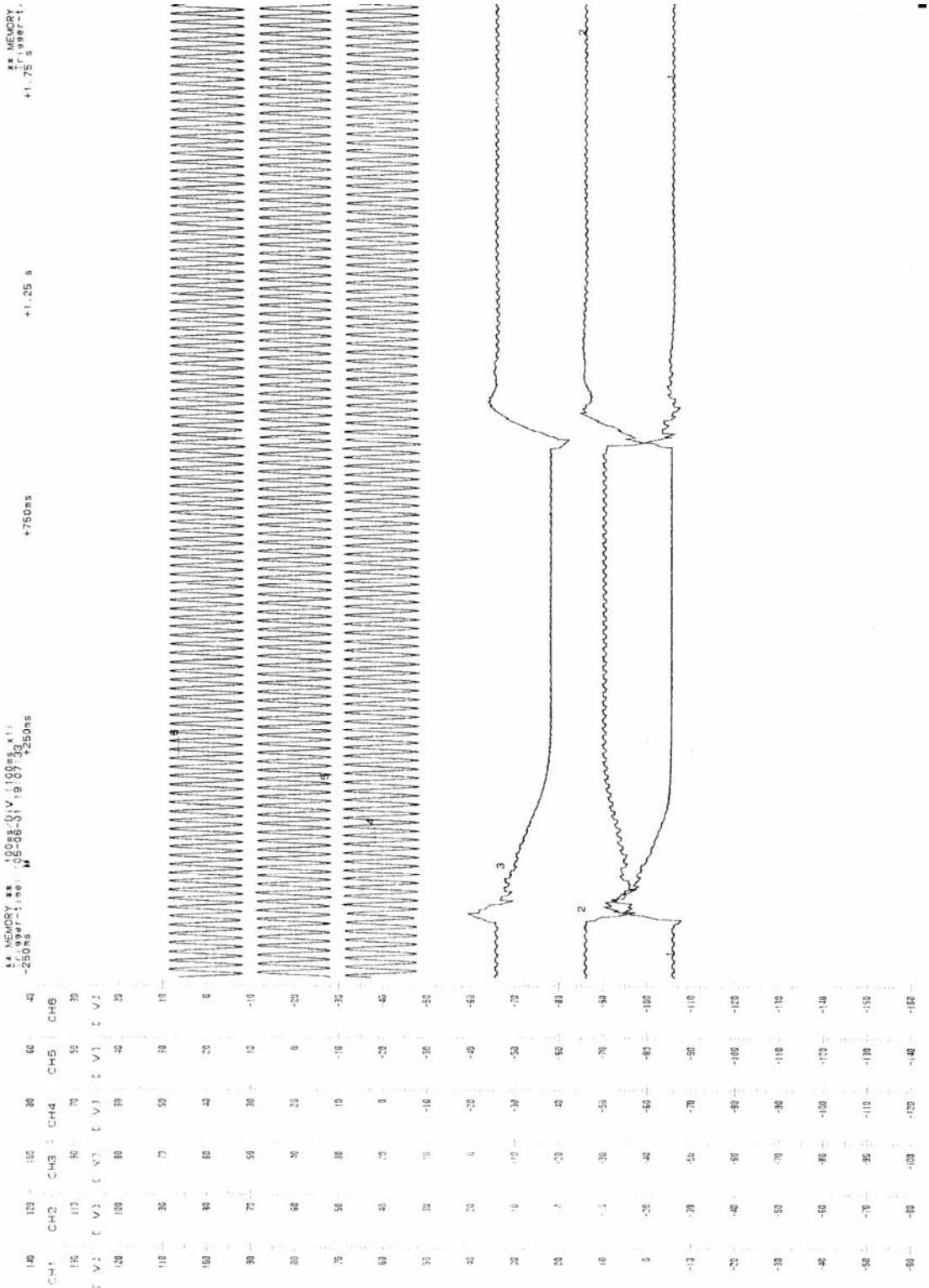


Figure G.6: Calculated susceptance response to 0.5 pu step input C-A∅, Gain = 6.

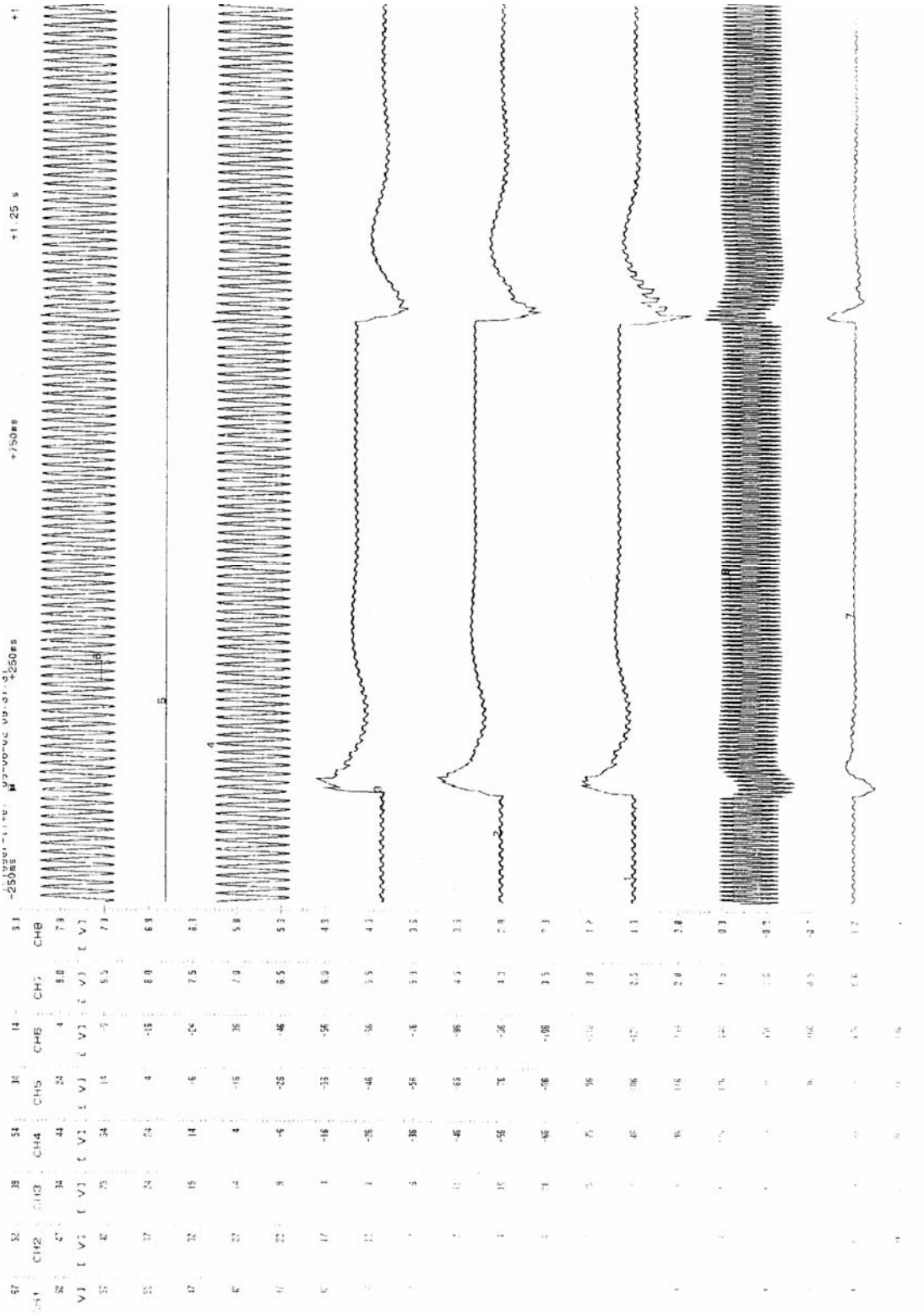


Figure G.7: Calculated susceptance response to unbalanced load input, Gain = 5.

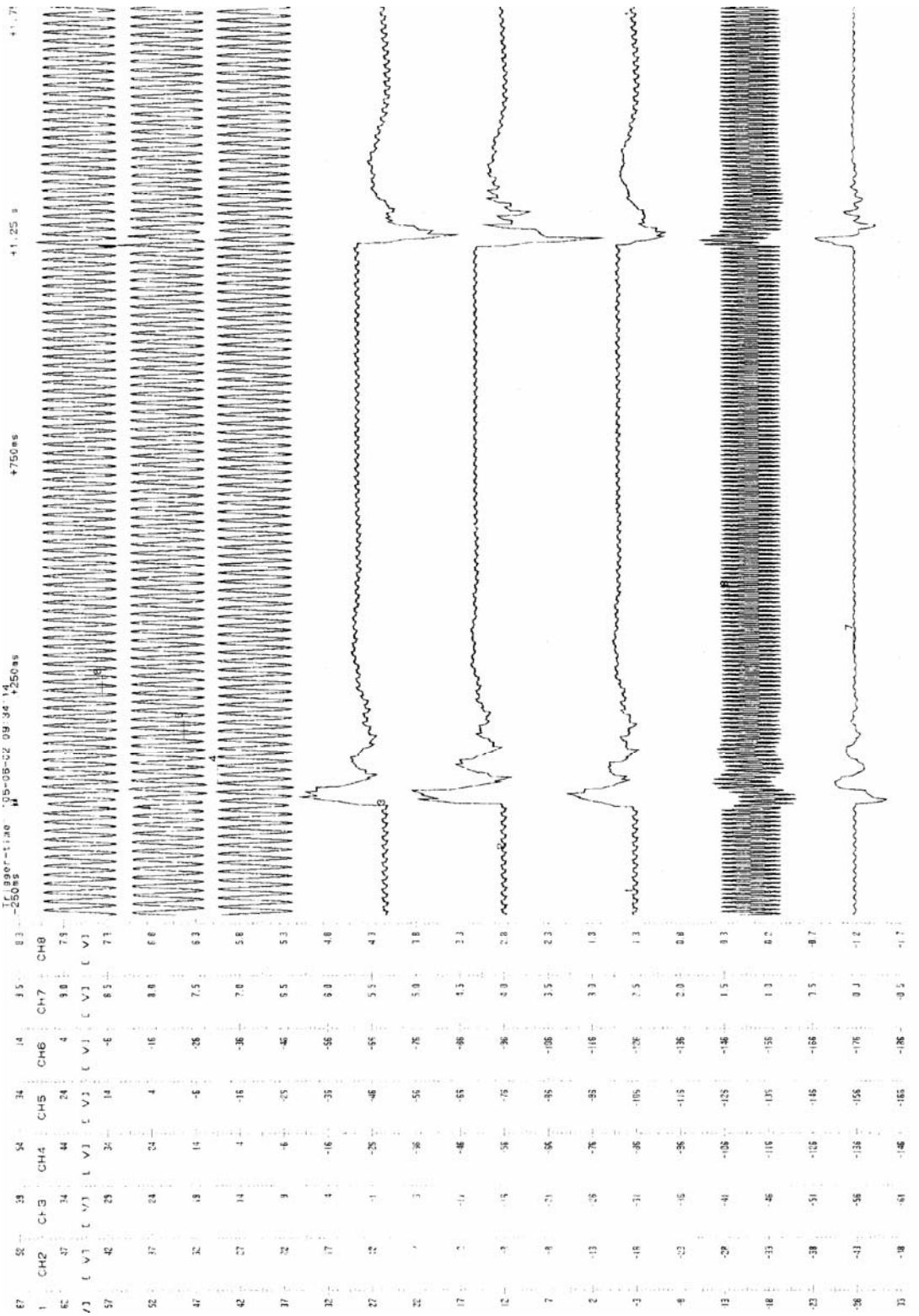


Figure G.8: Calculated susceptance response to unbalanced load input, Gain = 6.

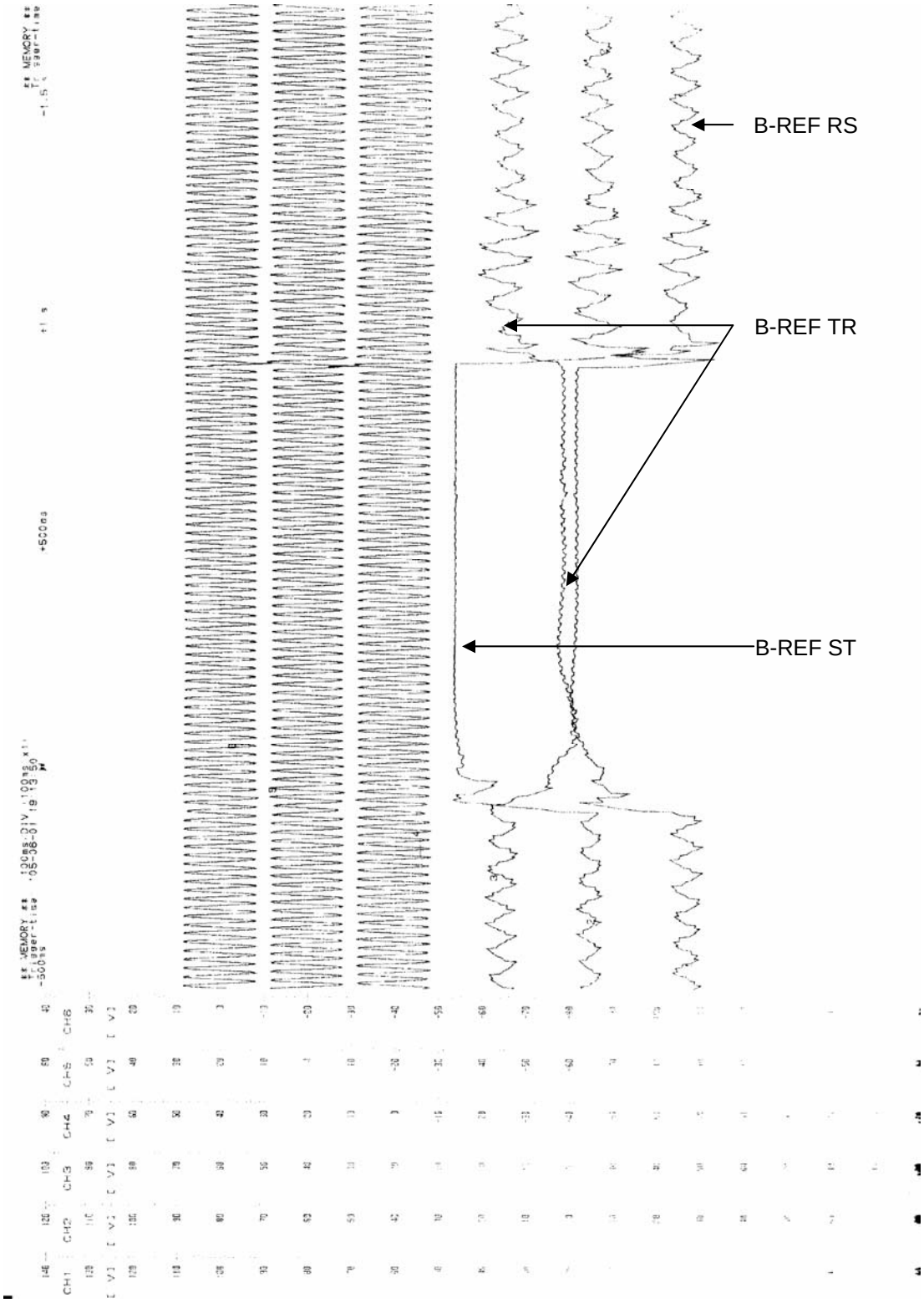


Figure G.9: Calculated susceptance response to unbalanced load input, Gain = 7.

Control system response has reached critical stability.

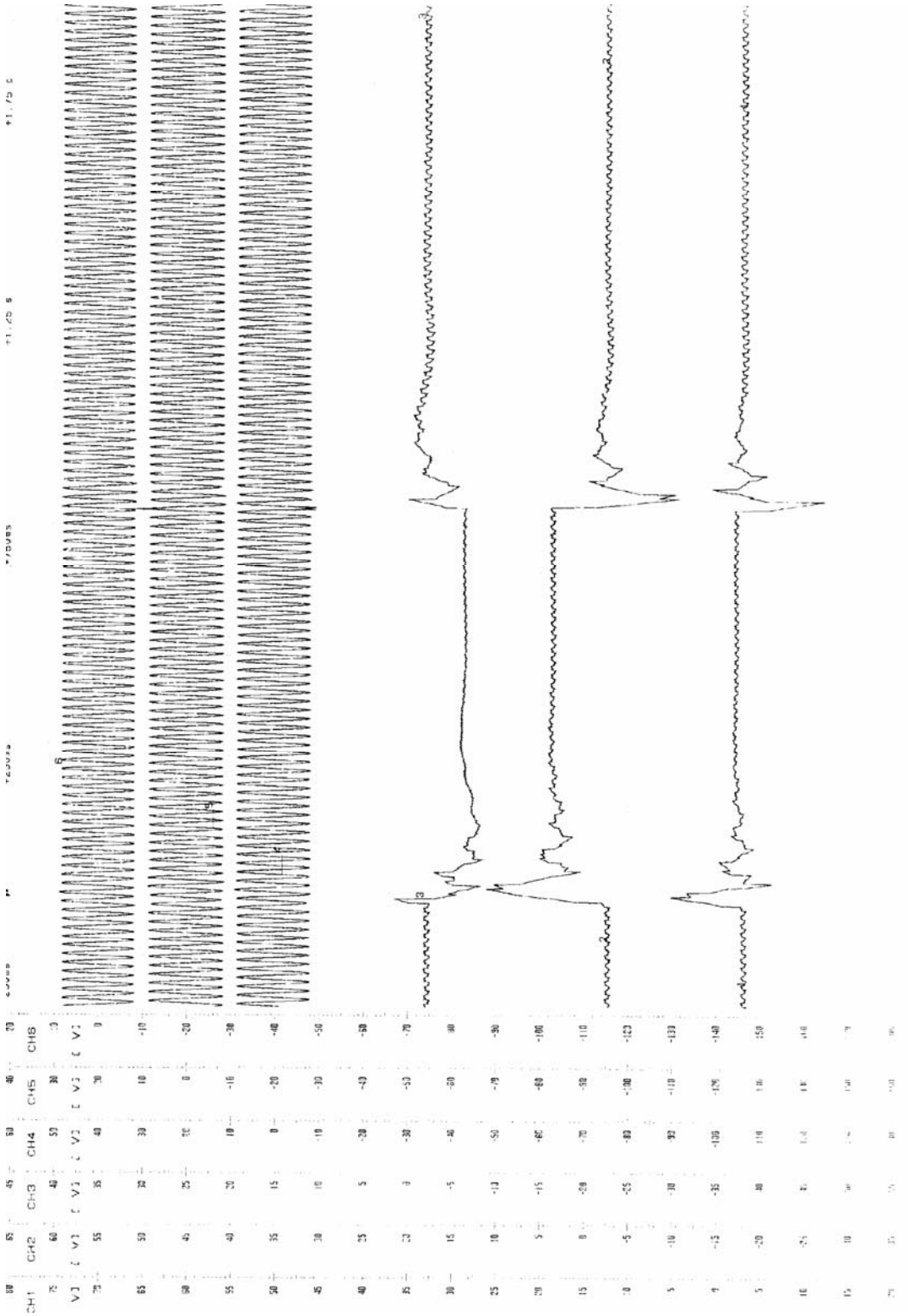


Figure G.10: Steinmetz calculated susceptance response to unbalanced load input.

Control system response is rapid but oscillatory, as the Steinmetz controller is open loop.

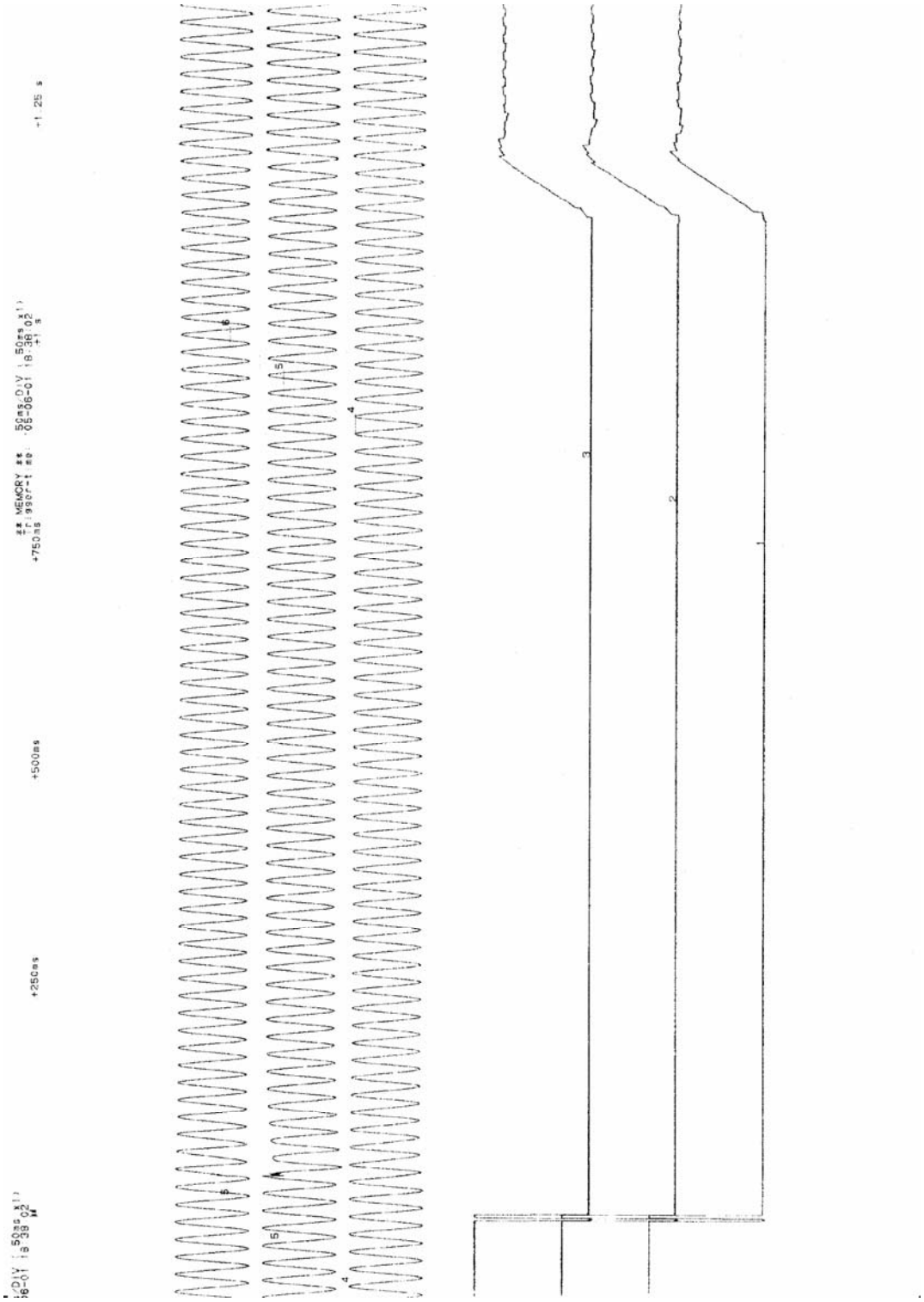


Figure G.11: SVC start sequence.

During SVC start up sequence the thyristors are fully conducted (maximum SVC inductive output) for one second to allow the phase locked loops sufficient time to synchronise with the reference voltage after the SVC is activated (ASEA 1986, p. 34).

Appendix H

H.1: Theoretical modelling of voltage regulation

H.2: Modelling using measured inputs

H.3: MATLAB code for verification

H.1 Theoretical Modelling of Voltage Regulation

The following waveforms were obtained while simulating the theoretical operation of the active rectifier, summing junction, integrator and sample and hold circuits of voltage regulation card YXR 206A. An ideal voltage input of 1.0 per unit phase to phase was input to the regulator simulation to allow verification of the outputs. The following waveforms were obtained for intermediate points prior to and after the specified test points TP12 and TP13.

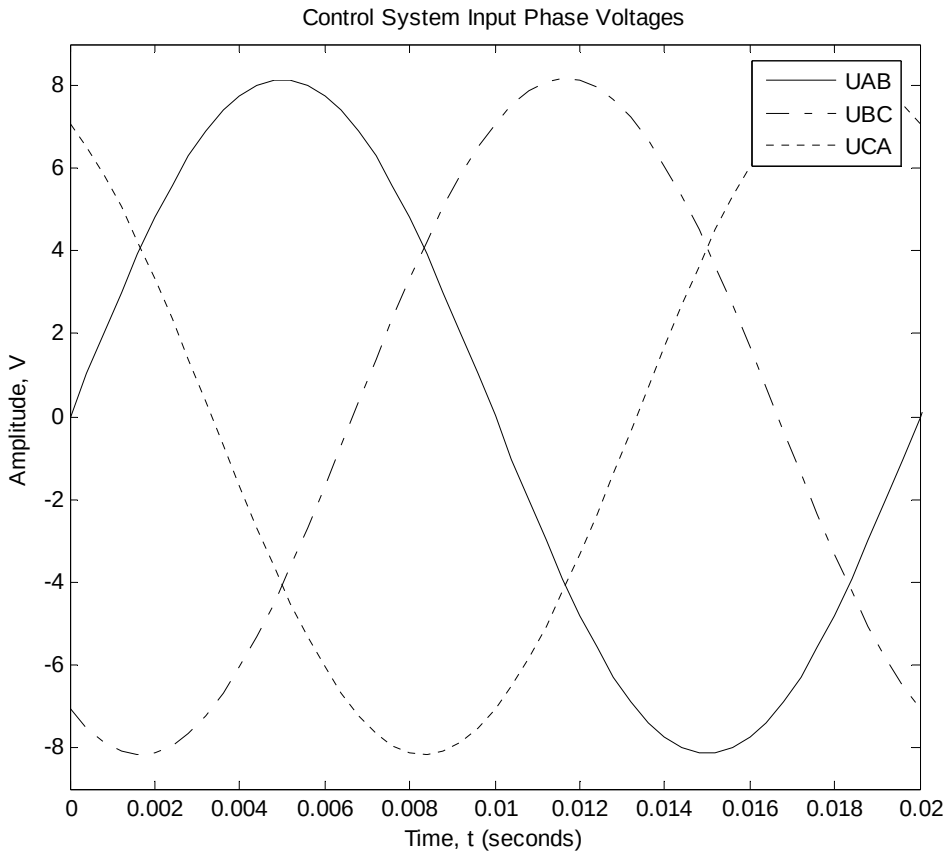


Figure H.1: One cycle simulation of ideal voltage input.

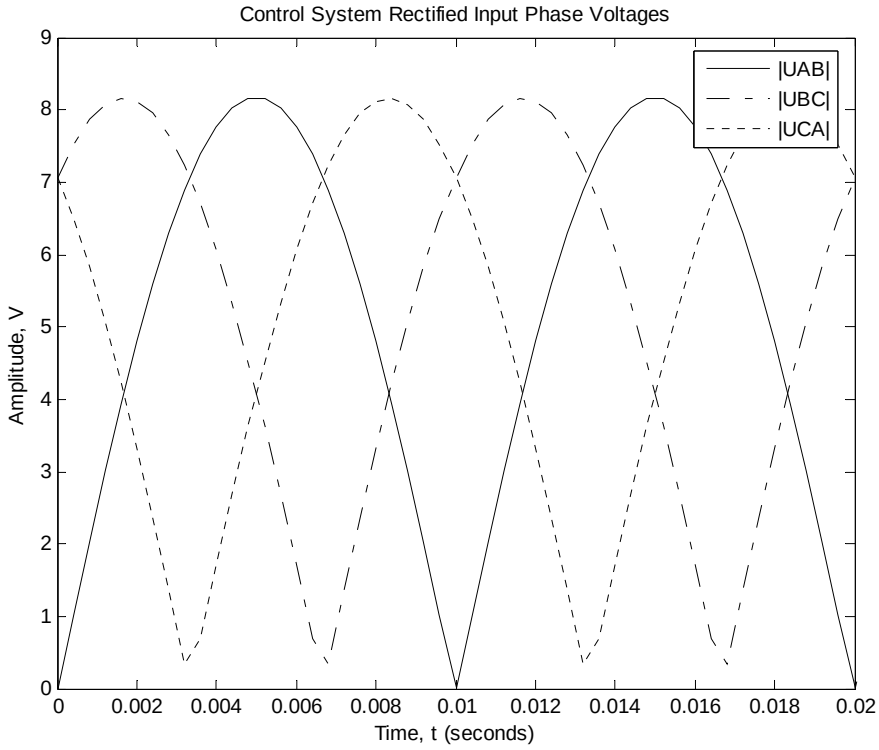


Figure H.2: One cycle simulation of ideal rectified voltage input.

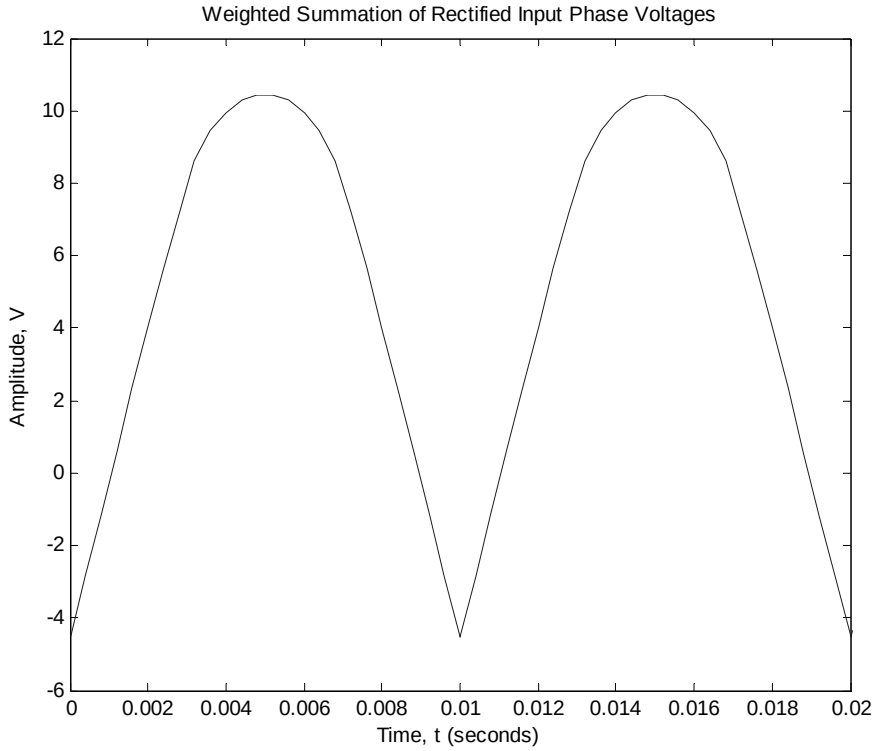


Figure H.3: One cycle simulation of ideal summated voltage input.

H.2 Modelling using Measured Inputs

The following waveforms were obtained while simulating the theoretical operation of the active rectifier, summing junction, integrator and sample and hold circuits of voltage regulation card YXR 206A. Actual measured input voltages were used to allow direct comparison of calculated outputs using the voltage regulation algorithm, and the control signals measured.

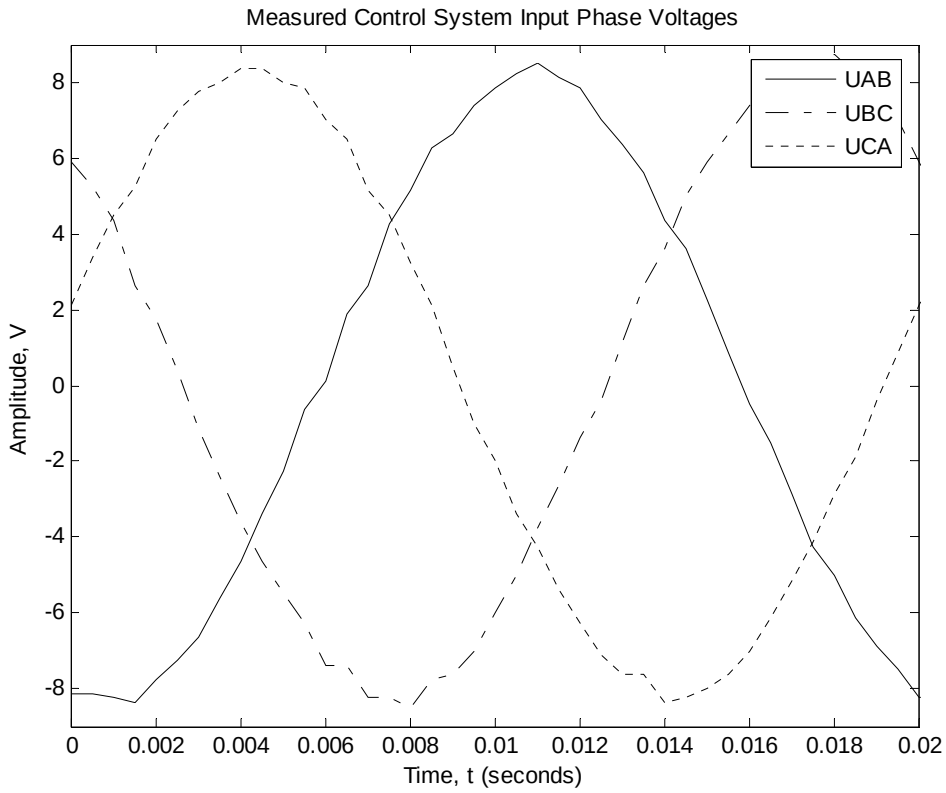


Figure H.4: One cycle of measured voltage input to control system.

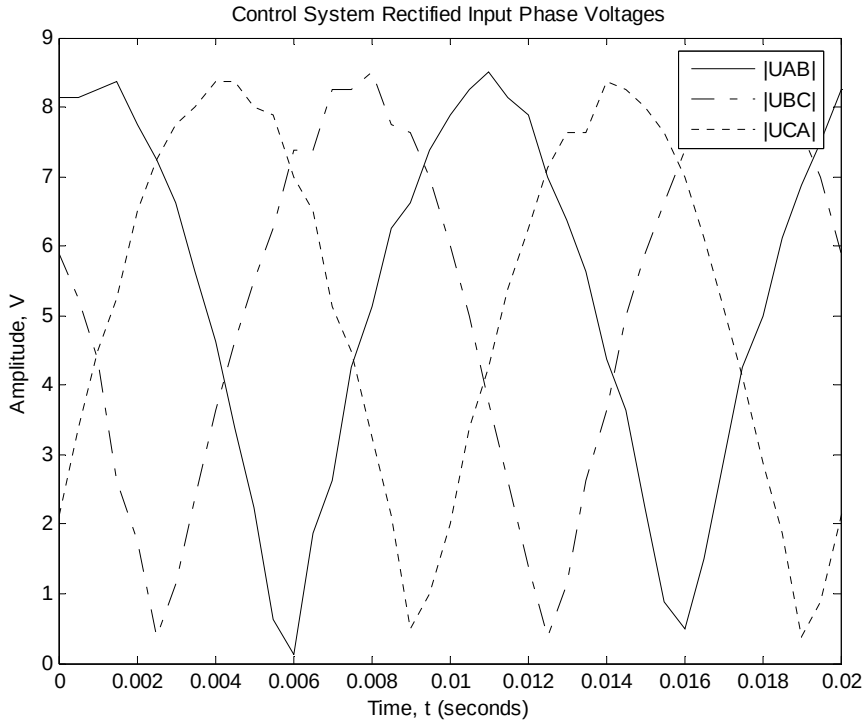


Figure H.5: One cycle of calculated rectification of measured voltage.

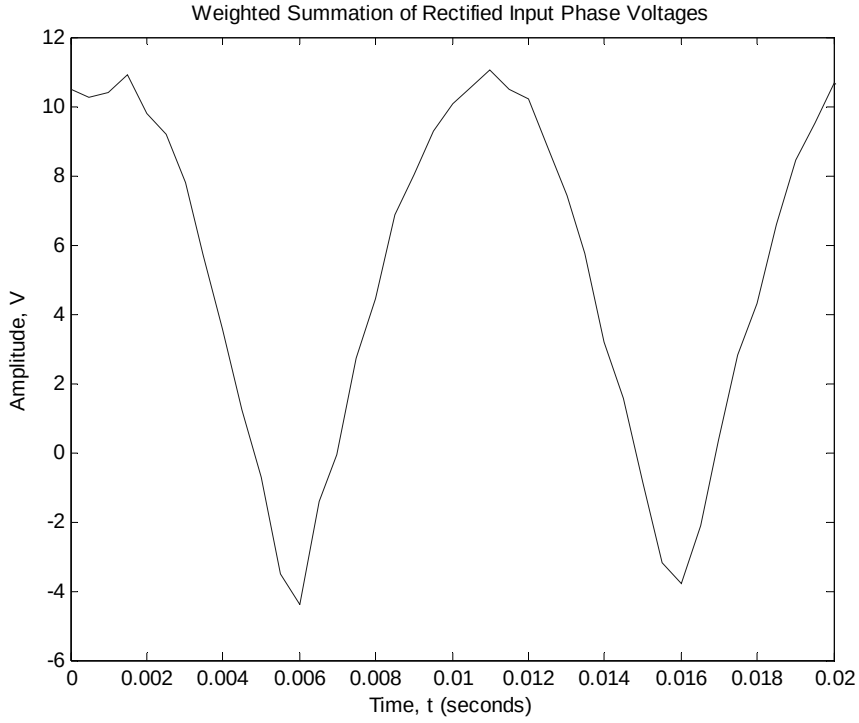


Figure H.6: One cycle of calculated summated rectified voltage.

The following output was obtained from the voltage response simulation script using the measured waveform data during an unbalanced load step input to the control system.

```
Simulating voltage regulator function using measured values:
Average of Summing Junction output = -0.007599
Average of measured Test Point 12 = 0.004529
Average of Integrator and S&H output = -0.000024
Average of measured Test Point 13 = 0.018314
```

Whereas the measured test point TP13 waveform was proven to be noise only and the comparison therefore meaningless, the measured and calculated TP12 values are similar and verify the voltage rectification and summation simulation.

H.3 MATLAB Code

The following MATLAB code was used to manually simulate the measurement and transformation circuitry prior to the input to the PI controller on voltage regulation card YXR 206A. This code was then arranged so as to import experimental data and perform the same simulation operations with actual inputs to the voltage regulation card, and compare the program outputs with those measured at key points.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Script:   YXR_206A
% Input:    Nil
% Output:   Graphical analysis of expected waveforms at key points
%           throughout the SVC control system voltage regulation
%           card YXR206A, for one phase only.
% Purpose:  To verify the modelling algorithms and scaling factors
%           used to model the voltage regulation functional blocks
%           prior to input to the PI controller.
% Source:   K Dawson 0019423038 27/08/05
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all; close all; clc;
format long

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%% Exclusions and Operating Conditions %%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Signals not required: The inductive reference shown as an input to
% the summing junction is only used during SVC start up, where the
% thyristors are fully conducting for the first second of operation.
% This is not within the scope of the simulation, therefore this signal
% is not considered
% The slope of Blackwater SVC control system is set to 0%, therefore
% the slope input to the summing junction need not be considered.
% NPS deadband was set to 0% for experimental testing purposes,
% therefore it need not be considered in the simulation.

% No transmission delays are incorporated for the output of the sample
% and hold function.

% Operating Conditions: It is assumed that the SVC has achieved normal
% operating status (i.e. not in start up or stop mode) and that system
% loading is steady.
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%% Define Theoretical Input Waveforms %%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Define theoretical waveform input to workspace.  10V phase to phase
% (peak) input of UAB, UBS and UCA to the voltage regulator card
% represents 1pu. Therefore each phase waveform will have a peak
% amplitude of 10*(sqrt(2)) / sqrt(3).  The power system frequency is
% 50 Hz.  As the experimental waveform recordings have 2.5 s
% duration with 5001 sample points, this will be matched with
% the theoretical simulation for ease of comparison.

w   =   2 * pi * 50;                    % Define frequency in rad.
x   =   (linspace(0,2.5,5001))';        % 5001 points in x domain

a   =   10 * (sqrt(2)) / (sqrt(3));     % Peak amplitude
uab =   a * sin(w*(x));                 % Define leading phase
ubc =   a * sin(w*(x-(0.02/3)));        %  add phase shift for
uca =   a * sin(w*(x-(2*(0.02/3))));    %  subsequent phases
ff  =   2 / pi;                         % Define form factor

% Therefore 10 V phase to phase input (1 pu) should equal 8.16V peak
% phase to ground waveform, or 5.77 V RMS.
% Dividing by the form factor, 2/pi, gives 5.20 V average.

%----------------- Plot ideal voltage waveform input -----------------%
figure(1)
plot(x,uab,'r',x,ubc,'y',x,uca,'b')
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Control System Input Phase Voltages');
axis([0 0.02 -9 9])
legend('UAB','UBC','UCA')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%% Simulation of Active Rectifier %%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Simulate Rectification of UAB, UBC, UCA voltages, the resultant
% signal is used by the control system to determine voltage response.

uabr    =   abs(uab);                   % Full wave rectification
ubcr    =   abs(ubc);                   % obtains |UAB|,|UBC| and |UCA|
ucar    =   abs(uca);
```

```
%------------ Plot rectified phase voltage waveform inputs -----------%
figure(2)
plot(x,uabr,'r',x,ubcr,'y',x,ucar,'b')
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Control System Rectified Input Phase Voltages');
axis([0 0.02 0 9])
legend('|UAB|','|UBC|','|UCA|')

% It may be observed that the frequency of the waveform has effectively
% doubled, hence the introduction of 100 Hz ripple mentioned in the
% manufacturer's documentation.


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%% Simulation of Summation Block %%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Summing junction for response and reference - the output is the
% difference detected between measured voltage and set voltage, delta V

% The linear range of the op. amps are given in the manufacturer's
% documentation as -5 to +5 volts.  Therefore scaling factors must be
% applied to ensure that the signals remain within this range for
% normal operating conditions.

% The summation block is to produce an average zero output if the input
% voltage and set point voltage are the same per unit value.  It is
% shown with a constant multiplier block attached, stated in the
% manufacturer's documentation as a 1 / 4.98 scaling factor.

% A linear combination of the rectified voltages |UAB|, |UBC| and |UCA|
% is required such that if the set voltage is 1 pu, then the sum of
% the weighted rectified voltage inputs must be equal and opposite in
% magnitude, resulting in a zero summing junction output.
% Abridged schematics (Appendix C) indicate that |UBC| and |UCA| are
% inverted and applied to the summing junction with a weighting of 0.2.

% Manufacturer's documentation states that the FIXED VREF signal, 10V,
% is applied to the voltage regulator with a weighting of 0.5.  The
% VREF signal represents the difference between FIXED VREF and the
% voltage set point.  10V represents 0.1 pu, and the VREF signal is
% applied with a weighting of 0.05.
```

```
%----------- Calculate linear combination weighting factors ----------%

% Using the average waveform value to calculate the weighting factor

avgw    =   a * ff;                     % average = peak x form factor


% calculate coefficients if total linear combination must average 5V.

coeff   =   5 / (0.6 * avgw);           % see Chapter 5, part 5.3.5
coeff2  =   0.2 * coeff;                % coeff for |UBC| and |UCA|


%--------------------- Summate all input signals ---------------------%

% Define reference voltages

fvref   =   10;                         % FIXED VREF voltage
vref    =   0;                          % VREF = 0 when set V = 1.0 pu


% Apply weighting factors calculated for input rectified voltages

u_in    =   (coeff*uabr) - (coeff2*ubcr) - (coeff2*ucar);


% Perform summation with manufacturer's weightings and this should
% simulate the control waveform measured at test point 12 on voltage
% regulation card YXR 206A.  Apply manufacturer's scaling factor.

tp12 =   u_in - (0.5 * fvref) - (0.05 * vref);

tp12    =   tp12 / 4.98;                % apply manufacturer's scaling


%------------ Confirm correctness of summation algorithm -------------%

% Confirm correctness of algorithm and scaling factors - the average of
% the summing junction should equal zero as reference and set voltages
% are equal.

av_tp12   =   sum(tp12) / length(tp12); % Average of tp12 signal

fprintf('\nAverage of Summing Junction output = %6.6f\n\n',av_tp12);

% This is found should be close to zero.  This could be improved by
% increasing sampling rate.  However, 5001 samples will allow direct
% comparison between theoretical and experimental results and is
% therefore retained.
```

```
%------------ Plot weighted summation of rectified voltages ----------%
figure(3)
plot(x,u_in)
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Weighted Summation of Rectified Input Phase Voltages');
axis([0 0.02 -6 12])
%--------------------------------------------------------------------%


%------- Plot output control system waveform of summing junction -----%
figure(4)
plot(x, tp12)
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Output Control Signal Waveform of YXR206A Summing Junction');
axis([0 0.02 -6 6])


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%% Simulation of Integrator and S&H %%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% The output of the integrator and sample & hold blocks is test point
% 13 on card YXR 206A.  This is test point 12 rescaled and with the
% 100 Hz ripple eliminated.

% The input control system waveform is integrated in 10 ms blocks.
% As the time division is 0.5 ms, 20 sample points are required in
% each block.

tp13 =  [];                             % create storage vector
c    =  ones(1,20);                     % create 'hold' block
d    =  0;                              % pointer for sample block no.
dt   =  x(2) - x(1);                    % time increment

% Extract 10ms block and integrate - use trapezoidal integration.
% Add 1st and last samples and two times all points inside this
% range, multiplied by the time increment and divided by 2.
```

```
for n = 1:250                          % 250 samples of 10ms blocks
    outer   =   tp12((d*20)+1) + tp12(n*20);
    inner   =   (sum(tp12(((d*20)+2):((n*20)-1))));

    int_tp12 =  (outer + inner) * dt / 2;

    h       =   (int_tp12).* c;        % hold value for 10 ms
    tp13    = [tp13 h];                % concatenate blocks
    d       = d + 1;                   % increment pointer
end

% As the number of sample points, 5001, is not neatly divided into
% 10 ms blocks, the one lost point will have to be re-instated to
% maintain correct vector length.

tp13    =   [tp13 tp13(5000)];         % add last integrated point


%------- Apply circuit gains and manufacturer's scaling factors ------%
% Integrator block has gain = - 4.5454546 (See Chapter 5 section 5.3.5)

tp13    =   tp13 .* (- 4.5454546);

% According to available circuitry details, the output of the
% integrator and sample and hold process has a further scaling factor
% applied by an inverting amplifier prior to TP13 on card YXR 206A.

R1  =   150;                           % k ohms
R2  =   22;                            % k ohms
ia_gain =   - (R2 / R1);               % Gain = - 0.147
tp13    =   tp13 .* ia_gain;


%------- Confirm correctness of integration and S&H algorithm --------%

% Confirm correctness of algorithm and scaling factors - the average of
% the integrator and sample and hold blocks should equal zero as
% reference and set voltages are equal.

av_tp13   = sum(tp13) / length(tp13);   % Find average of TP13 signal
fprintf('Average of Integrator and S&H output = %6.6f\n\n\n',av_tp13);

% The input to the PI controller (TP 13) should be equal to zero when
% set and measured voltages are the same.  The average of TP13 should
% be close to zero.
```

```
% Some accumulating error is observed toward the end of the 2 second
% period, but it is very small in magnitude and likely due to sampling
% rate and round off error in the coefficients.

%---- Plot output control system waveform of integration and S&H -----%
figure(5)
plot(x,tp13)
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Output Waveform of YXR206A Integrator and Sample & Hold Block');

%------------------- END OF THEORETICAL MODELLING --------------------%


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%% Comparison with Experimental Results %%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

disp('Simulating voltage regulator function using measured values:')

load bwsvcman                           % Load SVC measurements

Time    =   Point * 0.0005;             % Recreate time scale from info

%---------------- Plot actual voltage waveform input -----------------%
figure(6)
plot(Time,UAB1,'r',Time,UBC1,'y',Time,UCA1,'b')
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Measured Control System Input Phase Voltages');
axis([0 0.02 -9 9])
legend('UAB','UBC','UCA')


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%% Simulation of Active Rectifier %%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Simulate Rectification of measured UAB, UBC, UCA voltages.

UABr    =   abs(UAB1);                   % Full wave rectification
UBCr    =   abs(UBC1);                   % obtains |UAB|,|UBC| and |UCA|
UCAr    =   abs(UCA1);
```

```
%------------ Plot rectified phase voltage waveform inputs -----------%
figure(7)
plot(Time,UABr,'r',Time,UBCr,'y',Time,UCAr,'b')
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Control System Rectified Input Phase Voltages');
axis([0 0.02 0 9])
legend('|UAB|','|UBC|','|UCA|')

% The 100 Hz ripple may be observed in measured waveform.


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%% Simulation of Summation Block %%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Output is the difference detected between measured voltage and set
% voltage, delta V

% F-VREF will again be 10 V.  However, VREF was measured and actual
% value will be input to calculation, as the control system set voltage

FVREF   =   10.*(ones(length(VREF),1));

% Apply weighting factors calculated for input rectified voltages

U_IN    =   (coeff.*UABr) - (coeff2.*UBCr) - (coeff2.*UCAr);

% Perform summation with manufacturer's weightings and this should
% approximately equal the control waveform measured at test point 12
% on voltage regulation card YXR 206A.

TP12 =   U_IN - (0.5 .* FVREF) - (0.05 .* VREF);

TP12    =   TP12 / 4.98;               % apply manufacturer's scaling

%------------ Confirm correctness of summation algorithm -------------%

% The average of the summing junction should equal zero.  This will be
% approximate only using experimental data.

% This will be verified against the average of the measured signal.
```

```
AV_TP12   =   sum(TP12) / length(TP12); % Average of calc tp12 signal
                                        % Average of measured signal
GMI     =   sum(GainMeasIn) / length(GainMeasIn);

fprintf('\nAverage of Summing Junction output = %6.6f\n\n',AV_TP12);
fprintf('Average of measured Test Point 12 = %6.6f\n\n',GMI);

% These should both be close to zero.  There will be some error due to
% sampling rate and the likely variations in system load during
% measurements, and the transmission delay not allowed for.

%------------ Plot weighted summation of rectified voltages ----------%
figure(8)
plot(Time,U_IN)
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Weighted Summation of Rectified Input Phase Voltages');
axis([0 0.02 -6 12])
%--------------------------------------------------------------------%

%------- Plot output control system waveform of summing junction -----%
figure(9)
plot(Time, TP12, Time, GainMeasIn)
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Output Control Signal Waveform of YXR206A Summing Junction');
axis([0 0.02 -6 6])
legend('Calculated','Measured')


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%% Simulation of Integrator and S&H %%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% The output of the integrator and sample & hold blocks is test point
% 13 on card YXR 206A.  This is test point 12 rescaled and with the
% 100 Hz ripple eliminated.

% The input control system waveform is integrated in 10 ms blocks.
% As the time division is 0.5 ms, 20 sample points are required in
% each block.
```

```
TP12   = TP12';                          % convert to row vector
TP13 = [];                               % create storage vector
C   =   ones(1,20);                      % create 'hold' block
D   = 0;                                 % pointer for sample block no.
DT  =   Time(2) - Time(1);               % calculate time increment

for N = 1:250                            % 250 samples of 10ms blocks

    Outer   =   TP12((D*20)+1) + TP12(N*20);
    Inner   =   (sum(TP12(((D*20)+2):((N*20)-1))));

    INT_TP12 =  (Outer + Inner) * DT / 2;

    H       =   (INT_TP12).* C;          % hold value for 10 ms
    TP13    = [TP13 H];                  % concatenate blocks
    D       = D + 1;                     % increment pointer

end

% As the number of sample points, 5001, is not neatly divided into
% 10 ms blocks, the one lost point will have to be re-instated to
% maintain correct vector length.

TP13    =   [TP13 TP13(5000)];           % add last integrated point

%------- Apply circuit gains and manufacturer's scaling factors ------%

% Integrator block has gain = - 4.5454546 (See Chapter 5 section 5.3.6)

TP13    =   TP13 .* (- 4.5454546);

% According to available circuitry details, the output of the
% integrator and sample and hold process has a further scaling factor
% applied by an inverting amplifier prior to TP13 on card YXR 206A.

TP13    =   TP13 .* ia_gain;

%------- Confirm correctness of integration and S&H algorithm --------%

% The average of the integrator and sample & hold blocks should equal
% zero.  This will be approximate only using experimental data.

% This will be verified against the average of the measured TP13
```

```
AV_TP13   = sum(TP13) / length(TP13);   % Find average of TP13 signal
GMO =   sum(GainMeasOut) / length(GainMeasOut);


fprintf('Average of Integrator and S&H output = %6.6f\n\n',AV_TP13);
fprintf('Average of measured Test Point 13 = %6.6f\n\n',GMO);


% These should both be close to zero.  There will be some error due to
% sampling rate and the likely variations in system load during
% measurements, and the transmission delay not allowed for.


%----- Plot calculated and measured integration and S&H output -------%

% Convert other waveforms to row vectors to match integrator output

figure(10)
plot(Time',TP13,Time',GainMeasOut')
xlabel('Time, t (seconds)')
ylabel('Amplitude, V')
title('Output Waveform of YXR206A Integrator and Sample & Hold Block');
legend('Calculated','Measured')
axis([0 0.1 -0.05 0.05])

%------------------- END OF ALGORITHM VERIFICATION -------------------%
```

Appendix I

Revised SVC control system model

- Model Overview
- Specific detail of Voltage Regulator model

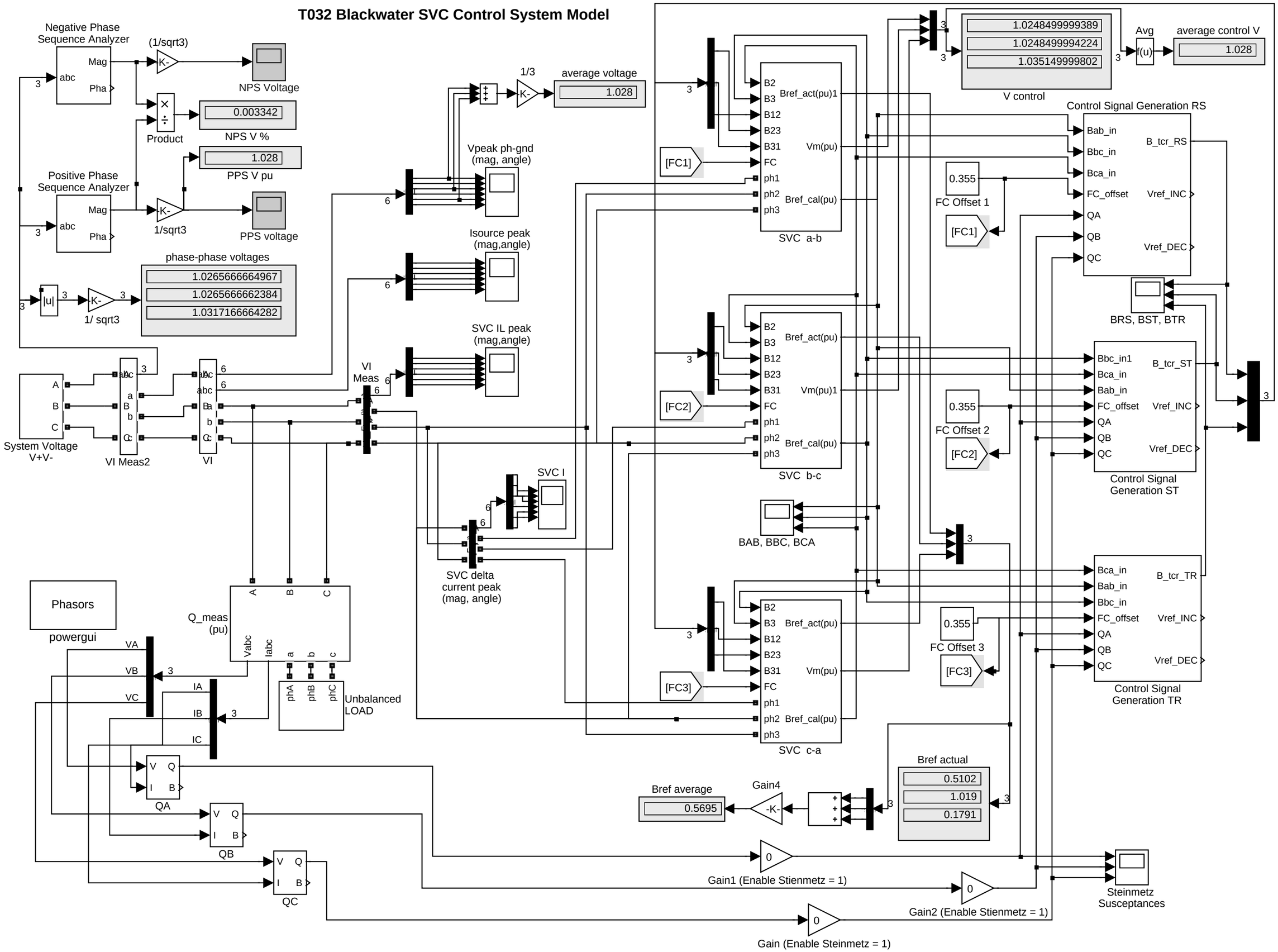


Figure I.1: Blackwater SVC Control System Model

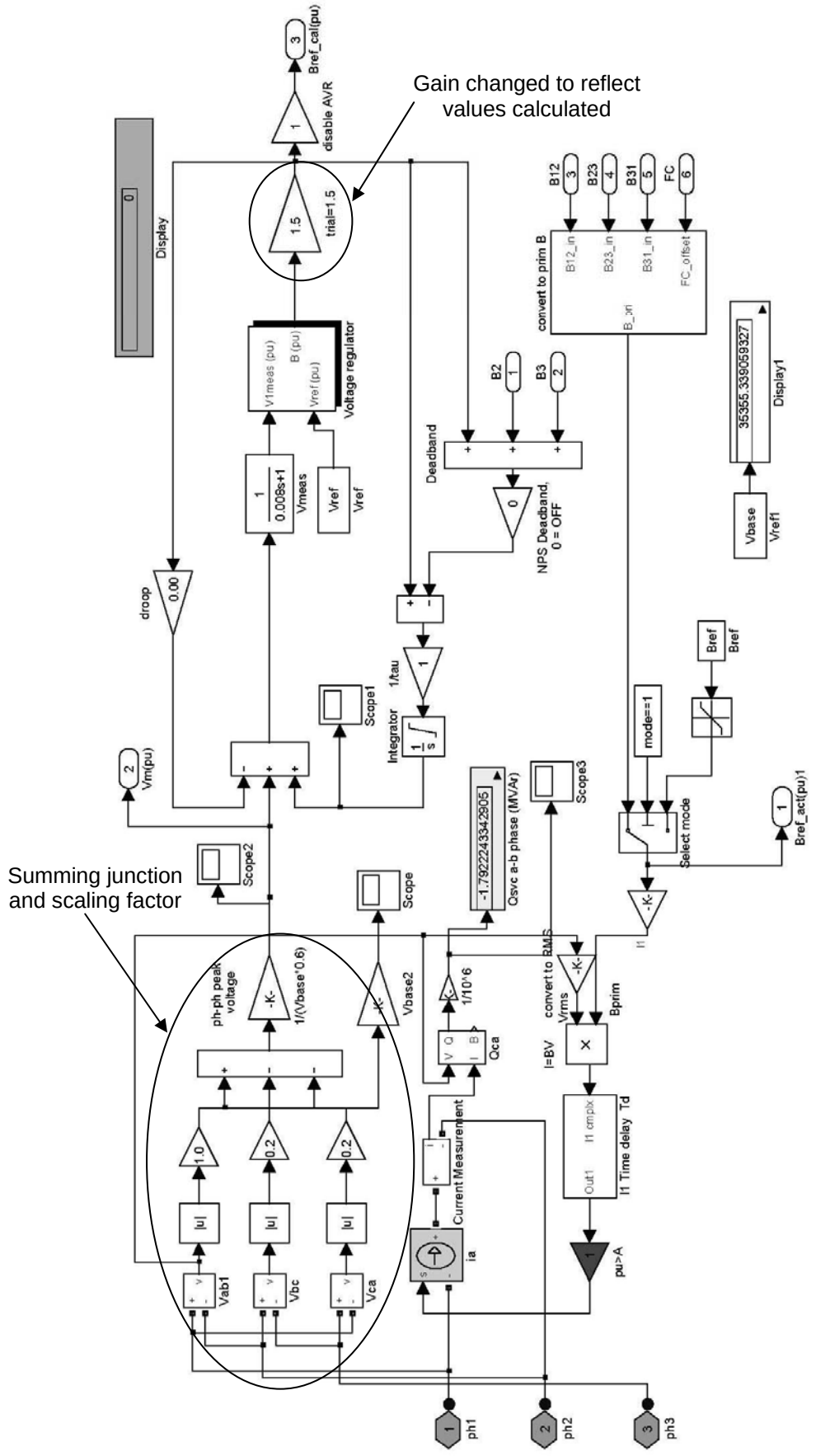


Figure I.2: Blackwater SVC control system model voltage regulation block.

Appendix J

Comparison of predicted and measured control system responses.

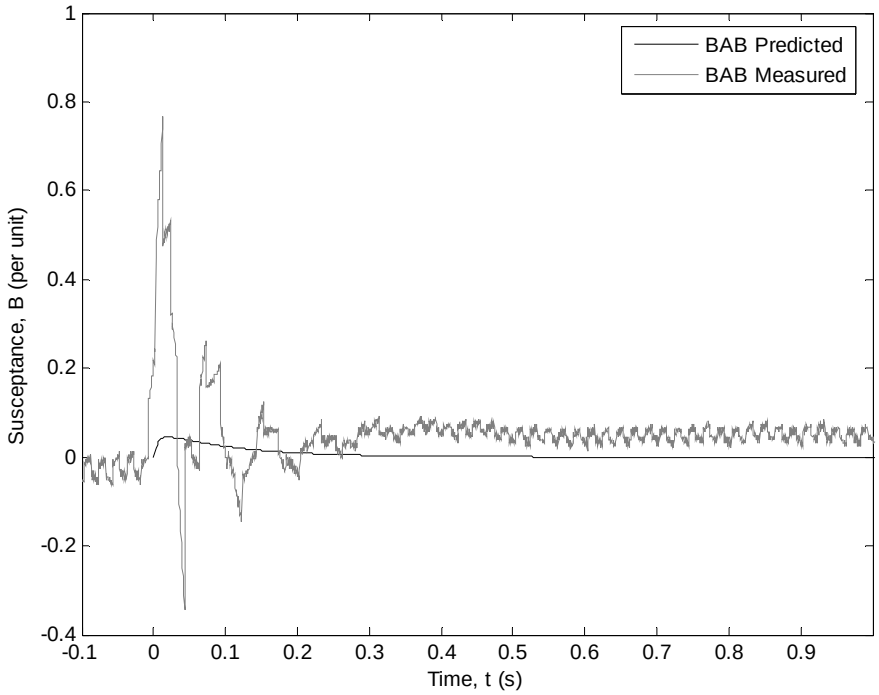


Figure J.1: Comparison of A-B phase voltage regulator predicted and measured response to A-B phase load imbalance.

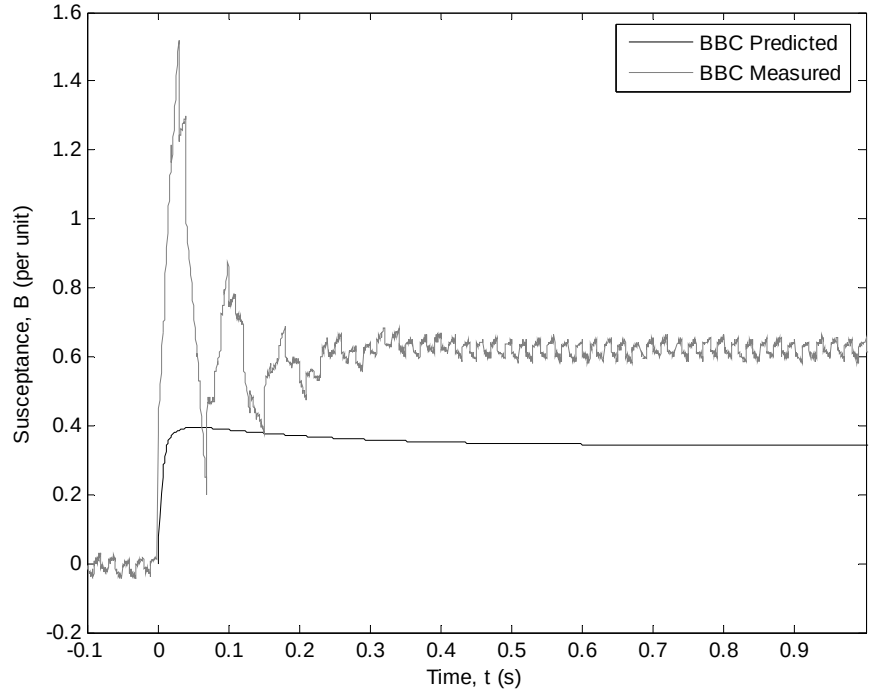


Figure J.2: Comparison of B-C phase voltage regulator predicted and measured response to A-B phase load imbalance.

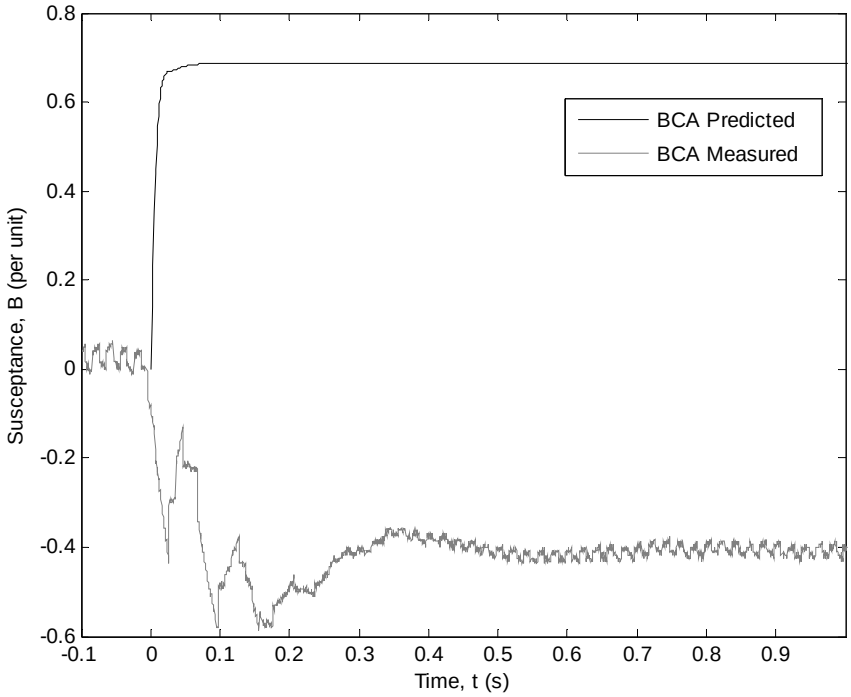


Figure J.3: Comparison of C-A phase voltage regulator predicted and measured response to A-B phase load imbalance.

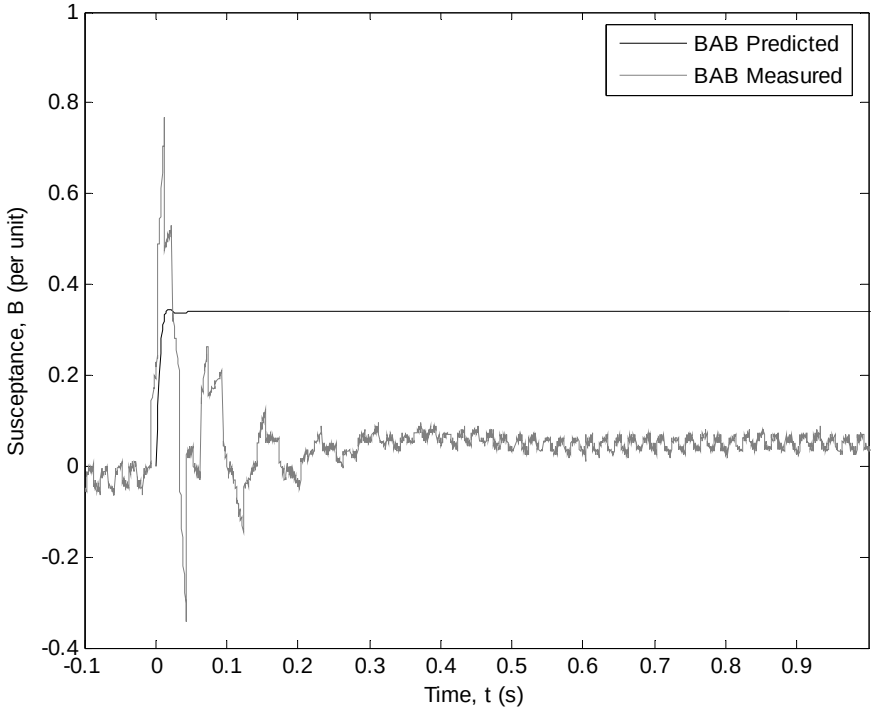


Figure J.4: Comparison of A-B phase voltage regulator predicted and measured response to B-C phase load imbalance.

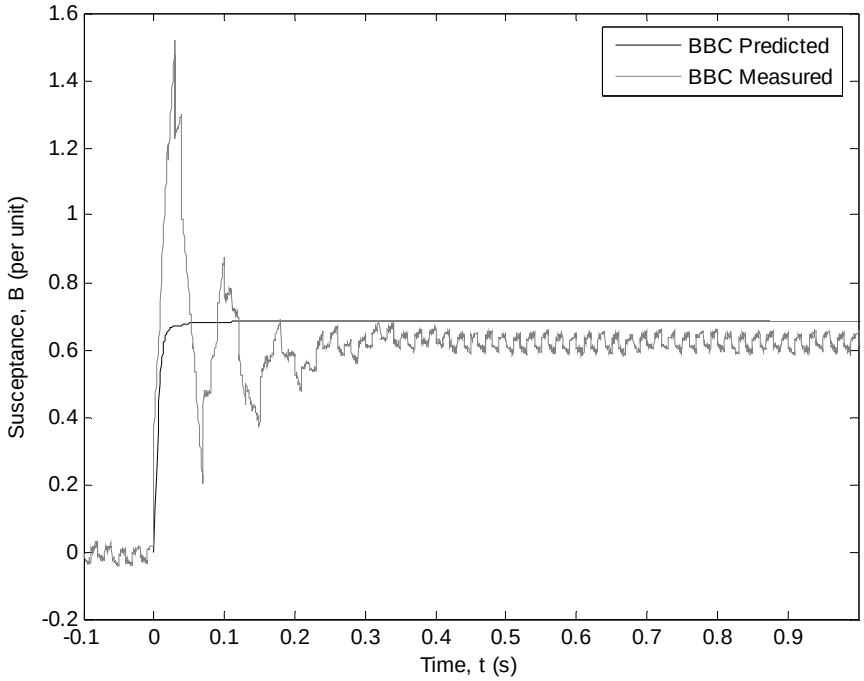


Figure J.5: Comparison of B-C phase voltage regulator predicted and measured response to B-C phase load imbalance.

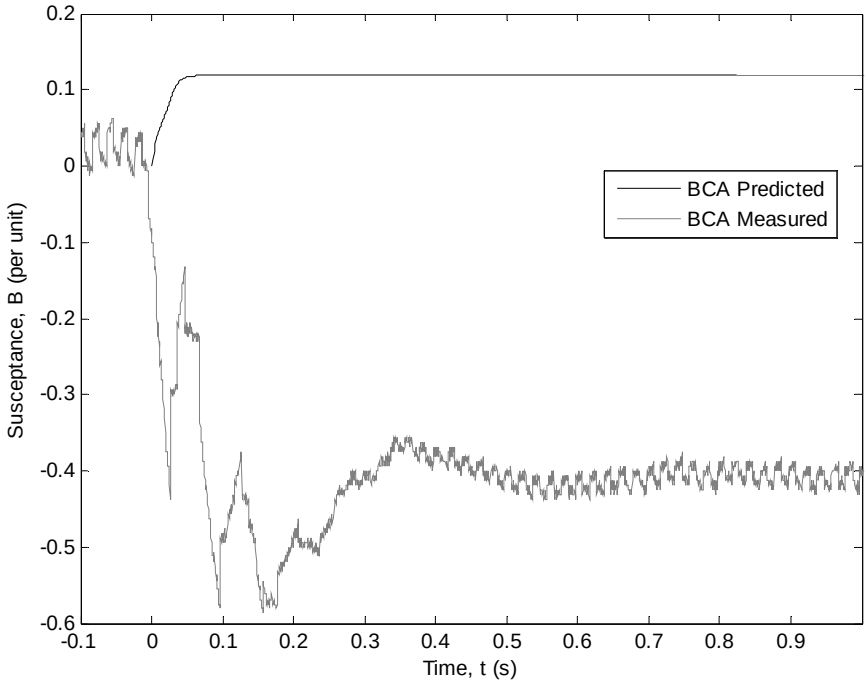


Figure J.6: Comparison of C-A phase voltage regulator predicted and measured response to B-C phase load imbalance.

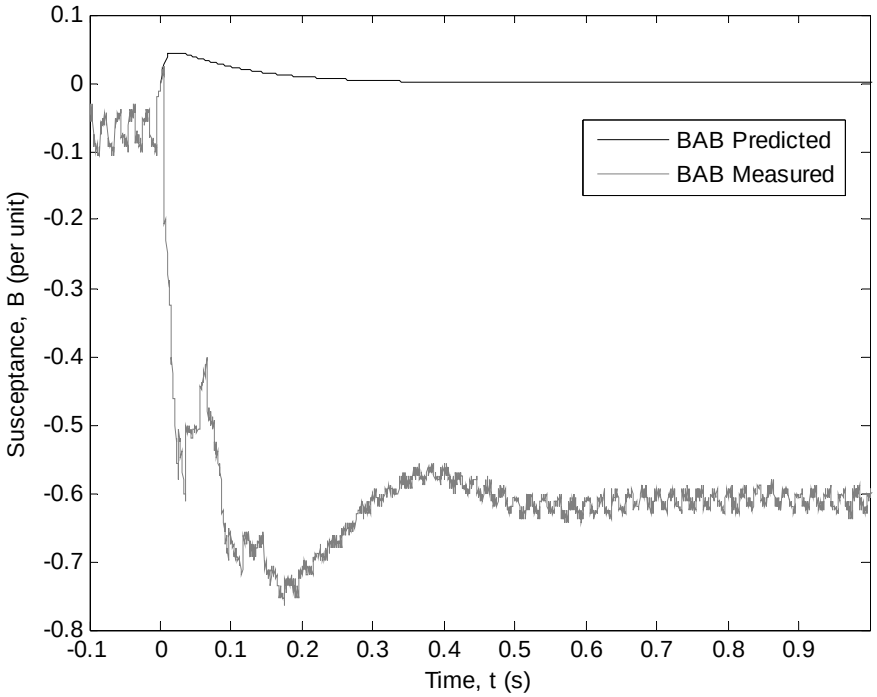


Figure J.7: Comparison of A-B phase voltage regulator predicted and measured response to C-A phase load imbalance.

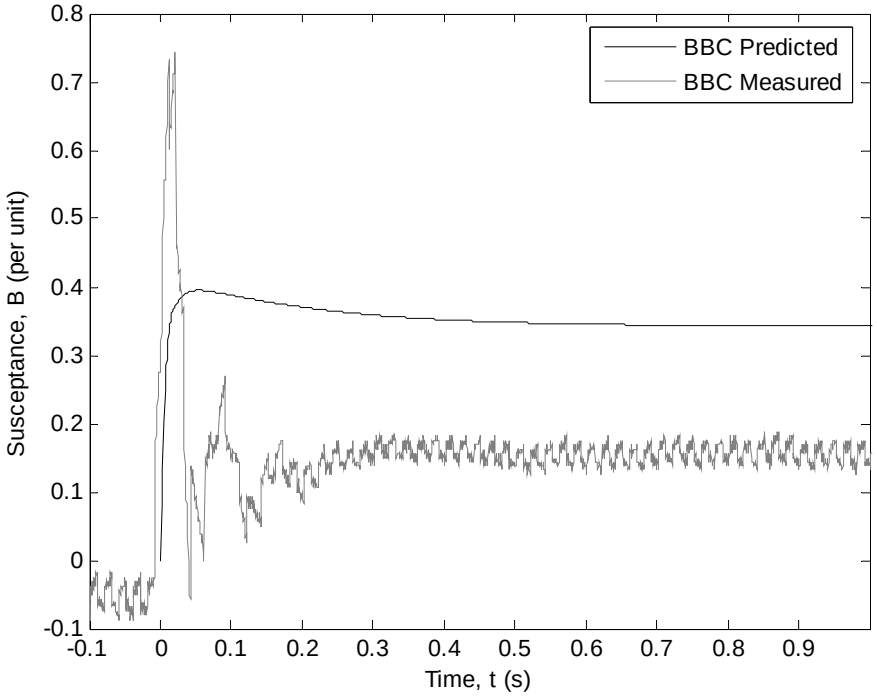


Figure J.8: Comparison of B-C phase voltage regulator predicted and measured response to C-A phase load imbalance.

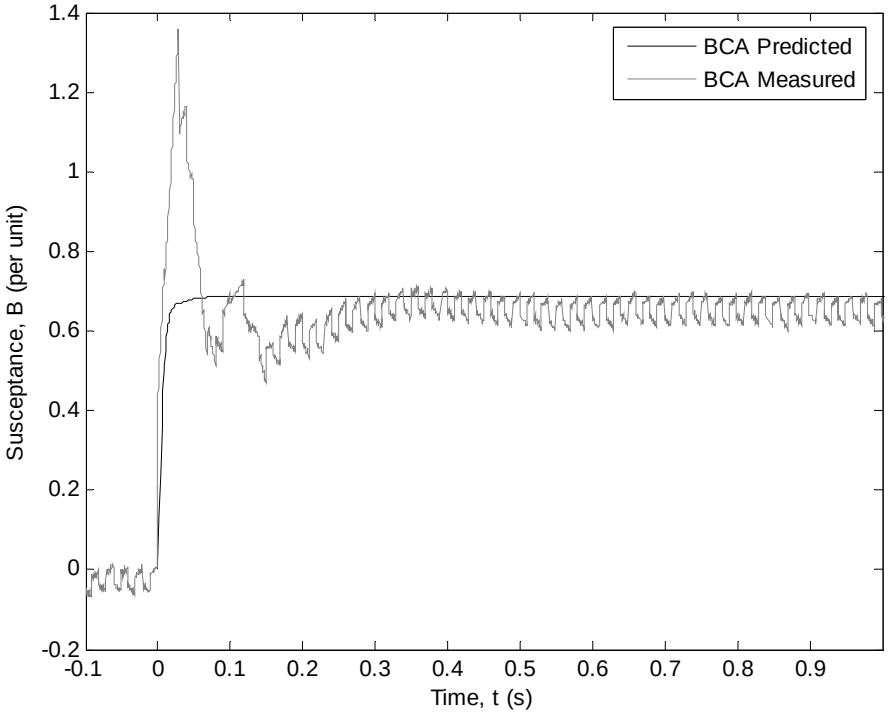


Figure J.9: Comparison of C-A phase voltage regulator predicted and measured response to C-A phase load imbalance.

Appendix K

Voltage Regulation Relevant Standards and Codes

The standards and codes identified as relevant to the research project are:

- National Electricity Code (NEC) and the Electricity Distribution (Supply Standards) Code specify allowable limits for voltage, frequency and power quality, and recovery times for excursions;
- The Customer Guide to Electricity Supply by Electricity Supply Association of Australia (ESAA) outlines supply quantity, reliability and quality and factors affecting these aspects;
- AS 60038 – 2000 *Standard Voltages*, that specifies AC transmission system nominal voltages and the allowable variations;
- AS 1359.31 – 1997 *Rotating electrical machines – General requirements Part 31: Three-phase induction motors – Operation on unbalanced voltages*. This Australian Standard details the effects of unbalanced supply voltages on the performance of three phase cage induction motors and the ensuing de-rating due to Negative Phase Sequence (NPS) voltage;
- AS 2279.2 – 1991 *Disturbance in mains supply networks Part 2: Limitation of harmonics caused by industrial equipment*, which discusses equipment producing harmonics and voltage fluctuations and assessment of impacts;
- AS 2279.4 – 1991 *Disturbance in mains supply networks Part 4: Limitation of voltage fluctuations caused by industrial equipment*, outlining acceptable limits of voltage fluctuations at the point of supply;
- IEEE Standard 1547, *IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems*, providing technical specifications for interconnection of power systems, most importantly power quality and specified response times to abnormal operating conditions, and
- IEEE Standard 1031-1991, *IEEE Guide for a Detailed Functional Specification and Application of Static VAR Compensators*, providing and overview of power system characteristics and main SVC characteristics.