A Thesis Submitted for the Degree of PhD at the University of Warwick

Permanent WRAP URL:

http://wrap.warwick.ac.uk/93459

Copyright and reuse:

This thesis is made available online and is protected by original copyright.

Please scroll down to view the document itself.

Please refer to the repository record for this item for information to help you to cite it.

Our policy information is available from the repository home page.

For more information, please contact the WRAP Team at: wrap@warwick.ac.uk
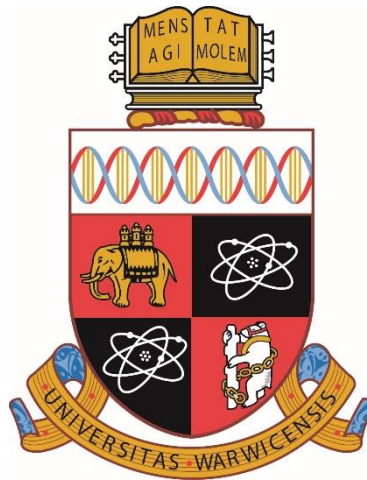
Germanium-Tin-Silicon Epitaxial Structures Grown on Silicon by Reduced Pressure Chemical Vapour Deposition

by

David Patchett
Thesis

Submitted to the University of Warwick

in partial fulfilment of the requirements

for admission to the degree of

Doctor of Philosophy

Department of Physics

THE UNIVERSITY OF
WARWICK

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. All experimental work presented was carried out by the author, or (where stated) by specialists under the author's direction.

Acknowledgments

I would like to thank my PhD supervisors Dr. Maksym Myronov and Prof. David Leadley for providing me with the opportunity to pursue my passion, provide guidance when it was needed, and the patience to let me learn from my mistakes. Special thanks to Dr. Maksym Myronov for producing the many samples investigated in this work.

Many thanks also to the members of the Nano-Silicon research group past and present including: Jamie Foronda, Phil Allred, Gerard Colston, Oliver Newall, Alan Burton, Ali Julian, Dr. John Halpin, Dr. Steven Rhead and Dr. Vishal Shah. Between you all, you have been friends, mentors and councillors at one time or another.

A huge thank you also to my partner, Ms Hannah Hickman, who has supported me in many ways throughout my studies. You have put up with my many ramblings wearing a smile. I honestly do not know how you managed.

Lastly, thank you to my family. My mother and father Susan and Paul Patchett, who encouraged me from a young age to be curious and showed me support as I pursued those curiosities. And thanks to my siblings Clare, John and Ruth for their continual support and for keeping me grounded.

Abstract

Crystalline germanium-tin (GeSn) binary alloys have been subject to a significant research effort in recent years. This research effort is motivated by the myriad of potential applications that GeSn alloys offer.

Crystalline epitaxial layers of GeSn and silicon-germanium-tin (SiGeSn) have been grown onto Si(001) substrates on a relaxed Ge buffer using reduced pressure CVD and commercially available precursors. X-ray diffraction, transmission electron microscopy, atomic force microscopy, secondary ion mass spectrometry and Raman spectroscopy were used to determine layer composition, layer thickness, crystallinity, degree of strain relaxation, surface features and roughness of the samples investigated in this work.

The epilayers produced have been both fully strained to their growth platform and partially relaxed. The Sn fraction of the alloy layers varied from 1 to 12 at. % Sn. Using N_2 as the carrier gas during growth is observed to inhibit $Ge_{1-x}Sn_x$ growth. Off-axis substrates are determined to hinder the production of crystalline layers of GeSn.

In-situ material characterization of GeSn layers during thermal treatment has identified the existence of a critical temperature for higher Sn fraction layers, beyond which the material quality degrades rapidly. This critical temperature is dependent on the layer composition, layer thickness, layer strain state and annealing environment. Layers of germanium-tin-oxide are produced by thermal oxidation and shown to have similar oxide formation rates to pure Ge.

The low thermal budget limit for the high Sn fraction alloys has driven research into forming Ohmic metal contacts on GeSn layers with processes limited to low temperatures. Gold is determined to be the optimum electrical contact material.

Publications and Presentations

Journal Publications

1. Rhead, S., Halpin, John E., Shah, V. A., Myronov, Maksym, **Patchett, D. H.**, Allred, Phil, Kachkanov, V., Dolbnya, I. P., Reparaz, J. S., Wilson, Neil R., Sotomayor Torres, C. M. and Leadley, D. R. (2014) *Tensile strain mapping in flat germanium membranes.* Applied Physics Letters, 104, 17

2. Fabio Pezzoli, Anna Giorgioni, **David Patchett**, and Maksym Myronov "Temperature-dependent photoluminescence characteristics of GeSn epitaxial layers", Submitted

3. David Patchett, Stephen Rhead, and Maksym Myronov "Thermal treatments of GeSn Epilayers with *in-situ* and *ex-situ* materials characterization", Thin Solid Films.

4. David Patchett, Stephen Rhead, and Maksym Myronov "Thermal oxidation of GeSn Epilayers with high levels of control"

5. David Patchett, Gerard Colston, Oliver Newall, and Maksym Myronov *"In-situ* characterization of GeSn epilayers at high temperatures using synchrotron radiation"

6. David Patchett, Thomas Walker, Maksym Myronov "Low temperature formation of electrical contacts to GeSn epitaxial layers"

Conference Presentations

1. **D. Patchett**, S.D. Rhead, M. Myronov, and D.R. Leadley "Challenges in Epitaxial Growth by RP-CVD of Strained and Relaxed GeSn Epilayers on a Si Substrate" *International SiGe Technology and Device Meeting (ISTDM 2013)*, Singapore, June, 2013.

2. **D.H. Patchett**, M. Myronov, S.D. Rhead, G. Colston, and D.R. Leadley "Challenges of growth and sample preparation of GeSn for electron

microscopy" *Microscopy of Semiconducting Materials* (MSM 2015), Cambridge, March, 2015

Table of Contents

1 Introduction

1.1 Semiconductors in the Wider World

Semiconductor technology is fundamental in the modern world, and its role is likely to only increase over time. A pivotal point for the widespread usage of semiconductors came with the invention of the first (widely recognised) transistor at Bell labs, which led to the awarding of the 1956 Nobel Prize in physics to William Shockley, John Bardeen and Walter Brattain "for their researches on semiconductors and their discovery of the transistor effect". However, it should be noted that previous work on transistors had been undertaken by Lilienfeld and later Heil. The first transistor at Bell Labs was made using crystalline germanium, and it's function was reliant on what was at the time the only recently developed quantum theory.

However, due to its high bulk cost, germanium was not to be the dominant material used in semiconductor devices. Silicon became the material of choice largely due to being more widely available, the excellent quality and non-water-soluble nature of the native oxide and significantly more economical semiconductor material for the expanding semiconductor industry.

Since its conception in 1965 and subsequent revision in 1975 "Moore's Law" has been both a predictor and driving force for advancement in the semiconductor microprocessor industry. Moore's law has several variations, but commonly interpreted as "the number of transistors on an integrated circuit will double approximately every two years", see Figure 1-1 which is adapted from a *Nature* news article [1]. This is possible due to the continuing reduction in the scale of individual transistors which allows the transistor density of computer chips to be increased,

which in turn increases the available processing power. However, Moore's law is not a physical law, and the scaling methodology is approaching its limits in pure silicon; as the dimensions of individual transistors approach the atomic scale, detrimental behaviour occurs such as transistor source-drain current leakage and device heating. Even if these issues are overcome, the single atom transistor is a hard limit for bulk materials, as using fractions of atoms for transistors is not a viable option.

To continue to improve the capabilities of available microprocessors and other semiconductor based technologies it is necessary to utilize the properties of more novel materials beyond pure silicon. In past decades this work has been investigated with great vigour, including III-V semiconducting alloys, epitaxial and bulk germanium and silicon-germanium (Si_yGe_{1-y}) alloys.
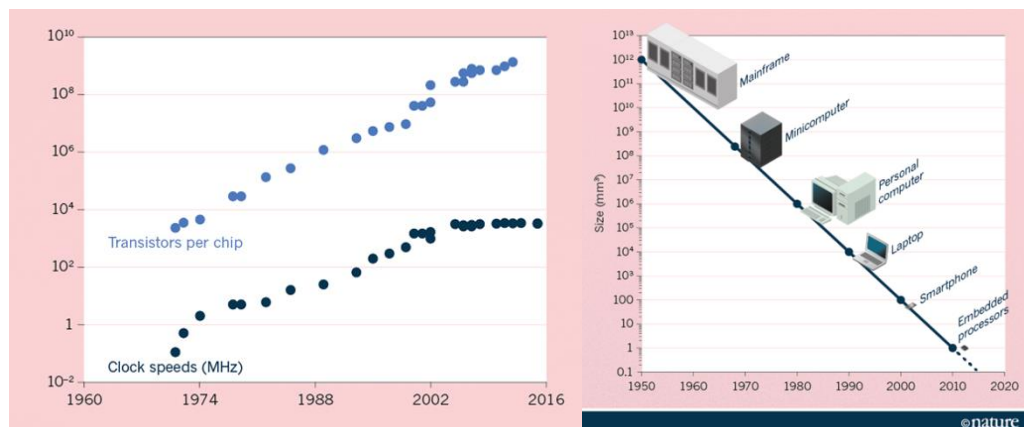
Figure 1-1 The historical trend of Moore's law, showing the number of transistors on a chip increasing in a logarithmic trend, agreeing with the doubling of transitors approximately every two years since the mid-sixties/early seventies.

1.2 Germanium-Tin and Silicon-Germanium-Tin

The germanium-tin ($Ge_{1-x}Sn_x$) binary alloy was first proposed by Soref as a potential material composed solely of group IV constituent elements which would possess a direct bandgap [2,3]. It is an alloy of the diamond cubic lattice α-phase Sn and Ge, which also has a diamond-like cubic lattice [4].

Increasing the Sn fraction produces $Ge_{1-x}Sn_x$ alloys with a larger lattice parameter and narrower bandgap than that of pure Ge, thus expanding the available parameter space of group IV alloys, such as lattice parameter, bandgap, thermal expansion coefficient, dielectric constant, charge carrier mobility, etc [5].

The significant obstacle to the development and implementation of $Ge_{1-x}Sn_x$ alloys is its metastability; under equilibrium conditions the maximum Sn fraction is ~1 at. % Sn in Ge-rich alloys, whereas incorporating any Ge into the Sn matrix to form a single phase Sn-rich alloys is also extremely challenging [6].

The binary $Ge_{1-x}Sn_x$ alloy has a single degree of freedom of composition, thus a particular alloy composition has a unique relaxed lattice parameter and a unique fundamental bandgap, and knowledge of one parameter can be used to infer the others. The ternary silicon-germanium-tin ($Si_yGe_{1-x-y}Sn_x$) alloy, however offers two degrees of freedom in composition space which allows lattice parameter and bandgap to be independently altered. For a single lattice parameter, the bandgap can be altered by ~0.2 eV, by tuning the composition [7].

The incorporation of silicon into the $Ge_{1-x}Sn_x$ matrix increases the alloy bandgap and increases the Γ-L conduction band separation, making the bandgap of such alloys further from a direct bandgap nature. The incorporation of silicon also increases the thermal stability of the alloy, which is desirable for many device applications [8].

1.2.1 Applications of (Silicon-)Germanium-Tin

The extension of parameter space of group IV semiconductors provided by binary $Ge_{1-x}Sn_x$ alloys and ternary $Si_yGe_{1-x-y}Sn_x$ alloys facilitates increasing the existing range of device applications for group IV semiconductors in addition to potential enhancements to existing applications.

By increasing the upper limit on lattice parameter from group IV materials, $Ge_{1-x}Sn_x$ epitaxial layers can use to improve upon existing structures. The larger lattice parameter of $Ge_{1-x}Sn_x$ means it can be grown lattice matched to a range of III-V alloy semiconductors, reducing the defect density in active layers of hybrid devices [9,10] and thus improving their performance. The high crystal quality, including low density of threading defects, high crystal order and sufficiently low surface roughness, makes $Ge_{1-x}Sn_x$ alloy epitaxial layers a suitable platform for subsequent growth of crystalline epitaxial layers [5,11–15]. Indeed studies have shown $Ge_{1-x}Sn_x$ layers are better able to absorb significant amounts of lattice stress than stiffer Si-rich alloys by forming lattice dislocations, this is supported by theoretical predictions which indicate $Ge_{1-x}Sn_x$ alloys have a particularly high plasticity compared to other group IV semiconducting alloys [9,16].

By using $Ge_{1-x}Sn_x$ layers as a platform for further epitaxial growth $Ge_{1-x}Sn_x$ can act as a stressor for thin Ge layers grown epitaxially on top of the alloy [17,18]. Inducing biaxial tensile strain in Ge has multiple benefits – the hole mobility increases, the bandgap shifts towards a more direct nature due to relative lowering of the Γ minima compared to the L minima, for these reasons tensile strain is used to improve the performance of Ge FETs [17,19].

The $Ge_{1-x}Sn_x$ alloys have either a direct bandgap or a smaller difference between their indirect and direct bandgap energy (L-Γ energy separation) compared to other group IV semiconducting materials, which makes epilayers favourable for applications such as photodetectors, avalanche photodiodes and emitters [20,21]. These structures can be grown on a silicon platform, enabling $Ge_{1-x}Sn_x$ growth processes developed to be more readily reproducible with current industry setups and keeping production costs low.

The narrowing of the bandgap and increased photonic efficiency of $Ge_{1-x}Sn_x$ layers compared to Ge and Si, particularly at longer wavelengths, makes the alloy a potential candidate for fabricating photodetectors and photoemittors well into IR region, extending the existing work done with inducing tensile strain in Ge layers for this purpose [22]. Of particular interest are $Ge_{1-x}Sn_x$ alloys with a bandgap suitable for photon emission and detection wavelength of approximately 1.5 μm, approximately 0.8 eV, which is in the centre of the range currently used in long distance telecommunications. This wavelength is used because 1.55 μm gives the best signal transmission in the IR range in optical fibres [23–25], although there is also potential applications for $Ge_{1-x}Sn_x$ based optical devices operating at even longer wavelengths [26].

Many of the proposed devices using the ternary $Si_yGe_{1-x-y}Sn_x$ alloy utilize the decoupling between lattice parameter and bandgap. By having such a large range of lattice parameters, $Si_yGe_{1-x-y}Sn_x$ layers can be grown lattice-matched to a large range of materials, theoretically spanning the full range from Si (5.43102 Å) to α-Sn (6.493 Å) if a wide range of compositions are attainable. $Si_yGe_{1-x-y}Sn_x$ has proposed applications as an active layer in multi-junction photovoltaics, with the layer covering a photon energy range which is not sufficiently covered by existing materials, also reducing abrupt lattice mismatch between Ge and III-V layers [27,28]. This would increase the possible collection efficiency of the device. The $Si_yGe_{1-x-y}Sn_x$ alloy also has applications in FETs as a stressor, with the composition being tuned to produce layers with a desired lattice parameter which can be larger or smaller than bulk Ge [29].

1.2.2 Strained Germanium-Tin

Very thin epitaxial $Ge_{1-x}Sn_x$ layers will be strained to their growth platform. Typical growth platforms are Si or Ge, and due to the smaller lattice parameter these substrates the $Ge_{1-x}Sn_x$ epilayer are typically compressively strained in-plane.

Lattice strain alters multiple material properties of all crystalline semiconductors, $Ge_{1-x}Sn_x$ included. Strain, either biaxial or uniaxial, also lifts the symmetry of the x, y and z axis found in bulk cubic materials, thus strain leads to the splitting of conduction and valence bands which can mean that charge carriers of the same type possess different properties, for example producing non-degenerate heavy hole and light hole bands [30,31].

In a compressively strained $Ge_{1-x}Sn_x$ alloy epilayer, the in-plane lattice parameter matches that of the smaller lattice growth platform, while the $Ge_{1-x}Sn_x$ out-of-plane lattice parameter expands as the unit cell volume acts to try to maintain the relaxed lattice cell volume following Poisson's rule.

For $Ge_{1-x}Sn_x$ epitaxial layers, compressive strain raises both the Γ and L conduction band minima – increasing the fundamental bandgap. The direct Γ band increases to a greater extent with compressive strain than the indirect L band, thus increasing the Γ-L conduction band separation and therefore producing a material further from a direct bandgap [32].

1.2.3 Relaxed Germanium-Tin

Lattice stain relaxation of $Ge_{1-x}Sn_x$ epilayers is important for achieving an indirect-to-direct bandgap transition and narrowing the fundamental bandgap, which is desirable for devices functioning in the IR region [33].

However, for heteroepitaxial structures this strain relaxation can only be achieved by the formation of strain-relieving lattice dislocations. In $Ge_{1-x}Sn_x$ heterostructures, these strain-relieving dislocations are typically Lomer edge dislocations, rather than threading dislocations which are typical in silicon-germanium heterostructures [7,9]. For many devices, the tendency to form edge dislocations is preferable to threading dislocations as the lattice defect does not propagate upwards through the layer material; which degrades the material and thus can degrade the electrical, mechanical, and optical properties. The tendency to form edge dislocations in $Ge_{1-x}Sn_x$ epitaxial layers therefore enhances the potential of this material to be used for devices and as a superior platform for subsequent growth.

Lattice strain relaxation initiates when the thickness of the layer being grown increases above the threshold critical thickness. This critical thickness depends on the degree of lattice mismatch between the layer and the substrate (i.e. alloy composition and growth platform), the growth temperature and thermal expansion mismatch between the epilayer and substrate (which alters the lattice mismatch upon cooling post-growth). Ultimately, as the initially strained layer thickness increases, strain energy accumulates in the epilayer until the threshold is reached whereupon the formation of misfit dislocations in the lattice release the strain energy with further increases in layer thickness increasing the degree of relaxation until the layer has adopted its bulk state.

1.3 Motivation

The growth of $Ge_{1-x}Sn_x$ alloy epitaxial layers by CVD, the growth method used in this work, is a novel process and successful growth has been reliably achieved in only a limited number of chemical vapour deposition (CVD) reactors. Upon the

initial demonstration of $Ge_{1-x}Sn_x$ CVD growth in 2002 [34], a single research group dominated research for the first decade, with a publication demonstrating CVD growth using an alternative growth method by a separate research group not being produced until 2011 [35]. The current range of CVD growth methodologies have significant differences, including precursor sources utilized, CVD chamber working pressure and CVD geometry, all of which affect the growth parameters necessary to reproduce growth results. Due to the limited scope of research, the details of growth conditions on produced alloy properties are yet to be fully explored.

Pseudomorphic, or fully strained, $Ge_{1-x}Sn_x$ layers are an important research area, covering epilayers without any lattice relaxation and therefore in this work are compressively strained in-plane to be lattice matched to the underlying strain relaxed Ge-buffer lattice. Compared to their lattice relaxed counterparts, fully strained $Ge_{1-x}Sn_x$ epilayers exhibit fewer lattice defects, as many defects are generated during lattice relaxation in the form of misfit dislocations.

The lower concentration of lattice defects in strained layer structures makes them favourable for many optical devices, as defects act as centres for non-radiative charge carrier recombination, inhibiting photonic device efficiency. Lattice strain modifies the bandstructure of the material, influencing charge carrier mobility [36]. Sufficiently strained layers may also exhibit significant band splitting, where the in- and out-of-plane lattice parameter differ producing two distinct conduction bands and two distinct valence bands, charge carriers within the split bands have different properties such as effective mass and mobility [37,38]. Strain induced bandstructure modifications can be utilized to enhance devices performance, for example increasing mobility in FETs [39].

Strain relaxed $Ge_{1-x}Sn_x$ layers are also an important area of research. In this work, $Ge_{1-x}Sn_x$ epilayer compressive strain relaxation increases the in-plane and reduces the out-of-plane lattice parameter, shifting towards a bulk cubic lattice. This is desirable for applications of $Ge_{1-x}Sn_x$ as a platform for subsequent lattice matched growth of III-V semiconductors, with lattice parameters larger than Ge, such as AlAs and InP. $Ge_{1-x}Sn_x$ layer relaxation from compressive strain also modifies the bandstructure, narrowing the bandgap and reducing the L-Γ separation [40], of great use in many applications such as IR photodevices and explored in detail previously.

Off-axis Si substrates are being researched as a potential method to integrate III-V semiconductor alloys onto group IV platforms and reduce the formation of anti-phase domains of the III-V epilayer [41,42]. As $Ge_{1-x}Sn_x$ epilayers are being investigated as potential platform for III-V materials, particularly low defect density layers for photonic devices.

Altering the carrier gas used during CVD growth was investigated with the aim of increasing the $Ge_{1-x}Sn_x$ growth rate. While many $Ge_{1-x}Sn_x$ growth investigations have used the H_2 carrier gas, growth of pure Ge at low temperatures has shown that switching to the N_2 carrier gas increases the growth rate. However, whether this will be seen in $Ge_{1-x}Sn_x$ growth is uncertain due to the different reaction chemistry [43].

The ternary $Si_yGe_{1-x-y}Sn_x$ alloy is also investigated, as discussed in section 7.2.5.3 the decoupled bandgap and lattice parameter makes it suitable for strain and bandstructure engineering in heretostructures.

1.4 Summary

Semiconducting alloys of group IV elements which incorporate tin have many fascinating properties, with the expansion of available parameter space offering the

exciting potential to enlarge and enhance the capabilities of existing semiconductor devices; however, our understanding and ability to produce these alloys is not yet well established.

Many challenges remain to be overcome in order to achieve reliable growth of semiconducting crystalline group IV alloys incorporating Sn. Prior to the widespread use of $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$ alloy epitaxy, it will be necessary to develop methods which supress alloy segregation during growth. These include growth at low temperatures with novel gas precursors that have still to be developed and fully-characterized. Methods to minimise the negative consequences of low growth rates at these reduced growth temperatures will also need to be developed. $Ge_{1-x}Sn_x$ alloys grown in this way will be metastable, which also limits post-growth thermal treatments and the subsequent growth of additional layers to low temperatures, to prevent loss of crystallinity of the $Ge_{1-x}Sn_x$ layer. The details of these thermal limits require further investigation.

Material characterization of the ternary $Si_yGe_{1-x-y}Sn_x$ alloys is more complicated than the established methods to characterize binary Si_yGe_{1-y} alloys and $Ge_{1-x}Sn_x$ alloys. The ternary alloy composition cannot be determined solely from x-ray diffraction, as is common for binary alloys. Thus alternative characterization methods are required to determine the composition, but parameter extraction can be more difficult in these less-standard methods, the equipment is less prevalent, and there are fewer established results with which newly acquired results could use for comparison.

This work details the investigation of the effect on material properties due to changes in several growth parameters. The material properties of strained and relaxed $Ge_{1-x}Sn_x$ epilayers will be explored. The response of $Ge_{1-x}Sn_x$ epilayers to thermal treatments is examined, to determine the existence and nature of any material

degradation, epilayer relaxation and oxidation and their relation to the Pre-thermal treatment materials properties. Finally, the formation of Ohmic contacts while minimising the damage to the $Ge_{1-x}Sn_x$ alloy epilayer will also be investigated.

2   Theoretical and Background Discussion

In this chapter the background knowledge regarding semiconducting crystalline germanium-tin alloys and silicon-germanium-tin-alloys relevant to this work is discussed including: the alloys' constituent elements (Si, Ge and Sn); the formation of crystalline epitaxial layers of alloys, with a focus on the binary $Ge_{1-x}Sn_x$ alloy; and the material properties of the elements and alloys and their inter-relation are explored, identifying the interdependence between alloy composition, lattice parameter, lattice relaxation, bandstructure and thermal stability.

As previously mentioned bulk silicon, germanium and alpha-tin all have a face-centred cubic lattice, commonly referred to as diamond cubic.

Regarding Si_yGe_{1-y} alloys, Si and Ge are completely miscible and any composition of this binary alloy can be produced at fairly high growth temperatures [44]. Despite the fairly large mismatch between the lattice parameter bulk Si and Ge lattice parameter of approximately 4.2%, any composition can be grown under equilibrium conditions and is thermally stable.

However, Ge and α-Sn are not fully miscible. At almost the opposite extreme a very limited compositional range of $Ge_{1-x}Sn_x$ alloys can be grown under equilibrium conditions and there exists a significant lattice mismatch of approximately 14% between the bulk lattices of Ge and α-Sn.

2.1 Basic Material Properties of Binary Germanium-Tin Alloys

Germanium-Tin (GeSn) alloys expand the potential range of properties achievable with group IV materials, expanding available parameter space with narrower bandgap, larger lattice parameter with a tuneable thermal expansion coefficient.

The expansion in material properties makes $Ge_{1-x}Sn_x$ alloy based devices superior to the current range of group IV alloys – $Ge_{1-x}Sn_x$ can be used to tensile strain Ge which improves carrier mobility and shifts the bandgap to a more direct nature. $Ge_{1-x}Sn_x$ layers have many potential applications in photonics devices – including applications in photovoltaics, photodectectors, and light emitting diodes [7,24,27,45,46]. The narrowing of the bandgap with increasing Sn fraction pushes $Ge_{1-x}Sn_x$ photon absorption region well into the 1.5 μm range, which is used in telecommunications, with the potential for operating at even longer wavelengths [47,48].

The majority of $Ge_{1-x}Sn_x$ epilayers grown by CVD using the $SnCl_4$ precursor utilize Ge-buffered Si substrates in order to minimise the lattice mismatch. Growth directly onto a Si substrate leads to massive lattice mismatch, this mismatch is reduced though not eliminated, by growing onto a relaxed Ge layer. However, Ge substrates are prohibitively expensive, therefore it is more economic to use a Ge buffer on Si substrates, which reduces the lattice mismatch with $Ge_{1-x}Sn_x$ with a low dislocation density at the growth surface, minimising the buffer/epilayer interface roughness and ensure epilayer quality is maintained.

2.1.1 Band Properties

Si and Ge are indirect bandgap semiconductors, the lowest energy part of the band are the L-minima, as such carrier excitation by photon absorption requires interacting

with a lattice phonon, which is an inefficient process and so requires thick layers for significant absorption. However, it has been recognised for some time that the energy separation between the Ge L-minima (indirect L band gap 664 meV [32]) and Ge Γ-minimum (direct gap of 800 meV) is very slight, with recent investigations indicating it is as narrow as 136 meV and therefore only relatively slight bandstructure modifications are necessary to close this gap [49]. A schematic diagram of the bandstructure of pure Ge in a relaxed and tensile strained state, which is indicative of the and the potential bandstructure of a Ge$_{1-x}$Sn$_x$ alloy, is shown in Figure 2-1, figure adapted from [32].

The novel aspect of Ge$_{1-x}$Sn$_x$ alloys is the effect of incorporating tin, specifically the cubic lattice phase called alpha-tin (grey tin). In isolation pure α-Sn has metallic
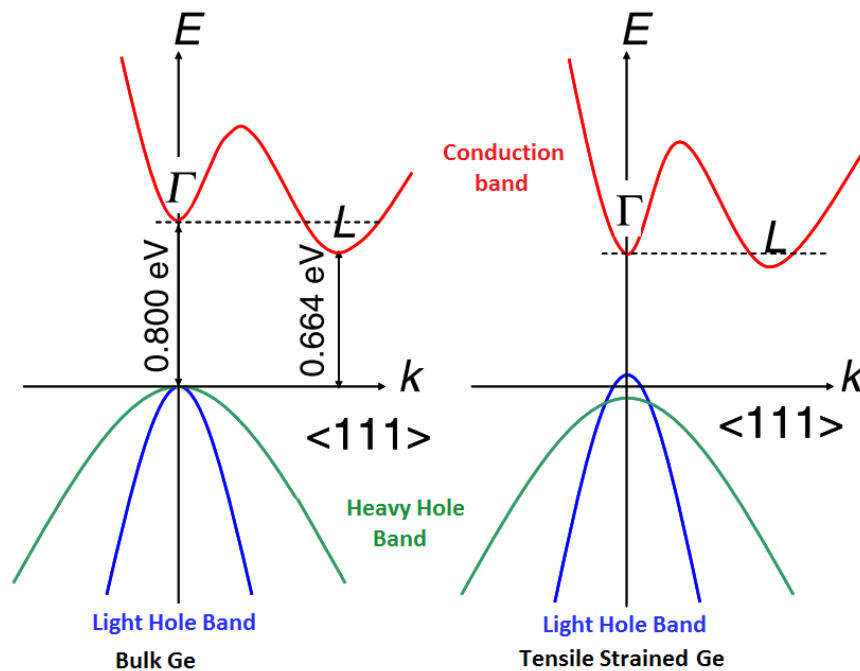
Figure 2-1 Schematic diagrams of the bandstructure of (left) pure relaxed Ge, with the indirect, L, gap being smaller than the direct, Γ, gap. (right) The bandstructure of tensile strained Ge, where the direct Γ gap has been reduced relative to relaxed Ge and the L-Γ separation has been reduced. A similar change in bandstructure is seen with the incorporation of Sn into Ge. For sufficient Sn incorporation the effect bandgap becomes direct in nature.

electrical properties. However, when regarding $Ge_{1-x}Sn_x$ alloys α-Sn is referred to as a semiconductor with a negative direct bandgap of -0.4 eV [50]. This is because it is the α-Sn direct Γ band which dictates the influence of Sn incorporation into Ge, and therefore the aspect of the bandstructure of α-Sn which must be considered when predicting the material properties in Ge-rich $Ge_{1-x}Sn_x$ alloys.

For some years it has been predicted that for a sufficiently high Sn fraction in the $Ge_{1-x}Sn_x$ alloy the Γ-minima will be at the same energy as the L-minima and thus the alloy will transition from an indirect-to-direct bandgap. The exact composition at which this transition is predicted to occur has changed with recent research. A simple linear interpolation would indicate a crossover at $x \approx 0.20$, with other compositions also predicted based on a range of theoretical models combined with experimental results from grown materials giving a large range of crossover compositions with $x = 0.06, 0.065, 0.08, 0.105$ [33,51–55].

However, $Ge_{1-x}Sn_x$ layers are typically grown on either Si or Ge and even thick layers retain some residual compressive lattice strain which in effect has the opposite impact on the alloy bandgap as greater Sn incorporation, increasing the magnitude of the Γ and L bandgaps and increasing their separation. Therefore to achieve a transition to direct bandgap material it is necessary to either grow an alloy which is compressively strained with a very high Sn fraction or induce compressive strain relaxation in a lower Sn fraction $Ge_{1-x}Sn_x$ layer. The effect of Sn fraction on the bandgaps of $Ge_{1-x}Sn_x$ alloys is non-linear for both strained and relaxed layers [15,51].

2.1.2 Crystal Lattice
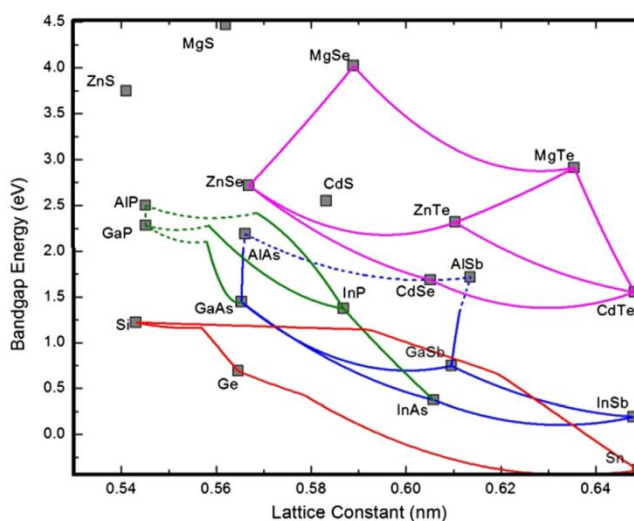
Figure 2-2 The range of lattice parameters and bandgaps of Si, Ge and alpha-Sn and for comparison those of many III-V semiconductor alloys. This highlights the board range of materials Si-Ge-Sn alloys can potentially be lattice matched to in order to produce low defect density heterostructures. This image is adapted from G. Sun, *et al.*, [143]

Of the materials studied in this work, Si has smallest lattice parameter at 5.43102 Å, the next smallest is Ge at 5.6579 Å, and α-Sn has by far the largest lattice parameter at 6.493 Å. Historically, it was challenging to determine the lattice parameter of α-Sn due to the difficulties with obtaining crystalline samples of sufficient size to obtain meaningful x-ray diffraction data. Additionally, after producing large enough sample for X-ray data the sample must be stored below room temperature in order to prevent the material transitioning to beta phase Sn.

The range of lattice parameters which can be attained with alloys of these three components is huge, with $Ge_{1-x}Sn_x$ alloys covering the greatest range. In combination these materials have the ability to lattice match with many III-V alloys, as illustrated in Figure 2-2, which would significantly aid the production of high quality hybrid structures with lattice matching to reduce defect densities. For the full scope of this

potential to be utilized, it is necessary to be able to produce a wide range of $Ge_{1-x}Sn_x$ alloy compositions.

As previously detailed, creating high Sn fraction $Ge_{1-x}Sn_x$ alloys is challenging due to the low, ≤ 1 at. %, equilibrium solid solubility of Sn in crystalline Ge. The propensity for alloy segregation is in large part due to the aforementioned huge lattice mismatch between α-Sn and Ge, in addition to the large difference in atomic radius of Sn from 15-16% [56,57].

In unstrained, i.e. bulk, cubic crystal lattice structures the lattice parameters in all 3 crystal directions are equal, i.e. $a_0 = b_0 = c_0$, additionally the base crystal lattice vectors equal and orthogonal, hence $\alpha = \beta = \gamma = 90°$. This significantly simplifies conceptualising crystal lattice modifications.

For many binary alloys the lattice parameter of the alloy of a specific composition can to the first approximation be regarded as a linear relation between the bulk lattice parameter for the two component elements, weighted by the proportional composition of the alloy. This is a 'pure' or 'unmodified' Vegard's law, as given in equation 2-1.

$$a_{ij} = x \cdot a_i + (1 - x) \cdot a_j \qquad (2\text{-}1)$$

Where 'a_{ij}' is the lattice parameter of the alloy, 'a_i' and 'a_j' are bulk lattice parameters of elements 'i' and 'j' respectively and 'x' is the fraction of element 'i' in the alloy. Real crystals are not represented by a perfectly linear relation. There is typically a non-linear component to the relation between lattice parameter and alloy composition, the general form of this is given in equation 2-2.

$$a_{ij} = x \cdot a_i + (1 - x) \cdot a_j + b_{ij} \cdot x \cdot (1 - x) \tag{2-2}$$

Where 'b_{ij}' is degree of the non-linear behaviour of the lattice parameter, the alloy bowing parameter. In crystal physics this relation referred to as Vegard's law. For Si_yGe_{1-y} alloys and other semiconductor alloys the bowing parameter is negative, b_{SiGe} = -0.02733 [58]. However for $Ge_{1-x}Sn_x$ alloys the bowing parameter is positive, b_{GeSn} = 0.041 Å, [59], with the full Vegard's law for $Ge_{1-x}Sn_x$ given in equation 2-3.

$$a_{GeSn} = x \cdot a_{\alpha-Sn} + (1 - x) \cdot a_{Ge} + 0.041 \cdot x \cdot (1 - x) \tag{2-3}$$

The bowing parameter of $Ge_{1-x}Sn_x$ required experimental determination. For this X-ray diffraction (XRD) data is used to determine the lattice parameter of a sample, and combined with an independent measurement of the composition of the same sample and the results compared. This process is repeated for many samples with a range of alloy compositions to determine the bowing parameter. Secondary ion mass spectroscopy (SIMS), Rutherford back scattering (RBS) and Energy dispersive X-ray spectroscopy (EDS) measurements provide composition information, but each characterization method has its own source of measurement error. These methods must therefore be used with some caution, so it is common to use multiple methods to determine the composition, such that the results from each method can be compared very reliable verification.

Different publications report a range of $Ge_{1-x}Sn_x$ alloy bowing parameters, with initial values ranging from 0.00882 Å to 0.65 Å, but after a series of systematic studies it is generally being accepted as b_{GeSn} = 0.041 Å [12,55,59–61]. The majority of research is in agreement that the sign of the $Ge_{1-x}Sn_x$ bowing parameter is positive, which is opposite of that found in the Si_yGe_{1-y} and $Si_{1-z}C_z$ systems, indeed all other group IV semiconductor alloy systems have small negative bowing parameters

[58,62]. This difference is attributed to the comparatively huge difference in Ge and

α-Sn atomic radii and lattice parameters.
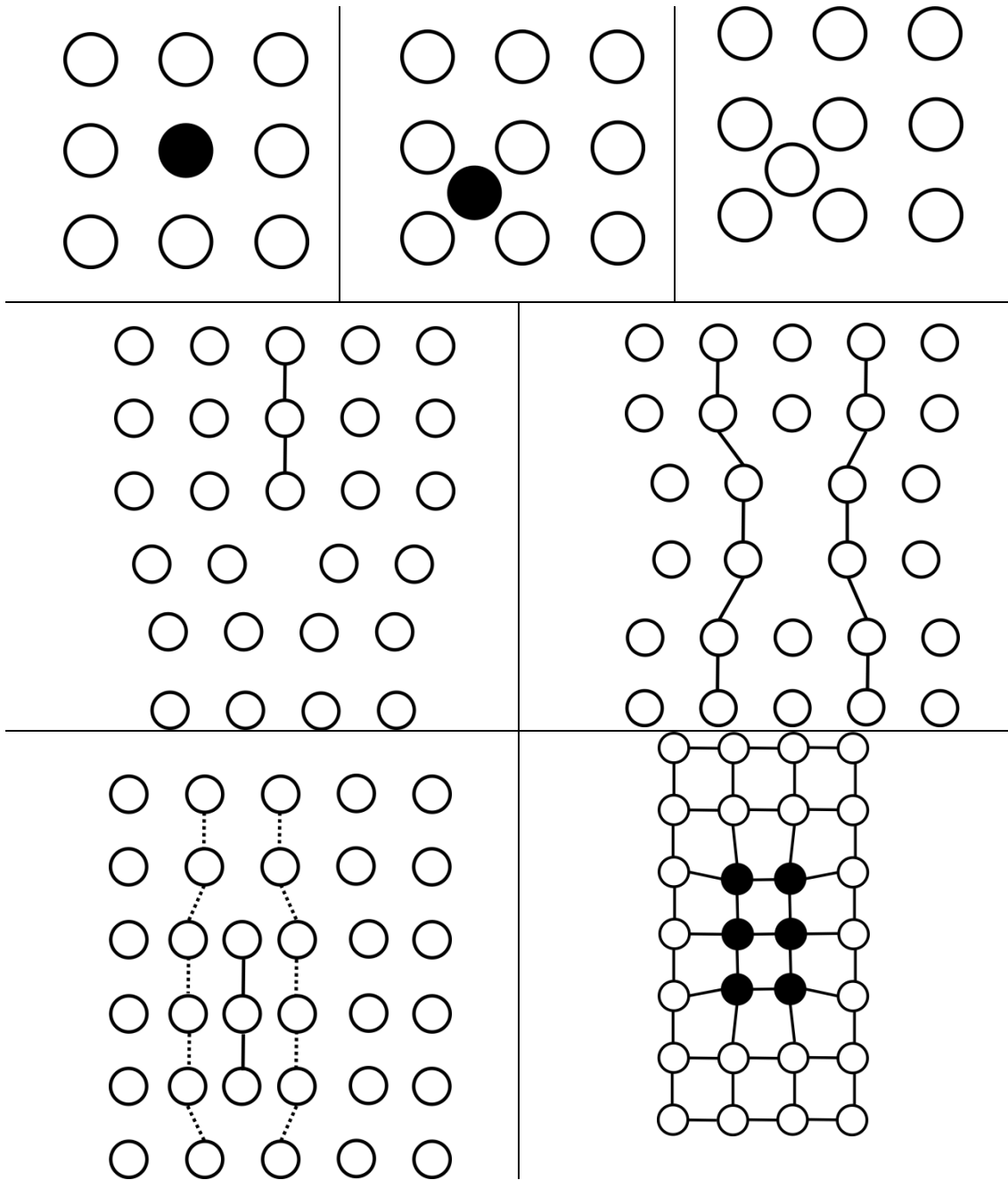
Figure 2-3 Schematic diagrams of several crystal defects in 2D with a square lattice. Unfilled circles represent bulk crystal atoms, filled circles represent impurity atoms. Lines denoting bonds are shown to illustrate interruptions in crystalline order. Defect types shown: (Top left) A substitutional impurity atom. (Top centre) An interstitial impurity atom. (Top right) An interstitial bulk atom – where the atom comprises a significant proportion of the bulk. (Middle left) An edge dislocation, with a partial plane of atoms inserted into the crystal from the edge of the crystal. (Middle right) A vacancy dislocation. (Lower left) Interstitial dislocation. (Lower right) Impurity precipitation

Fully-strained $Ge_{1-x}Sn_x$ layers have been reported that are thicker than would be thought possible without undergoing some strain relaxation [59]. The out-of-equilibrium, i.e. low temperature, nature of $Ge_{1-x}Sn_x$ growth is believed to supresses the formation of misfit dislocations, and consequently the experimental critical thickness for relaxation is larger than expected for group IV semiconductor alloys grown at higher temperatures [58,59]. This suppression of the formation of strain-relieving misfit dislocations may contribute to the challenge of reaching high degrees of lattice strain relaxation by growing very thick $Ge_{1-x}Sn_x$ layers.
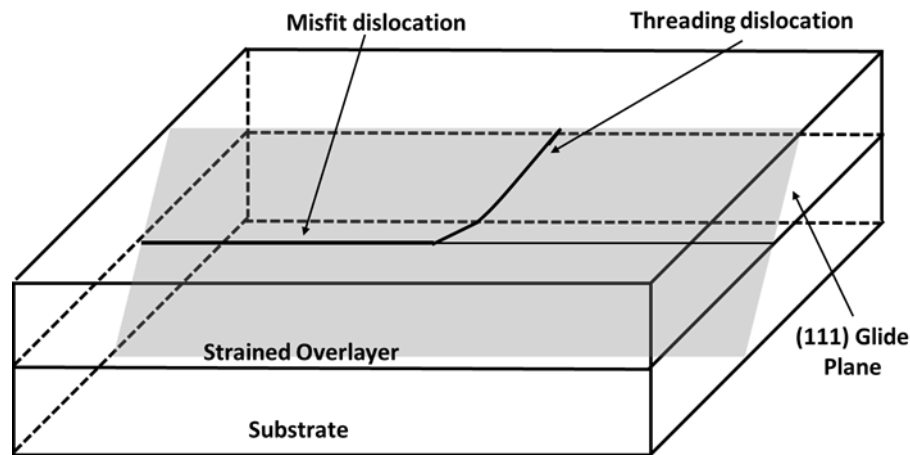
Figure 2-4 Schematic of the formation of a threading dislocation from a misfit dislocation generated at the interface between two mismatched layers of a heterostructure.

The misfit dislocations that are predominantly observed appear to be Lomar edge dislocations, which are confined to the $Ge_{1-x}Sn_x$/Ge interface and do not propagate upwards through the $Ge_{1-x}Sn_x$ epilayer [5,7].

The deformation of the crystal lattice in response to lattice strain is determined in part by the material's elastic constants. The values of which are given for Si, Ge and α-Sn in Table 1, note the α-Sn Poisson ratio is comparable to that of Ge.

Figure 2-3contains schematic diagrams of a range of crystal defects. Point defects include impurity atoms in substitutional and interstitial sites, and atoms of the

element(s) which compose the bulk crystal which are in interstitial lattice sites. Line defects, or dislocations, are generated when a partial plane of atoms is present in or absent from the crystal, disrupting the local symmetry and causing localised strain. A volume defect of particular interest to this work is a precipitate of impurity atoms with a crystal structure different to the bulk crystal, which is also shown schematically.

Misfit dislocations form between lattice mismatched layers when the lattice strain energy exceeds a threshold and crystal defects are formed in order to relieve this strain energy. Misfit dislocations can lead to the formation of a threading dislocation, a line defect which propagates in both the in plane and out of plane directions as shown schematically in Figure 2-4. An additional mechanism for misfit dislocations is to form a Lomar edge dislocation, a line defect which is constrained to the interface between the mismatched crystal layer as it has no out of plane component, a detailed exploration can be found in ref [63].

2.1.3 Thermal Stability

The diamond-like cubic alpha-Sn phase is only stable up to a temperature of 13 °C; at higher temperatures the tin crystal structure will change phase to β-Sn, which has a non-cubic lattice and a metallic nature. However, the epitaxially grown α-Sn onto low lattice mismatched substrates increased the temperature limit to ~70 °C [64]. The melting temperature of Sn is relatively low, 505 K, compared to those of Ge and Si shown in Table 1. The Sn bulk melting temperature is close to the typical $Ge_{1-x}Sn_x$ CVD growth temperature which is typically 520 K and above. This may be expected to have implications for the interdiffusion of Sn atoms between the $Ge_{1-x}Sn_x$ epilayer and the Ge buffer, with the Sn atoms being mobile relative to the Ge atoms and

readily diffusing across the $Ge_{1-x}Sn_x$/Ge interface, leading to a less abrupt interface. However, this is not reported in the literature, where even high Sn fraction $Ge_{1-x}Sn_x$ layers grown on a Ge buffer have been demonstrated which do not exhibit interdiffusion when annealed at 300 °C [65].

The maximum equilibrium solid solubility Sn fraction is ~1 at. %, the alloy phase diagram is shown in Figure 2-5, with two distinct phases being thermodynamically favourable at higher Sn fractions. Thus, growth of single phase alloys with a higher Sn fraction requires out-of-equilibrium conditions; with the need for conditions to be increasing far from equilibrium as the target Sn fraction increases.

Due to the equilibrium state being phase separation, once grown single crystalline epitaxial layers of $Ge_{1-x}Sn_x$ alloys are metastable; any post-growth treatments at sufficiently high temperatures will induce alloy segregation into Sn-rich and Ge-rich regions and is no longer monocrystalline. The thermal stability of alloy layers is dependent on multiple factors, including the Sn fraction [66,67].

Thermal treatments are used for annealing epilayers to improve crystal quality [30]. As grown material will typically have atoms not just in substitutional sites, but there will also be atoms in interstitial sites and the crystal will have vacancies where a lattice atom should be located. Treatment of the sample at high temperatures provides the thermal energy necessary for atoms to move, allowing interstitial defects and vacancies to move and annihilate, thus improving the crystal quality. The increased thermal energy can also allow small crystal imperfections to re-orientate to the match the rest of the crystal. Thermal cycling has been used to reduce the density of threading dislocations in Ge epilayers [68]. These processes improve the crystal quality, but excessive thermal treatments can cause alloy segregation [69].

In addition to improving material quality, thermal treatments are also necessary for Ohmic contact formation; the increased thermal energy facilitates atoms from the metal contact to diffuse into the $Ge_{1-x}Sn_x$ epilayer, forming a high quality contact. Again this must be done without significantly degrading the crystal quality of the whole layer [70].

The coefficient of thermal expansion is an important material parameter as it contributes to lattice strain after growth, for example it causes the over relaxation of Ge buffers grown on Si substrates. This effect of different expansion coefficient of heteroepitaxial layers has been used to induce strain in Si-Ge epilayers with multiple thermal cycles [32]. The α-Sn linear thermal expansion coefficient, given in Table 1, is intermediate between Ge and Si, but how the coefficient changes with alloy composition has yet to be investigated.

Metastable high Sn fraction crystalline $Ge_{1-x}Sn_x$ alloys heated to high temperatures
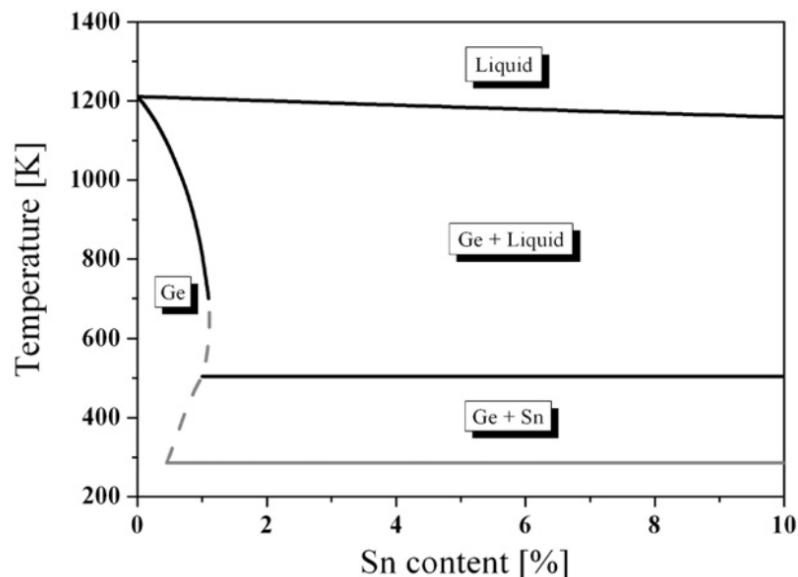
Figure 2-5 The phase diagram of Ge-rich $Ge_{1-x}Sn_x$ alloys. Note the maximum Sn fraction that can be incorporated into the Ge matrix is ~1 at. %. At the opposite range, essentially no Ge fraction can be incorporated into the Sn matrix. Image obtained from Kasper *et al.* [6].

exhibit Sn segregation, with Sn features appearing on the sample surface. As the Sn fraction of the alloy increases the temperature at which this segregation takes place decreases, as the original alloy is further from equilibrium [19]. It has been suggested that there exists a critical temperature, where a $Ge_{1-x}Sn_x$ alloy layer is relatively stable below this temperature but the crystallinity severely degraded with Sn segregation above this temperature [69]. Understanding the nature of the $Ge_{1-x}Sn_x$ response to thermal treatments, whether the critical temperature does exist and if so what material parameters influence it, is vital for optimal material processing without causing critical damage to the crystal quality. However, a sufficient level of understanding has yet to be reached. Currently, the critical temperature has only been suggested, but not confirmed, and additionally there are conflicting published results of whether strain relaxation can be achieved with thermal treatments before the onset of material degradation [67].

The melting temperatures of Si, Ge and α-Sn are given in Table 1. All temperatures used for $Ge_{1-x}Sn_x$ alloy growth and thermal treatments are significantly below the melting points of Si and Ge, thus it can be safely assumed that the Ge buffer and Si substrate layers will be stable. The melting temperature for Sn is above the temperature at which Sn undergoes a phase change to β-Sn. As mentioned previously, the Sn melting temperature is close to that of typical growth temperatures and below the thermal treatment temperatures used in this work. It is anticipated therefore that the response of $Ge_{1-x}Sn_x$ alloys to high temperatures will vary from the response of silicon-germanium materials.

	Silicon (Si)	Germanium (Ge)	Alpha-Tin (α-Sn)
Lattice parameter (Å) [5]	5.431	5.658	6.493
Elastic constants (GPa) [5]			
C_{11}	165.8	128.8	66
C_{12}	63.9	48.3	34
C_{44}	79.6	66.8	29
Poisson Ratio ((100) Orientation)[59]	0.28	0.26	0.263
Melting point (K)[71]	1687	1211	505
Linear thermal expansion coefficient (K^{-1}) [71]	2.92×10^{-6} (293 K)	5.90×10^{-6} (293 K)	4.7×10^{-6} (293 K)
Atomic Covalent Radius (pm) [71]	117	122	140
Energy band gap (eV) [71]	1.1242 (at 300 K)	0.664 (at 291 K)	-0.4

Table 1- Several of the material properties of bulk Si, Ge and α-Sn

2.1.4 Summary of GeSn

Crystalline $Ge_{1-x}Sn_x$ epitaxial layers expand the existing parameter space of group IV materials; with larger lattice parameters and narrower bandgaps becoming attainable. Additionally there is the potential for an indirect-to-direct bandgap transition in $Ge_{1-x}Sn_x$ for higher efficiency photonic devices than found in existing group IV materials.

Several of the significant initial challenges of epitaxial growth incorporating Sn into other group IV materials have begun to be overcome by the research to date. $Ge_{1-x}Sn_x$

alloys have routinely been grown with Sn fractions far exceeding the low equilibrium Sn solid solubility in Ge. Recently, direct bandgap $Ge_{1-x}Sn_x$ has been demonstrated experimentally with a high Sn fraction epilayer, with significant but not complete degree of strain relaxation by the growth of a very thick $Ge_{1-x}Sn_x$ epilayer [72].

2.2 Ternary Silicon-Germanium-Tin Alloys

Similar to the binary germanium-tin alloy, the ternary silicon-germanium-tin $(Si_yGe_{1-x-y}Sn_x)$ alloy is composed solely of group IV elements. Attempts have even been made towards producing the quaternary SiGeSnC alloy, but making progress is challenging [73]. An appropriate comparison of a ternary group IV alloy is with quaternary alloys in III-V semiconductor systems. Bulk binary III-V semiconductors, such as GaAs, have fixed bandgaps and composition, similar to elemental group IV semiconductors, such as Si and Ge. As the proportion of two elements of a ternary III-V semiconductor alloy can be altered in a coupled way, either the two group III or group V constituent elements must sum to constitute half of the total atoms in alloy, such as varying the indium and gallium content in $In_xGa_{1-x}As$ [74]. Altering the composition of a ternary III-V alloy alters the bandgap and lattice parameter in a coupled way, providing a single degree of freedom, analogous to binary group IV alloys, such as Si_yGe_{1-y}. Finally quaternary III-V alloys, for example $In_xGa_{1-x}As_{1-y}P_y$, have two degrees of freedom; allowing lattice parameter and bandgap to be independently altered [75]; though still confined by the properties of the constituent elements. Ternary alloy group IV semiconductors, such as $Si_yGe_{1-x-y}Sn_x$, have two degrees of freedom in composition, and lattice parameter and bandgap can be altered in an uncoupled way, though again to a limited degree, which is comparable to quaternary III-V semiconductors [29,76,77]. The two degrees of freedom of the alloy

composition decouples lattice parameter and bandgap, such that alloys with the same lattice parameter can have different bandgaps.

The use of a ternary $Si_yGe_{1-x-y}Sn_x$ alloys makes available a wider range of lattice parameters, bandgaps, and degree of directness of the effective bandgap [78]. These properties make this alloy very promising for lattice matching to layers of many other materials. The material parameters can be varied by changing composition and lattice strain. $Si_yGe_{1-x-y}Sn_x$ is also more thermally stable that binary $Ge_{1-x}Sn_x$, with the incorporation of Si atoms acting to stabilize the alloy, which may facilitate more device processing methods [8].

It should be noted that the properties and growth of $Si_yGe_{1-x-y}Sn_x$ are regarded as the incorporation of Si into $Ge_{1-x}Sn_x$ and not the incorporation of Sn into Si_yGe_{1-y}. Consequently, the growth of $Si_yGe_{1-x-y}Sn_x$ requires the low growth temperatures used in $Ge_{1-x}Sn_x$ alloy growth.

2.2.1 Band Properties

The incorporation of Si into $Ge_{1-x}Sn_x$ makes the formation of a direct bandgap increasingly difficult, as increasing the Si content increases both the L and Γ bandgaps, with the Γ bandgap increasing more rapidly with Si fraction than the L gap; reducing the degree of directness of the bandgap [78]. At the extreme case of a binary $Si_{1-x}Sn_x$ alloy, theoretical predictions suggest that a direct bandgap is not possible [79].

2.2.2 Lattice Parameter

The decoupling of the $Si_yGe_{1-x-y}Sn_x$ lattice parameter and bandgap means that for a given lattice parameter the bandgap can be altered by ~0.2 eV by tuning the

composition [7]. The lattice parameter range covers that of several III-V alloys alloying for high quality integration, as shown in Figure 2-2.

The decoupling of alloy composition and lattice parameter means that it is not possible to determine a unique composition using many common characterization methods, such as XRD. Determining composition therefore requires using the more complex methods such as RBS, which is less prevalent than XRD, or composition from SIMS which is both less prevalent than XRD and which requires high surface quality and the precision of SIMS measurements diminishing with increased probing depth.

The incorporation of Si into the $Ge_{1-x}Sn_x$ matrix reduces the lattice parameter of the alloy. It is therefore possible to produce a SiGeSn alloy lattice matched to pure Ge, with an Si-to-Sn ratio of ~4 : 1. The ability to lattice-match to pure Ge means that strain relaxed $Si_{4x}Ge_{1-5x}Sn_x$ can be grown onto pure Ge without the formation of strain reliving lattice dislocations [76,77,80].

2.2.3 Thermal Stability

Increasing the Si alloy fraction at a constant Sn fraction increases the thermal stability [8,77]. The increase in stability is attributed to the Si atoms partially counteracting the mismatch effects of the Sn when incorporated into a Ge-rich matrix. The increased thermal stability is important for applications where it is desirable for the layer to have a high thermal budget; for example if subsequently grown epitaxial layers would require a high growth temperature, if there are device processing steps which require high temperatures, or if the desired device will be exposed to high temperatures.

2.2.4 Summary of SiGeSn

Widespread research of $Si_yGe_{1-x-y}Sn_x$ is challenging due to the difficulties involved in both the material growth and the subsequent materials characterization. The effect of decoupling lattice parameter, composition and bandgap by incorporating both Si and Sn into the Ge matrix is both a large advantage for potential device applications of the alloy and a challenge to its development. Determining a unique composition is not possible solely with XRD measurements, which is the standard method for much of group IV semiconductor development.

As the incorporation of Si atoms in several ways counteracts the effect of incorporating Sn atoms into Ge, many of the potential advantages of the binary $Ge_{1-x}Sn_x$ alloy, such as a narrower bandgap with a greater degree of directness, are more challenging to achieve with the ternary alloy. Thus, the major characteristics of epitaxial layers of $Si_yGe_{1-x-y}Sn_x$ alloys that are exploitable for applications are lattice matching and band engineering which take advantage of the decoupling of bandgap and lattice parameter. However, a large range of potential devices are possible with direct bandgap or almost-direct bandgap $Si_yGe_{1-x-y}Sn_x$ alloy based devices [78].

2.3 Epitaxial growth

Epitaxy is the process of growth of a single-crystal film on a crystalline substrate, where the film adopts the crystalline structure and orientation of the substrate. Homoepitaxy is the case where the film composition and substrate composition are essentially identical, such as a silicon epilayer grown on a silicon substrate. In homoepitaxy, the film may have a variable doping profile or may be of a higher crystal quality than the growth substrate.

Heteroepitaxy is the case where the crystal film has a different composition than the substrate, for example a germanium epilayer grown on a silicon substrate. A different substrate to the epilayer may be used for application functionality reasons – the substrate may have useful properties for the intended application of the structure, but also the substrate may be chosen for economic reasons. Many structures are grown on silicon with the major motivation being that high quality silicon substrates are cheap and relatively easy to acquire with a reasonable mechanical strength and moderate thermally conductivity.

Heteroepitaxy can lead to lattice strain, the formation of lattice defects, the modification of the electrical properties of epitaxial layers compared to their bulk state, and modifications to the different layers thermal properties. The different layers may have sufficiently different chemical properties to allow for preferential chemical etching [81].

2.3.1 Thin Film Growth

The aim of semiconductor thin film growth is to produce high quality, single crystal thin semiconductor films. It is desirable to be capable of growing layers with thickness in the range of a several nanometers to few microns, for all layer thicknesses the film must be evenly spread over entire growth substrate – which can be up to 450 mm in diameter.

The ideal growth produces a structure which is essentially identical across the growth substrate. This requires complete film coverage, with constant thickness and composition of the film across the substrate. Ideally, the growth target should have as low a defect density, with the minimum lattice dislocations. The (multi)layers should be monocrystalline, with a very smooth surface. These material properties are

optimal for quality semiconductor devices, and are desirable for measurement accuracy for several characterization methods.

2.3.1.1 Growth Morphologies

There are three potential growth morphologies in thin film growth.

Firstly, there is ideal two dimensional film growth (Frank–van der Merwe). In this growth morphology adatom-substrate interactions dominate over adatom-adatom interactions, leading to perfect 2D film growth. Each atomic layer of the crystal is completed before any growth of subsequent layers is initiated. This growth morphology leads to the formation of pristine monocrystalline layers, with a very smooth surface. This is therefore the ideal growth morphology for thin film growth.

Secondly, there is three dimensional island growth (Volmer–Weber). In this growth morphology adatom-adatom interactions dominate and are stronger than adatom-substrate interactions. This leads to the growth of multiple separate crystalline areas on the growth substrate, which merge as growth progresses and in some circumstances form a polycrystalline layer with multiple crystal grain boundaries and defects. This growth morphology can produce a comparatively rough surface. This is therefore an undesirable growth mechanism.

Finally, there is a combination of the previously mentioned two dimensional film growth and three dimensional island growth (Stranski-Krastanov). In this growth morphology, the initial crystal growth is the perfect 2D layer Frank-van der Merwe growth morphology; however, after several crystal layers have been grown imperfections begin to form as distinct clusters and 3D islands form in Volmer-Weber type mechanism.

2.3.2 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is a widely used method for growing crystalline thin film epitaxial layers, the technique was first developed at Bell Labs in 1975 producing this layers of III-V alloys [82]. In MBE, the growth substrate is placed in a vacuum chamber and molecular beams of the desired elements are directed at the substrate surface to produce the target structure with high levels of control on layer thickness and composition. A schematic diagram of a MBE growth chamber is given in Figure 2-6.

For the MBE growth of $Ge_{1-x}Sn_x$ layers it necessary to grow at low temperatures, typically ranging from 50 °C to 250 °C, to prevent Sn segregation due to metastable nature of high Sn fraction $Ge_{1-x}Sn_x$ alloys [17,60,83,84].

MBE was the first growth method to produce crystalline $Ge_{1-x}Sn_x$ epilayers, and
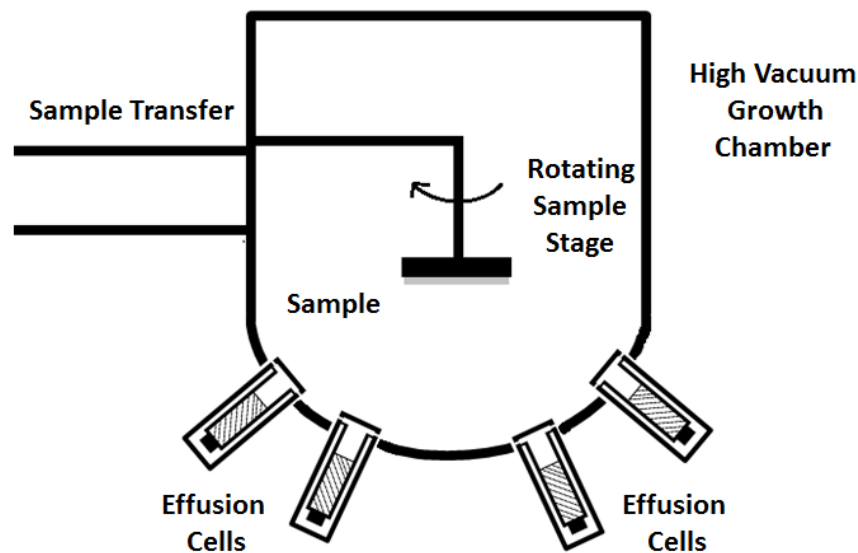
Figure 2-6 A schematic diagram of the molecular beam epitaxy growth chamber. A vacuum chamber is used for growth, in order to minimise contamination. The growth substrate is loaded onto a stage, which can be rotated during growth for improved layer homogenaity. Molecular beam elemental sources are provided by effuision cells directed at the growth substrate.

growth on non-standard substrates, which is useful for lattice matching the substrate to higher Sn fraction alloys, has also been demonstrated [85,86].

MBE has been used to produce epitaxial layers of high Sn fraction crystalline alloys, with Sn fractions significantly greater than the equilibrium limit of $Ge_{1-x}Sn_x$ alloys [60,66,84]. The crystal quality of recent MBE grown $Ge_{1-x}Sn_x$ layers has been sufficiently good to produce devices [19,45,46]. This is matched with additional capacity to introduce dopants in-situ now becoming well developed [19,87].

However, the production volume cannot be effectively scaled, as MBE is a relatively low throughput method, with large run times needed to produce individual wafers. It is therefore necessary to transition to an alternative growth method if production is to be scaled to significant volumes required for the production of consumer devices.

2.3.3 Chemical Vapour Deposition

As its name suggests, chemical vapour deposition (CVD) is a method of epitaxial crystal growth by chemical processes. CVD is the growth method used to produce the samples which are investigated in this work. Chemical reactions between gas phase precursors are used to produce epitaxial layers on a variety of growth substrates. In this section I will discuss the progress, challenges and methodology of crystalline $Ge_{1-x}Sn_x$ alloy growth by CVD.

2.3.3.1 Progress of Chemical Vapour Deposition growth of Germanium-Tin Epilayers

Growth of crystalline $Ge_{1-x}Sn_x$ epitaxial layers by CVD was first demonstrated in 2002, utilizing Ultra-High-Vacuum CVD (UHV-CVD) configuration at Arizona state university [34]. In order to produce single crystal $Ge_{1-x}Sn_x$, several Sn precursor

gases were trailled. SnH_4 was recognised as too unstable, and attempts at growth using SnD_3CH_3 proved unsuccessful [14]. Growth was finally achieved with tin-deuteride, SnD_4, which can be stabilised by storing in gas canisters and diluting with H_2 gas. Digermane, Ge_2H_6, gas was used as the Ge source. In this work growth temperatures from 250 – 350 °C were used, above what is typical for MBE growth of $Ge_{1-x}Sn_x$ but significantly below what is found in Si or Ge CVD growth. $Ge_{1-x}Sn_x$ layers were produced with Sn fractions from 13-17 at. % were produced using the lower temperature range from 250 to 290 °C, with the lower Sn fraction alloys, from 2 to 12 at. % Sn, being produced at the higher range of growth temperatures from 300 to 350 °C. The $Ge_{1-x}Sn_x$ epilayers in this work were fully strained relaxed and grown directly onto Si(001) substrates, with thicknesses in the range from 50 to 500 nm. The crystallinity of the low Sn fraction alloy layers was very good, with Rutherford backscattering spectroscopy (RBS) channelling yields of $\chi_{min} = 4\%$ for a $Ge_{0.98}Sn_{0.02}$ layer, where min is the ratio between the ratio of peak heights when aligned to a lattice planed and when at a random angle for RBS spectra, which is comparable to high quality epitaxial Ge. However, the crystallinity dropped to for higher Sn fraction alloys, with $\chi_{min} = 35\%$ for the $Ge_{0.88}Sn_{0.12}$ layer, this high value is indicative of significant degradation of the crystallinity attributed to mosaic spread within the layer reducing the determined crystallinity. A higher χ_{min} value indicates a greater proportion of atoms in the material under investigation are not positioned at lattice sites, hence a lower crystallinity.

In 2003 the same group expanded this work producing alloys with Sn fractions up to 20 at. % Sn, but again a low fraction of substitutional Sn was found for higher Sn fraction alloys ($\chi_{min} = 50\%$ for $Ge_{0.86}Sn_{0.14}$ layer), indicating that crystallinity is becoming a serious issue at high Sn fractions. Work was initiated to construct a

modified Vegard's law for the fundamental bandgap of crystalline $Ge_{1-x}Sn_x$, by comparing x-ray diffraction data and RBS data to ellipsometry data from samples with a range of $Ge_{1-x}Sn_x$ alloy compositions, and examining the effect of Sn incorporation on the materials' bandstructure [14,88]. In the same year research was published on the successful growth of crystalline layers of the ternary $Si_yGe_{1-x-y}Sn_x$ alloy using the same UHV-CVD growth method, with the SiH_3GeH_3 precursor being used as the Si source. These ternary alloy layers were grown onto $Ge_{1-x}Sn_x$ alloy ($x = 0.03-0.04$) buffers. The $Si_yGe_{1-x-y}Sn_x$ epilayer and $Ge_{1-x}Sn_x$ buffer were both grown at 350 °C. Two layers with different compositions, $Si_{0.14}Ge_{0.84}Sn_{0.02}$ and $Si_{0.14}Ge_{0.80}Sn_{0.06}$ as determined by RBS, were produced by varying the Sn precursor concentration at a constant growth temperature [89].

The Arizona university group was the sole institution producing crystalline $Ge_{1-x}Sn_x$ layers using the CVD growth for some time - to a large extent the reluctance of other institutions to reproduce the growth method was due to the difficulty and high expense of acquiring the SnD_4 gas used as the Sn precursor. Additionally, it remained uncertain whether crystalline growth was possible at higher growth chamber pressures. In 2011, nine years after the initial publication of CVD growth, both of these issues were addressed by Atmospheric-Pressure CVD (AP-CVD) growth of crystalline $Ge_{1-x}Sn_x$ layers on thick-Ge buffer on Si(001) substrates at IMEC, using the commercially available and thermally stable $SnCl_4$ precursor, commonly used for tin-oxide growth, as the Sn source [35]. As $SnCl_4$ is liquid at room temperature, a bubbler system is required to deliver the precursor in the gas phase. $Ge_{1-x}Sn_x$ layer growth was conducted at a fixed 320 °C temperature, which is within the temperature range used in the previous research by the Arizona group. With these growth conditions, a peak $Ge_{1-x}Sn_x$ alloy Sn fraction of 8 at. % was

achieved. Rapid thermal anneals (RTA) were conducted on these structures at 400 °C and 500 °C for both 10 and 30 minutes in N_2 atmosphere. The 30 minute anneals at 500 °C were found to degrade the $Ge_{1-x}Sn_x$ epilayer, with the Sn atoms diffusing in the Ge buffer. The $Ge_{1-x}Sn_x$ Bragg peak was observed in x-ray diffraction scans of all samples – indicating that even after the most intense anneal the $Ge_{1-x}Sn_x$ epilayer crystallinity was not completely lost. The authors note that if any $Ge_{1-x}Sn_x$ layer strain relaxation was observed, it was not to a significant degree. Also investigated in this work was *in-situ* B doping of the $Ge_{1-x}Sn_x$ layer, it was found that the boron precursor competes with the Sn precursor during growth, with the doped $Ge_{1-x}Sn_x$ layers having a lower Sn fraction to undoped layers grown under otherwise similar growth conditions. These are the initial results of the thermal (in)stability of $Ge_{1-x}Sn_x$ epitaxial layers grown by CVD.

The growth of crystalline $Ge_{1-x}Sn_x$ epilayers by Reduced-Pressure CVD (RP-CVD) was first demonstrated in 2012 in Juelich. This work demonstrated the growth of $Ge_{1-x}Sn_x$ alloys with a Sn fractions up to 10 at. %. For $Ge_{1-x}Sn_x$ growth this work used the now established Ge_2H_6 and $SnCl_4$ precursors. The CVD uses a vertical 'showerhead' set-up in order to improve layer growth uniformity and reduce precursor gas consumption [43]. In this work the $Ge_{1-x}Sn_x$ growth temperature range used was higher than reported previously, from 375 °C to 475 °C, this apparent discrepancy is attributed to the substrate temperature being measured by thermocouples encased in a graphite susceptor with heating provided by IR lamps leading to incorrect temperature measurements. This work demonstrated that the low temperature growth rate of pure Ge can be increased by using N_2 carrier gas instead of H_2 carrier gas and using Ge_2H_6 rather than GeH_4 as the Ge precursor source. $Ge_{1-x}Sn_x$ layers were grown directly onto a Si(001) substrate, without a Ge buffer.

The growth temperature ranged from 375-475 °C, with the precursor partial pressure ratio also varied at each temperature regime. In this $Ge_{1-x}Sn_x$ epilayers with a range of compositions from $x = 0.035$ - 0.18 were demonstrated. However, for higher Sn fraction $Ge_{1-x}Sn_x$ alloys RBS minimum channelling yields were very high, up to $\chi_{min} \sim 100\%$ for Sn, indicating significant Sn segregation. Lower Sn fraction epilayers showed better crystallinity with ~3.5 at. % Sn epilayers, having channelling yield for Ge $\chi_{min} = 12\%$ and Sn $\chi_{min} = 50\%$, which though still rather high compared to similar compositions in other works, these values are an improvement on the higher Sn fraction alloys. The relatively low crystallinity of samples in this work compared to previous work is attributed, at least partially, to growing directly onto Si rather than via a Ge buffer. Note in this work as with others, increasing the maximum Sn incorporation into the $Ge_{1-x}Sn_x$ layer is achieved by decreasing the growth temperature.

Since the publication of these initial works, the CVD growth of crystalline layers of $Ge_{1-x}Sn_x$ alloys has continued to progress, with high quality crystalline $Ge_{1-x}Sn_x$ samples now being produced by commercial companies for research and development purposes [90]. Details of the rapid progress of CVD growth of crystalline growth by the refinement of growth parameters by the research community are available in the literature [61].

2.3.3.2 Chemical Vapour Deposition Functionality

A spectrum of CVD system growth pressures exist though they can be categorized as Ultra high vacuum CVD (UHV-CVD) which operate at pressures of approximately 10^{-3} mbar for $Ge_{1-x}Sn_x$ growth. Reduced pressure CVD (RP-CVD) growth, which operates at pressures approximately 50 mbar. Lastly, atmospheric pressure CVD

(AP-CVD) growth, which operates close to ambient atmospheric pressure, ~1 bar. The continued use of a range of CVD operating pressures in $Ge_{1-x}Sn_x$ research exists due to the effect of chamber pressure on growth mechanics and the distribution of reactors among the research community.

It has been suggested that UHV is further from equilibrium conditions and thus better suited to produce meta-stable alloys such as $Ge_{1-x}Sn_x$, however the now repeatedly demonstrated growth of $Ge_{1-x}Sn_x$ at significantly higher pressures has essentially overturned this initial assumption of the need for low pressures to achieve out-of-equilibrium growth for $Ge_{1-x}Sn_x$ [35]. More generally a lower chamber pressure allows for more complete mixing of gases and thus prevents inhomogeneous growth. However, the limited gas concentrations limits the material available for growth.

Metal organic CVD (MOCVD) uses different strains of precursor, opens up the possibility of a larger range of the growth conditions. Successful growth of crystalline $Ge_{1-x}Sn_x$ layers has been demonstrated by MOCVD, but the Sn fractions of the produced alloys has typically been lower than achieved with the more standard inorganic CVD methods [91,92].

CVD growth is capable of having a high throughput and for this reason is the thin film growth method of choice for industrial scale production. However, CVD offers less control of the grown material than other methods such as MBE. Additionally, some of the precursor gases used in CVD are hazardous and thus significant safety systems are necessary for their safe use. It is also vital for CVD reactors to be very clean as any contaminates can seriously disrupt any further growth, for this reason regular maintenance is needed when using CVD for epitaxial growth which increases production costs.

A schematic diagram of a RP-CVD reactor is shown in Figure 2-8 and Figure 2-7 describes the general process for the CVD growth of a thin film layer. Once a substrate has been loaded into the reactor an suitably cleaned, gas precursors are transported into the growth chamber. These precursors then decompose with the precursor being adsorbed onto the growth platform surface. A series of chemical reactions then occur, with the unused precursor material being removed from the surface. The adatom may diffuse across the growth platform surface and bond to a site, contributing to the crystal growth.

As previously mentioned, though the simplest possible molecular source of Sn for $Ge_{1-x}Sn_x$ layer growth, the SnH_4 molecule is too unstable to be an effective precursor for CVD growth. Initial research attempts of the CVD growth of $Ge_{1-x}Sn_x$ alloy layers trialled the more stable $(Ph)SnH_3$ precursor as a Sn source but found it to be ineffective [5].

CVD chambers can have a range of carrier gases with H_2 and N_2 being common, the choice is dependent on the growth reactions, carrier gas availability, cost and other considerations. A hot-wall reactor allows for higher growth temperatures and more homogeneous temperatures across the growth platform (eg. Si substrate), facilitating more homogeneous layer growth. However, hot-wall rectors suffer from precursor deposition also occurring on the growth chamber walls, which can be problematic when attempting to repeat growth. Deposition on chamber walls also increases the particulates in the growth chamber, which may introduce contaminates in subsequent growth thus regular cleaning is necessary which increases maintenance costs. Cold-wall reactors in comparison cannot be operated at such high temperatures, and have lower temperature homogeneity, but are less susceptible to parasitic growth.

Precursors and carrier gas transported into growth chamber

↓

Precursor gases decompose

↓

Precursors adsorped on to wafers surface

↓

Reaction occurs at surface

↓

Crystal growth occurs, desorption, diffusion diffusion active molecular fragments

↓

Unreacted precursors are transported out of growth chamber with carrier gas
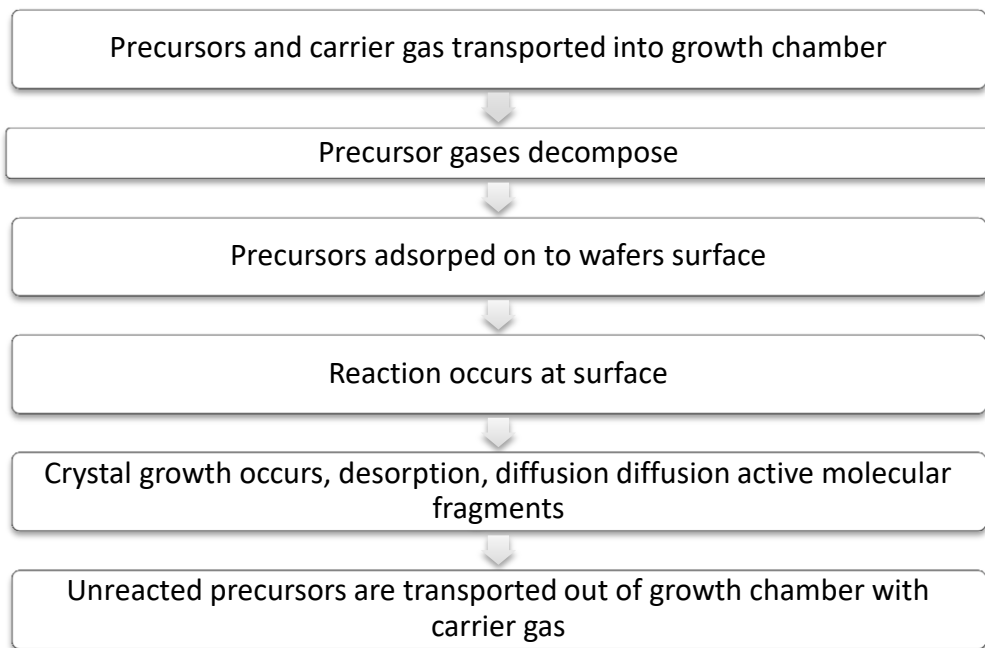
Figure 2-7 Steps of thin film deposition in RP-CVD. The durations of each step varies depending on the reactor, precurors and the target growth structure. Successful growth is dependent on other growth parameters such as growth temperature, suitable growth temperature and gas mixture.
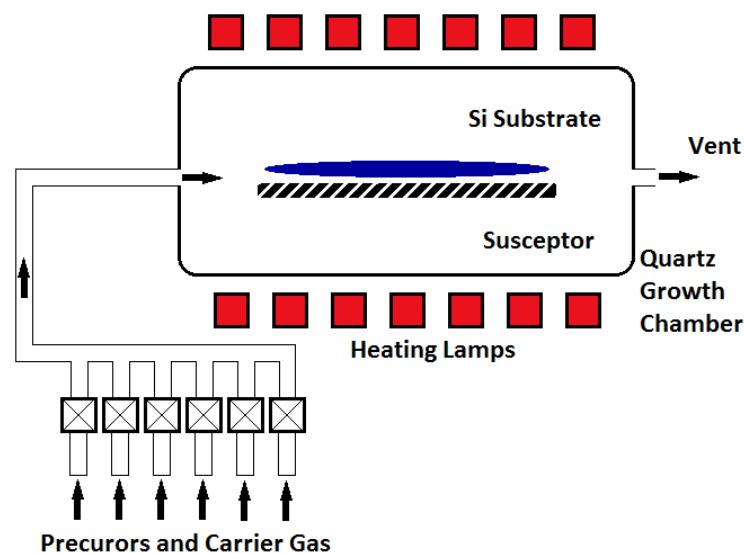
Figure 2-8 A simplified diagram of an RP-CVD reactor. Precursor gases and the carrier gas are input into the reactor from their storage (gas cilinder, or bubbler) with control over individual flow rates to control partial pressure of each precursor. The gas mixture flows into the reactor and elemental source precursors break down over the growth platform – such as a cleaned silicon substrate. The unused gases are vented from the system.

The growth of high quality epitaxial layers of crystalline Si, Ge and Si_yGe_{1-y} by CVD has become quite standard. High quality Ge layers grown onto Si are typically grown in the temperature range from 400 – 700 °C, with very low growth rates in the low temperature regime [93]. By comparison, growth of $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$ alloys by CVD has typically been performed in the temperature range 250 – 350 °C, with the exception of Wirths *et al*., who acknowledge their configuration for substrate temperature measurements means their temperature values may be directly comparable to those of other configurations. CVD growth at the university of Warwick is RP-CVD configuration using an ASM Epsilon type reactor. $Ge_{1-x}Sn_x$ alloy and $Si_yGe_{1-x-y}Sn_x$ alloy epilayers are grown onto Ge-buffered Si(001) 100 mm diameter substrates. The strain relaxed Ge buffer is used to reduce the lattice mismatch with the $Ge_{1-x}Sn_x$ epilayer and supress alloy segregation – explained in greater depth in section [2.2].
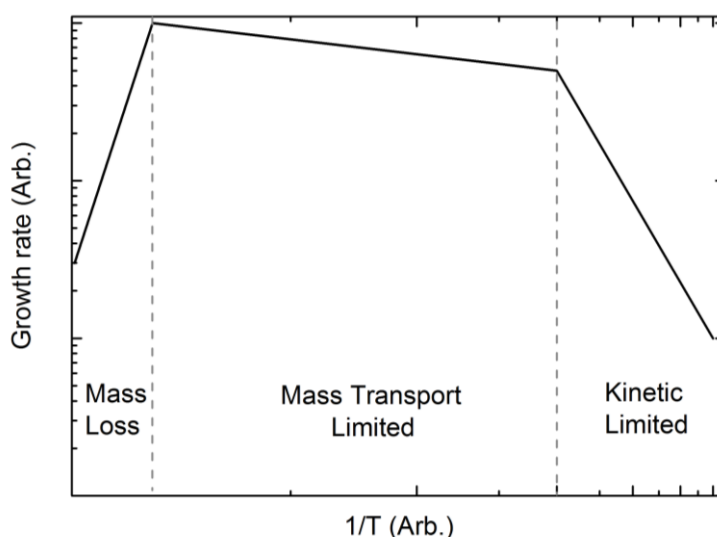

Figure 2-9 A schematic of the growth modes in CVD at different temperature regimes. At low growth temperatures, the growth rate is limited by the temperature. At higher growth temperatures, the growth rate is limited by the chamber pressure. At very high temperatures chemical reactions initiate in the gas phase with the epilayer growth rate declining with increasing temperature.

There are three generally recognised CVD growth regimes for a particular growth mechanism at a constant gas mixture over a range of growth temperatures, as illustrated schematically in the Arrhenius plot in Figure 2-9. At low crystal growth temperatures it is the temperature which is the limiting factor on growth rate, known as kinetically limited growth. Growth is inhibited by insufficient thermal energy to initiate the chemical reactions necessary for crystal growth, hence the growth rate is strongly dependent on the temperature. In this growth regime it is vital that substrate temperature stability and uniformity be maintained.

As the growth temperature increases there is a shift in growth regime and the growth temperature is no longer the limiting factor, which becomes the chamber pressure and the abundance of the precursor gases. This is mass transport limited growth, where the presence of precursor molecules at active sites on the growth surface is the limited factor. In this regime variations in the growth temperature has less impact on the growth rate. The higher thermal energy allows chemical reactions to occur readily between precursors and active sites on the substrate surface.

At even higher growth temperatures the thermal energy is sufficient for chemical reactions to occur in the gas phase, away from the growth surface. This gas phase nucleation leads to a decrease in the crystal growth rate. In this growth regime increases in the growth temperature decrease the growth rate.

2.3.3.3 Calibration

In this work we will be examining Ge/Si, $Ge_{1-x}Sn_x$/Ge/Si and $Si_yGe_{1-x-y}Sn_x$/Ge/Si structures. It will be necessary to understand the growth of both the Ge buffers and the $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$ epilayers.

It is necessary to calibrate the specific reactor used for the growth of any novel materials and to recalibrate it after any maintenance or reactor modifications. Reproducibility, the ability to produce a similar material of a similar thickness on different growth runs, is vital for all material growth methods with the aim of material development. Because CVD growth is challenging, due to the extreme sensitivity of the final material on small changes to growth conditions, and additionally as crystalline $Ge_{1-x}Sn_x$ alloy growth by CVD is not well established it is important to reproduce growth to isolate changes due to systematic changes from random variables. Of particular concern is any changes to the growth conditions which lead to the production of segregated alloy layers, it is necessary to understand what attributes lead to this these undesirable growth products.

In this work the $Ge_{1-x}Sn_x$ layers were grown on Ge buffers, which were approximately 800 nm thick, which is sufficiently thick to minimise the density of threading dislocations reaching the interface. The Ge buffer is under slight tensile strain, typically ~104.5% relaxed relative to the Si substrate, this 'over relaxation' is due to the mismatch of thermal expansion coefficient between silicon and germanium. The Ge layer fully relaxes at the growth temperature, but as it is still bound to the Si lattice upon cooling to room temperature it experiences slight tensile lattice strain. The Si substrate is 100 mm in diameter and approximately 1 mm thick. All Si substrates have the (001) orientation, except where stated otherwise in the off-axis growth section.

2.3.3.4 The Challenges of GeSn CVD Growth

In this section the challenges of producing crystalline $Ge_{1-x}Sn_x$ thin films using CVD are discussed. While the focus is challenges encountered when using the CVD

method, some of the issues examined are inherent to the alloy and thus also pose challenges with alternative growth methods.

Due to the metastable nature of higher Sn fraction $Ge_{1-x}Sn_x$ epitaxial layers, CVD growth requires low temperatures, with a typical maximum growth temperature of 350 °C for alloy Sn fractions significantly greater than the equilibrium. Such low growth temperatures result in lower growth rates relative to standard growth rates of other group IV materials which are typically grown at higher temperatures.

As material grown using several standard precursors, such as GeH_4 and SiH_4, has vanishingly small growth rates in the low $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$ growth temperature range (because the thermal energy available is insufficient to sustain the necessary chemical reaction mechanisms), alternative precursors must be sought. Desirable precursors should therefore have a lower activation energy. For a Ge source this means using higher order germanes: digermane (Ge_2H_6) is a standard for $Ge_{1-x}Sn_x$ and is used to produce the samples examined in this work. It should also be noted that research has shown clear advantages of using trigermane over digermane, with higher growth rates at a constant temperature and a lower minimum $Ge_{1-x}Sn_x$ growth temperature, but these advantages come with a prohibitively high costs [53].

Finding a suitable Sn source poses another challenge. While SnH_4 and SnH_3CH_3 have both been identified as poor Sn sources, those that have been successfully used come with trade-offs. As previously stated, SnD_4 is unstable for long term storage and expensive to acquire, while $SnCl_4$, though more standard, requires a bubbler system for delivery and the liberated Cl_2 must be efficiently removed from the growth chamber.

It is important to prevent segregation, precipitation and to an extent mosaic spread of $Ge_{1-x}Sn_x$ epilayers. Growth of high Sn fraction alloys gives poor crystal quality and

Sn precipitates. For growth of any significant Sn fraction (>1 at. %) single crystalline layer it is necessary to grow at low temperatures to supress segregation, but other considerations are also necessary. Segregation can be reduced by not growing directly onto a Si substrate, but using a Ge buffer or substrate to minimise the lattice mismatch; however, this increases the growth time and increases the cost. Note, when using the SnD_4 precursor direct growth onto Si is still common [94]. In order to prevent the surface segregation of Sn, the growth must be sufficiently fast to prevent the build-up of a pure Sn layer on the surface, which would prevent further crystalline growth as no Ge can be incorporated into the Sn matrix.

To increase the Sn fraction in the $Ge_{1-x}Sn_x$ grown it is necessary to further reduce the growth temperatures. This shifts growth further from equilibrium conditions, which means adatoms have insufficient (thermal) energy to move on the growth surface to energetically favourable sites. However, growth rate at such low growth temperatures is vanishingly small and, as previously mentioned, increasingly novel and often expensive precursors are required, which may not be economically viable for industrial production [95]. The trade-off between a low growth temperature for more Sn incorporation with a sufficiently high growth rate to supress segregation puts a lower limit on the growth temperature for a particular configuration.

A precise value for the α-Sn lattice parameter is necessary to produce an accurate bowing parameter for the modified $Ge_{1-x}Sn_x$ alloy Vegard's law, which accounts for the degree of deviation of the $Ge_{1-x}Sn_x$ lattice parameter from a simple weighted average of the Ge and α-Sn lattice parameter. However, attaining a precise lattice parameter for α-Sn is challenging as historically it was difficult to produce sufficiently large crystalline samples suitable for XRD measurements and these samples required an environment below the phase transition temperature (13 °C). As

such there is a small degree of disparity on the accepted value, although the $Ge_{1-x}Sn_x$ research community has settled on a 0.041 Å.

2.3.4 Novel Growth Methods

Other than MBE and chemical vapour deposition, discussed in the previous sections, alternative methods of producing semiconducting crystalline $Ge_{1-x}Sn_x$ alloys have been developed with some success. These methods have been investigated in an attempt to overcome several of the issues of other growth methods. The target being the ability to produce crystalline layers of $Ge_{1-x}Sn_x$ binary alloys at a low cost, using a reproducible method, preferably with potential for high throughput.

A method involving the rapid melting growth of a Sn layer deposited between two amorphous Ge layers has been investigated and is capable of producing laterally graded composition profiles. However, while this method produced $Ge_{1-x}Sn_x$ layers with Sn fractions above the equilibrium limit, achieving Sn fractions greater than ~3% may not be possible with this method as significant Sn precipitates observed [96]. The slow annealing at very low temperatures of amorphous Ge and Sn has produced layers with higher Sn fraction $Ge_{1-x}Sn_x$ alloys, but these layers were polycrystalline [97]. Quicker and higher temperature anneals of amorphous Ge and Sn materials are able to produce single crystal layers, but with a significantly reduced Sn fraction [98]. Solid phase epitaxy has achieved moderate Sn fraction alloys, but with a low crystallinity [99]. Liquid-phase epitaxy has even been attempted, but increasing the Sn fraction of the $Ge_{1-x}Sn_x$ alloy layers proved to be detrimental to the layer quality [100].

The ternary $Si_yGe_{1-x-y}Sn_x$ alloy has also been produced by solid phase mixing. By this method a crystalline layer of the binary $Ge_{1-x}Sn_x$ alloy was deposited by MBE onto

an oxide layer, a SiO_2 cap was then deposited. This structure was then annealing to form the ternary alloy [101].

This common issue with many growth methods is the lack of control over the produced materials. It is challenging to produce a homogeneous layer of the high Sn fraction alloy with a good crystallinity.

2.3.5 Relaxation and Critical Thickness
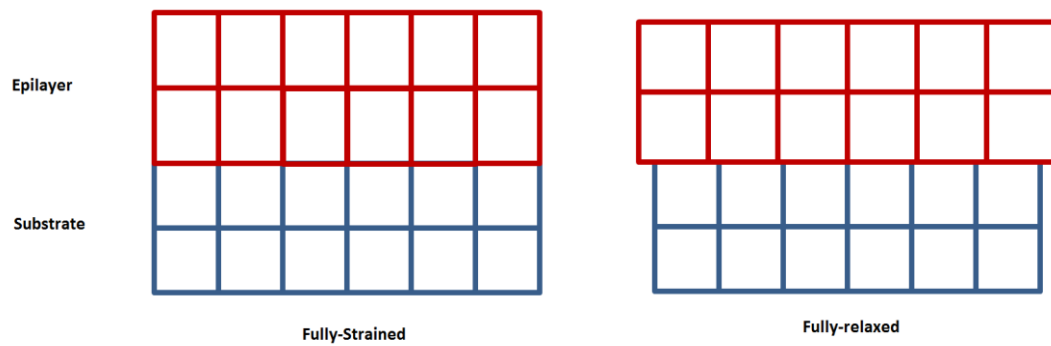
Figure 2-10 Schematic diagram of the effect of growing epilayers above the critical thickness. Below the critical thickness the epilayer in-plane lattice is matched to the substrate. Growth of thicknesses above the critical thickness the epilayer starts to relax until it reaches full relaxation.

During the initial stages of heteroepitaxial growth the initial epilayer atomic layers are fully strained to the crystal lattice of the substrate. This means the epilayer in-plane lattice parameter is matched to that of the substrate. In the initial atomic layers of the epilayer a strain energy is generated due to the epilayer crystal being deformed from its equilibrium (bulk, cubic) state. For example, a thin fully strained $Ge_{1-x}Sn_x$ layer grown on a relaxed Ge layer will have an in-plane lattice parameter matched to the Ge, with a larger out-of-plane lattice parameter. The $Ge_{1-x}Sn_x$ lattice will therefore be deformed from the equilibrium cubic structure.

For the initial atomic layers the epilayer is able to absorb the lattice strain. As more atomic layers are grown, the strain accumulates until the epilayer in no longer able to absorb all of the strain energy. The layer will mitigate the strain effects by producing dangling bond, lattice defects, these typically start at the interface between the epilayer and the growth substrate and depending on the nature of the two layers will propagate through the structure in a variety of ways.

Thin layered structures where layers have a different lattice parameter are typically strained. The in-plane lattice parameter of the epilayer is strained to that of the growth substrate. The degree of strain is determined by the lattice mismatch calculated using equation 2-4.

$$f_m = \frac{(a_{substrate} - a_{layer\,(bulk)})}{a_{substrate}} \tag{2-4}$$

Where 'f_m' is the lattice mismatch, '$a_{substrate}$' is the actual lattice parameter of the growth substrate and '$a_{layer\,(bulk)}$' is the lattice parameter of the layer material in its bulk state.

Strain can be defined relative to the bulk, i.e. fully relaxed, state of the epilayer or can be defined relative to the growth platform. For example, Ge buffers in this work are defined as 104.5% relaxed, relative to the Si substrate. $Ge_{1-x}Sn_x$ epilayer relaxation values in this work are given relative to the Ge buffer.

The compressive strain of the epilayer distorts the lattice, shifting it from being cubic to slightly tetragonal, i.e. $a_{/\!/} \neq a_{\perp}$. The distortion is still slight, so a cubic lattice notation is still used.

3 Experimental Techniques

In this chapter, the method used to produce the materials for this work and the techniques used to characterize the material properties of samples under investigation are first described and then compared and contrasted. The growth technique chemical vapour deposition is discussed. The materials characterization techniques examined are atomic force microscopy, Secondary ion mass spectrometry, X-ray diffraction, transmission electron microscopy and Raman spectroscopy. These are the main materials characterization techniques used in this work. The fabrication process for transmission line method (TLM) devices is explained and the electrical measurement process is detailed.

3.1 Introduction to Experimental Techniques

Materials characterization is fundamental to experimental condensed matter research. For accurate and precise models of the interrelation of material properties to be constructed, tested, improved and utilized the materials must be realized and tested in the physical world, not solely in computer simulations. Though useful for producing informed predictions, all material simulations are based on conceptual models which contain intrinsic assumptions and simplifications of the materials, which may or may not be sufficiently accurate for predicting the behaviour of the material under investigation. For example, the effect of such a large lattice mismatch and large difference in atomic radii between Ge and α-Sn and the meta-stability of their alloys is not accounted for in many common models used to predict the properties of semiconductors, such as the virtual crystal approximation, which can lead to significant errors in their predictions [5,51,102].

In this work, material characterization is necessary in order to understand the impact of growth parameters, such as growth temperature, on the produced material parameters, such as the alloy composition. Additionally materials characterization facilitates study of the interrelation between material parameters, such as the layer thickness and lattice strain. Additionally, in this work experiments are also undertaken to further our understanding of impact on the material to non-ambient temperatures, and for this the material properties prior to thermal treatments and post-treatments must be determined.

Crucial structural properties for thin layers of $Ge_{1-x}Sn_x$ alloys include the layer thickness, the lattice strain state, the alloy composition, and the crystalline quality, including any lattice defects. The importance of each of structural aspects is highlighted by their effect on the properties of any devices, such as microelectronics or photonic, fabricated from such a material. In this work, materials characterization is focused on determining these properties in the investigated samples.

Electrical characterization is necessary to identify if material parameters and epitaxial structure produces desirable attributes for devices, such as a high charge carrier mobility. Additionally, electrical characterization is used to indicate the optimum device processes for particular applications, such as contact material to form an Ohmic contact. In this work electrical characterization is used to identify the relative quality of metal contacts on $Ge_{1-x}Sn_x$ epilayer samples.

No existing individual characterization technique is capable of accurately providing all of the necessary material information about a given sample, therefore a range of characterization methods are used in order to collect a range of data sufficiently detailed such that a comprehensive understanding of materials can be achieved.

Using multiple characterization methods which measure the same property additionally allows for greater confidence in the measured result.

Characterization techniques vary in what material or device properties they can determine, to what accuracy and from which region of the material. Additionally, some characterization methods are destructive; the investigated material is consumed for the measurement, which prevents the same piece of material being used for further investigation by other characterization techniques. Other experimental measurements are non-destructive, facilitating further investigations on the exact same section of the sample. The range of properties which need to be determined for the desired investigation and the availability of sample material dictate which techniques should be used. Additional constraints may also exist due to time and equipment limitations.

3.2 Chemical Vapour Deposition

All samples investigated in this work were grown at the University of Warwick. Materials growth was performed by my colleague and supervisor, Dr. Maksym Myronov. The RP-CVD reactor used for growth is the cold-wall ASM Epsilon 2000E, a photo of a comparable reactor is given in Figure 3-1. This tool is very well-established, and used throughout the world for both research purposes and commercial scale production of semiconductor thin films. The CVD configuration at the University of Warwick is optimised to grow on a single 100 mm wafers each growth cycle.

For $Ge_{1-x}Sn_x$ epitaxial layer growth, a digermane, Ge_2H_6, gas source was used as the Ge precursor. Digermane is well established as a CVD precursor for the low temperature growth of both Ge and $Ge_{1-x}Sn_x$ layers [103]. Digermane is the optimal

Ge source as it facilitates higher growth rates at low temperatures than the lower order monogermane, GeH_4, precursor; furthermore, digermane is lower cost and more readily available than higher order germanes, such a trigermane, Ge_3H_8 [103–105].

Figure 3-1 A photo of the ASM Epsilon 2000, the same line of CVD reactors to that used to produce the samples investigated in this work. Image modified from image originally obtained from ASM website.

Tin-tetrachloride, $SnCl_4$, was used as the tin source precursor, which is an established CVD precursor used in tin-oxide and $Sn_{1-x}Se_x$ growth and more recently $Ge_{1-x}Sn_x$ alloy growth [19,35,106,107]. $SnCl_4$ is liquid at room temperature; therefore the vapour is delivered to the CVD growth chamber by a bubbler system, with the Sn precursor flow controlled by liquid temperature and carrier gas flow rate. $SnCl_4$ is more readily available and cheaper to acquire than SnD_4, the dominant alternative successful Sn source for crystalline $Ge_{1-x}Sn_x$ CVD growth found in literature, and $SnCl_4$ does not have the issues of instability during storage experienced with SnD_4. Alternative Sn sources have been used in publications, such as $Sn(CH_3)_4$, but for significantly different growth configurations with different target structures [108].

All $Ge_{1-x}Sn_x$ epitaxial layers studied in this work were produced with the growth temperature in the range $250\,°C$ to $350\,°C$. The substrate temperatures are

determined by thermocouples, with heating provided by IR lamps. 350 °C is the maximum $Ge_{1-x}Sn_x$ growth temperature in the published literature, where direct temperature measurements are used, with lower growth temperatures used to produce higher Sn fraction alloy epilayers.

Prior to growth, the 100 mm Si(001) substrate wafer is subject to standard chemical cleans, including a dilute HF rinse to remove the native oxide, both organic and inorganic contaminates, and leave a hydrogen-terminated growth surface. The Si substrate is then loaded into the CVD and transferred to the growth chamber via an automated handling system. Immediately prior to growth, the substrate undergoes a high temperature pre-epi at temperatures below 1000 °C bake to remove any residual SiO_2.
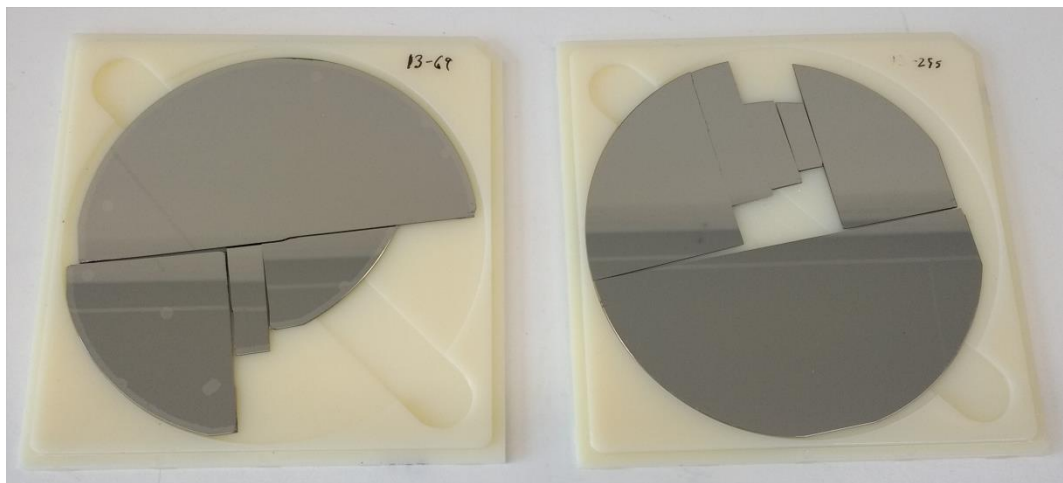
Figure 3-2 Photograph of two GeSn/Ge/Si wafers after being cleaved. The surface of both wafers is very smooth and reflective.

Initially, a 600-800 nm thick strain relaxed Ge buffer is grown by a two-step growth method to provide a smooth and low defect density growth platform essential for the subsequent $Ge_{1-x}Sn_x$ growth [93]. The Ge buffer also serves to minimise the lattice mismatch between the growth platform and the $Ge_{1-x}Sn_x$ alloy epilayer. The $Ge_{1-x}Sn_x$

layer was then grown on the Ge platform, at a constant temperature. Figure 3-2 shows two 100 mm wafers after they have been cleaved.

3.3 Atomic Force Microscopy

Figure 3-3 A schematic diagram of an atomic force microscope in operation. A laser (red) incident on the tip of a silicon cantilever (black) which reflects on to a photodiode array. The tip of the silicon cantilever is rastered over the sample surface (brown), any features on the surface deflect the cantilever and consequently the reflected laser is displaced on the photodiode array. The movement of the beam spot is interpreted as an associated feature.

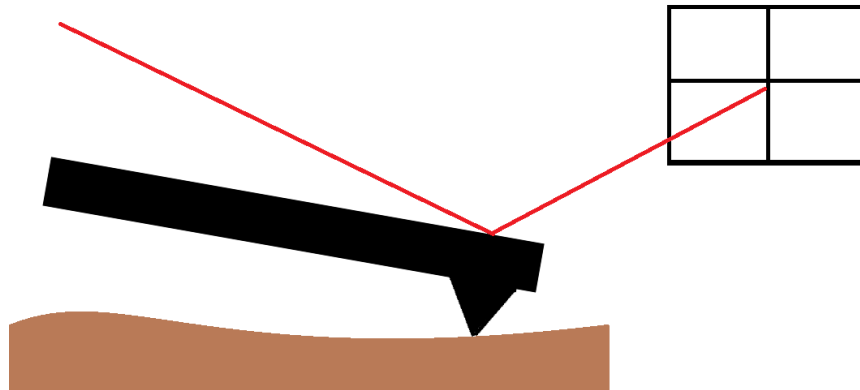Atomic force microscopy (AFM) is a primarily a surface morphology probe. During measurement a cantilever, typically composed of silicon, with a sharp tip protruding from an edge is rastered over the sample surface. A laser, operating in the visible spectrum, is reflected from the surface of the cantilever tip, onto the centre of 2×2 array of photodiodes, a schematic diagram of this is shown in Figure 3-3. As the cantilever tip is moved across the sample any surface topological features encountered on the surface, such as a surface dot or pit, cause the tip to deflect which alters the reflected beam position on the photodiode array, which is interpreted by the analysis software as a corresponding feature.

The photodiode difference in signal of the upper against lower, and left-most against right-most diodes are used to determine vertical and horizontal rotation of the

cantilever, respectively. The degree and type of tip deflection are interpreted as the property of the corresponding feature.

Though the standard AFM configuration is used to measure surface morphology, it is possible to measure other surface parameters with a modified configuration. It is possible to map variations in surface electric potential, electrical conductivity and other properties [109].
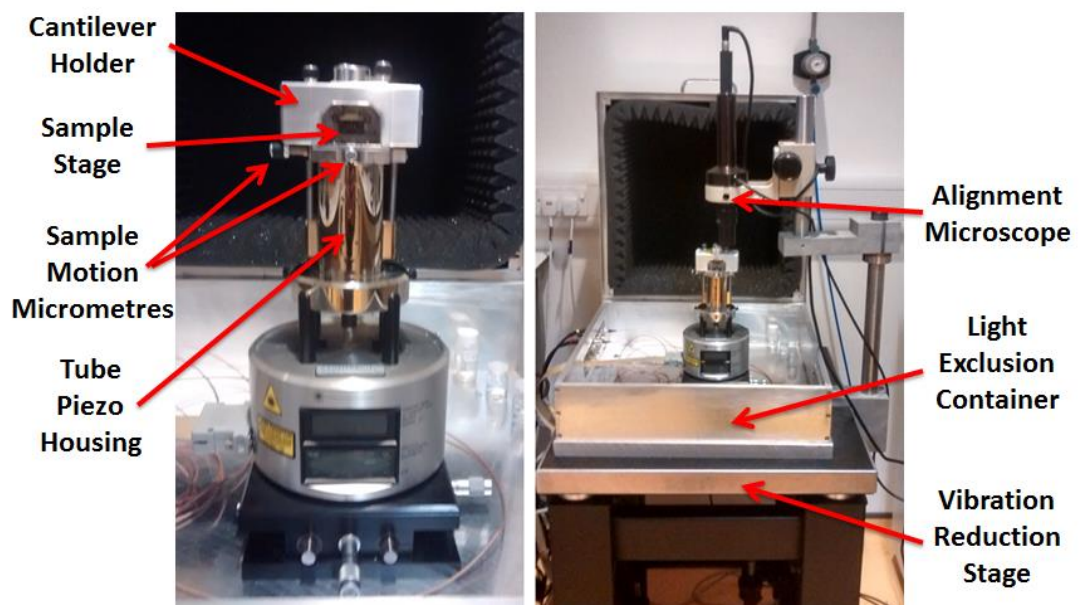
Figure 3-4 Photographs of the Vecco multimode AFM used at Warwick Univeristy. The Micorscope is mounted on a vibration reduction stage and is encased in a noise minimizing container during measurements.

The AFM scans in this work were conducted at the University of Warwick and used a Veeco multimode AFM, shown in Figure 3-4. This microscope is notable for having a tube piezo, which must be accounted for during data analysis.

Two rastering modes are common in AFM, contact and tapping, which are better suited to different ranges of surface roughness. In 'contact mode' the cantilever tip is kept in contact with the sample surface and a constant force applied. When a surface feature, such as a dot or a pit-like feature, is encountered the cantilever height

changes as the applied force is constant, this height change is detected and interpreted.

In 'tapping mode' the cantilever tip is vibrated and is driven at its resonant frequency. When a surface feature is encountered the dampening effect causes the cantilever vibration frequency to change, and the cantilever is raised or lowered correspondingly to return to the resonant frequency.

3.3.1 AFM Image Analysis

The appropriate length scale of the AFM scan must be taken into account. The standard silicon AFM tip has ≥50 nm radius of curvature [110], thus only features of ~0.5 μm in size can be imaged with acceptable accuracy. This places a lower limit on reasonable scan size. An upper limit on scan size is imposed by the range of the piezo on the microscope which is used for scanning, this limit is approximately 100 μm for the Vecco multimode. A reasonable scan size captures a representative image, containing any of the surface features, the underlying background surface and the relative ratio between the two being representative of the sample average. Hence, on relatively featureless (smooth) surfaces, relatively small scan sizes are appropriate; surfaces with a high feature density, such as hill-like features or cross-hatching, are more accurately observed using larger scan sizes. The observed sample surface RMS roughness, a common qualitative measure of surface quality, increases with scan size, but the value will plateau at a minimum representative scan size. An additional consideration is scan speed, a slower scan speed allows the tip position to recover after a perturbation, i.e. a feature; however, this increases the scan duration, which can lead to unacceptably long scans for larger scan areas.

Figure 3-5 shows AFM scans, taken from the same sample, with different scan ranges. The measured RMS roughness increases markedly from 2.3 nm in the smaller 20×20 μm scan to an RMS roughness of 3.0 nm in the 50×50 μm, indicating that the larger scan is more representative of longer range variations.
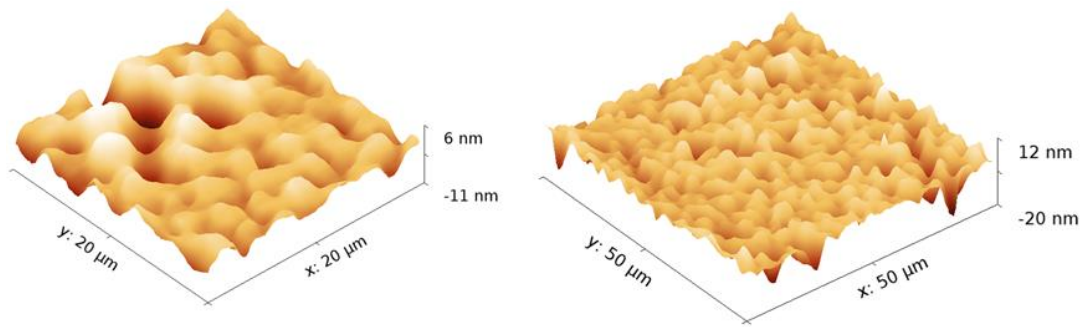
Figure 3-5 Two AFM scan of the same $Ge_{1-x}Sn_x$ epilayer surface. A 20×20 μm scan (left) leads to an observed RMS roughness of 2.3 nm, whereas the larger 50×50 μm scan (right) has a larger RMS roughness of 3.0 nm. The increase in observed roughness indicates the larger scan is more representative, capturing more surface features – irregularly spaced indentations in the surface and better representing the ratio of surface features to smooth surface.

3.3.2 Measurement Attributes

AFM measurements provide a quick, non-destructive method to determine surface roughness and topology. However, AFM cannot directly detect crystal quality, though significant alloy segregation will be detected as micro-scale dots on the sample surface. Additionally, AFM cannot infer layer thickness, epilayer composition and epilayer strain state, which can only be inferred by the presence or absence of surface cross-hatching features.

3.4 Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry (SIMS) is a materials characterization technique used to determine the elemental composition of a thin film structure as a function of

depth from the surface. Crucially, SIMS can determine the concentration of elements which compose only a very small fraction of the whole material with great precision. In semiconductor research and development, SIMS is used to measure alloy composition and doping density as a function of depth of the sample and has played a role in measuring composition for many decades [111].
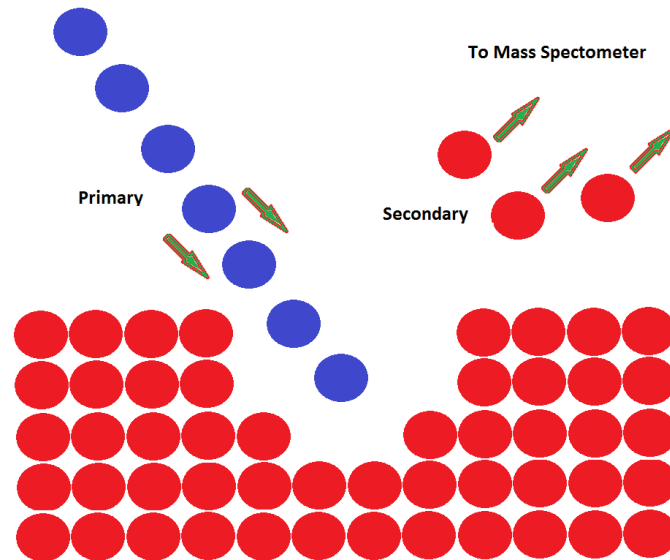
Figure 3-6 A schematic diagram of the generation of the secondary beam during a SIMS measurement. A beam of primary ions (blue) is used to mill atoms from the sample surface (red), these atoms sputtered from the surface form a secondary beam of atoms and ions which are analysed by a mass spectrometer, thus the composition of the layer under investigation can be determined from the ratio of atoms detected from the secondary beam.

During a SIMS measurement a (primary) ion beam, consisting of atoms of an element not present in the sample under study (often O_2^+/O^- or Cs), is incident on a sample surface, which sputters the sample material, see Figure 3-6. The sputtered sample material, a combination of neutral atoms and charged ions, forms the secondary ion beam which is passed through a mass spectrometer, which determines the ions charge/mass ratio to determine the element and if necessary the isotope and their relative abundance in the sample. The material composition is determined by

measuring and comparing the relative abundance of all elements which compose a significant proportion of the material [112].

SIMS can measure extremely low concentrations of a particular atomic species, with detection limits parts of per million being routine. Thus, SIMS can be used to determine the dopant densities in semiconductor structures, which are often at very low concentrations. If the approximate sample structure which is under investigation is known prior to measurement, the milling rate through the sample can be predicted and the elemental concentrations can be profiled against depth. For reasonable accuracy of the depth profile, the initial sample surface must be smooth. The nature of this measurement of milling through the sample makes this a destructive technique and investigated samples are consumed, though a profile area of only ~1 mm^2 is necessary.
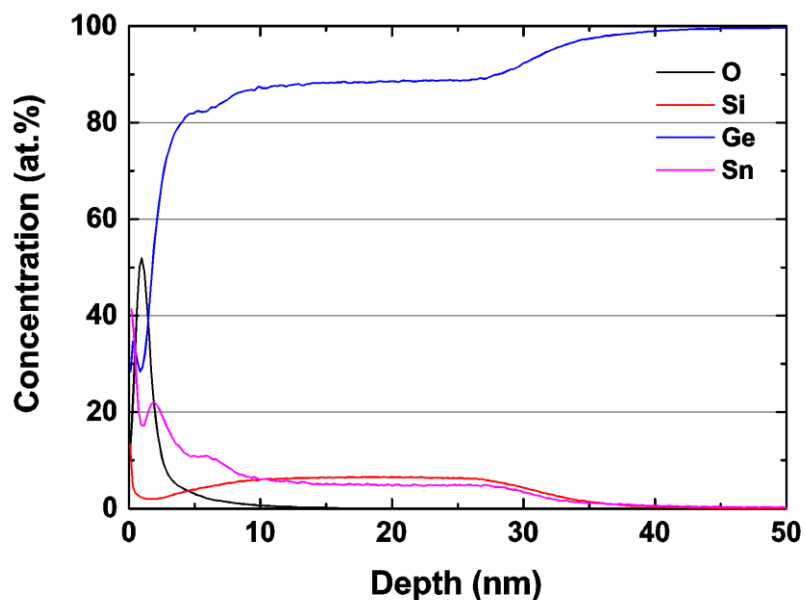

Figure 3-7 An example plot of a SIMS data from a SiGeSn/Ge/Si structure. At a shallow depth there is a high concentration of oxygen, indicating a surface oxide. From a depth of 10 to 30 nm the Si, Ge, Sn concentrations are constant. By a depth of 50 nm the material is high purity Ge.

All SIMS measurements collected for this work were performed by Evans Analytical Group LLC (EAG Laboratories). In this work, SIMS was used to determine the composition of the ternary $Si_yGe_{1-x-y}Sn_x$ alloy epilayers, an example of the data is shown in Figure 3-7.

3.4.1 Measurement Attributes

SIMS can determine the composition of a material to a high accuracy and, by milling, can measure the thickness of layers. However, the composition includes atoms at interstitial lattice sites, which are not of interest in this work. SIMS cannot infer the crystal quality of the material and loses accuracy as milling depth increases. Crucially, SIMS is useful in this work as it can determine the composition of ternary alloys as it doesn't rely on lattice constant measurements. SIMS also gives an indication of the penetration of atmospheric oxygen in the native oxide. However, SIMS is a destructive characterisation method, requires reference to a standard for accurate composition, and is expensive and labour intensive and is therefore not used as extensively as alternative characterization methods.

3.5 X-ray diffraction

X-ray diffraction (XRD) is a widely used and versatile non-destructive characterization method which is primarily used for studying crystalline materials. Single crystals, powdered crystals and, as examined in this work, layered crystal structures can be characterized by XRD. The fundamental parameter obtainable from XRD measurements is the distance of the regular spacing between crystal lattice
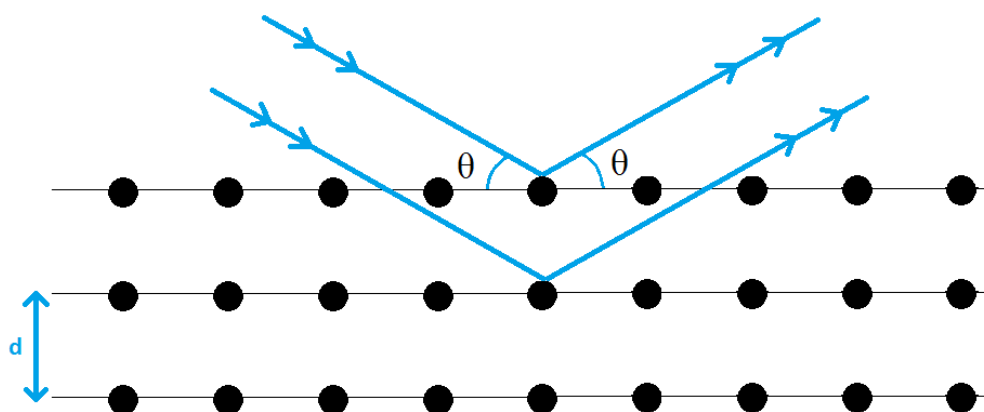
Figure 3-8 A schematic view of an XRD measurement. X-rays (blue lines) diffracting from planes of atoms (black circles), which are seperated by distance 'd', in a 3D periodic array – as found in a real crystal. The incident angle, 'θ', is identical to the exit angle. The X-ray path difference between two adjacent planes is 2dsin(θ). The black lines between atoms for illustratative purposes to highlight the atomic plane investigated.

planes, which can be used to determine the crystal lattice parameter(s), identify an unknown material, determine the composition of an alloy, and more.

3.5.1 Theory

To observe features using electromagnetic radiation the photons must have a wavelength on a similar length-scale or smaller than the features under investigation. Inter-atomic bonds typically have lengths of an Angstrom scale (Å, 10^{-10} m), corresponding to the X-ray region of the EM spectrum, which covers 0.1 Å to 100 Å. Direct imaging of molecular scale structures with X-rays is not possible with a conventional diffractometer or any other simple X-ray characterization method, though X-ray diffractive imaging is possible at some synchrotron sources. However, X-rays are diffracted by crystalline materials, as shown schematically in Figure 3-8. Therefore crystalline structural information can be obtained from X-ray diffraction measurements.

The diffraction of X-rays is succinctly captured in the Bragg equation (or *Bragg's Law*), given in equation 3-1.

$$n\lambda = 2d \cdot \sin(\theta_{hkl})$$
<div align="right">3-1</div>

Where '*n*' is the order of the diffraction, λ is the wavelength of the X-ray, *d* is the lattice plane separation, and θ_{hkl} is the angle between the incident radiation and the crystal lattice plane defined by the *h*, *k* & *l* crystal Miller indices. This equation describes how radiation of a particular wavelength will be diffracted only at discrete specific angles which are dependent on the lattice plane spacing of the material from constructive interference. This equation was first proposed by the father and son team William Henry and William Lawrence Bragg in late 1912/early 1913 earning them the 1915 Nobel Prize in physics.

3.5.2 Lab Based X-ray Sources

Standard laboratory based X-ray sources function by exciting electrons from an anode and accelerating the liberated electrons with a strong electric field, typically 20-50 keV, onto the X-ray source, a metal target (typically copper though other materials are also used such as tungsten). The electron beam liberates bound atomic electrons in the (copper) target, producing a vacancy in the atomic electron shell. Other bound atomic electrons relax to this more tightly bound state, releasing a photon of specific energy, characteristic of the target material, such as Cu K_α. In addition to the strong emission lines, a broad energy spread of X-rays are also produced by Bremsstrahlung radiation from the rapid deceleration of the electron beam striking the metal target. To produce a monochromatic beam, undesired X-ray wavelengths are filtered using a series of high quality crystals, typically Ge, at a chosen Bragg angle to allow a low bandwidth beam with a specific wavelength to be

transmitted. The bandwidth which passes through the crystal monochromator is determined by the crystal quality, with higher crystal quality producing a narrower band; though at the cost of decreasing X-ray beam intensity available for diffraction experiments.

The hyperfine splitting Kα radiation in copper (1.54184 Å) produces two discrete energy levels (creatively named) Kα_1 and Kα_2, in copper these have a wavelength of 1.54056 Å and 1.54439 Å, respectively. For high resolution diffraction investigations a single one of these emission line is used, in this work the Cu Kα_1 emission line is used in XRD experiments [113].

The intensity of the X-ray beam in lab based sources can be their limiting factor in their use. The ongoing challenge is the target material heating due to the electron bombardment, despite target rotation and water cooling. Significant intensity increases in standard X-ray sources have not been achieved in recent decades. As a result large, detailed scans, such as heterostructure reciprocal space maps (RSMs), and scans of weakly interacting samples, such as very thin layers with small diffraction volumes, require long scan durations.

X-ray diffraction is a bulk sensitive characterization method, the diffracted beam is from the entire interaction volume with the penetration of the beam, typically down to a sample depth of ~100 μm and the beam width typically ~1 mm. This bulk sensitivity complicates data acquisition from features for which all dimensions are smaller than the beam width. Thus the detected signal from features such as nanodots, which have a width of the order of microns, is complex to isolate from the diffracted signal from the rest of the diffraction volume.

For this work lab based high resolution XRD was performed at the University of Warwick using a Panalytical X'Pert Pro MRD equipped with Cu Kα_1 hybrid

monochromator configured with a detector receiving slit for high resolution. X-ray measurements were performed on $\sim 2 \times 2$ cm sample sections, which were cleaved from close to the centre of the $Ge_{1-x}Sn_x$/Ge/Si sample wafer.

3.5.3 The Reciprocal Lattice

The *reciprocal lattice* is a useful concept when dealing with X-ray diffraction from crystals. The reciprocal lattice is simply the Fourier transform of the electron density of crystal lattice in real space, producing a periodic set of reciprocal lattice points of finite size in momentum space (k-space).

Momentum space is used in X-ray diffraction analysis, which eases the conceptualisation of the Laue condition: the change in momentum, i.e. momentum transfer, between an incident and scattered x-ray beam photon must coincide with a reciprocal lattice vector for diffraction to occur [1].

3.5.4 Structure Factors

All materials studied in this work (Si, Ge and their alloys including α-Sn) have a diamond cubic structure, which possess a face-centred cubic (FCC) lattice symmetry. The lattice symmetry imposes additional conditions for the observation of a Bragg reflection from a lattice plane. For a reflection from a diffraction plane to be observable, each of the Miller indices (h, k, l) which describe the diffraction plane must be either all odd or all even.

The atomic radius of the atoms in a crystal also affects the relative intensity of the Bragg reflections from a particular material. Given in Table 2 are the structure factors of Si lattice. Note that the commonly used symmetric (004) and asymmetric (224) reflections are amongst the higher structure factors of the material, resulting in

a higher scattered beam intensity for an otherwise identical set up from another Bragg reflection.

Reflection	001	002	004	111	222	333	011	022	044	112	224	113	115
$\|F_{hkl}\|$ V in electron units per Å^3 for one crystal of Si	0	0	0.39	0.38	0	0.24	0	0.45	0.31	0	0.35	0.3	0.24

Table 2 Values of $\|F_{hkl}\|$ V in electron volts for silicon for a number of useful reflections.

3.5.5 Rocking Curves and Reciprocal Space Maps

In semiconductor materials science a coupled ω-2θ scan, where the sample is rotated about the ω-axis and the detector is moved in a coupled manner along 2θ, see Figure 3-9, is a referred to as a "rocking curve" and series of coupled ω-2θ scans with varied starting ω value used to map diffracted beam intensity in reciprocal lattice space in the in-plane direction and out-of-plane direction is referred to as a "reciprocal space map" (RSM). In more general X-ray diffraction a different naming convention is used, a coupled ω-2θ scan is a "coupled scan" and a "rocking curve" is a scan from rotating solely the sample (ω-scan) without moving the detector (2θ), a plot of intensity against in- and out-of-plane reciprocal lattice space is referred to as a "momentum transfer map", while a plot of intensity against the Miller indices (h, k, and l) being a "reciprocal space map". As this work has its foundation in semiconductor materials science, it is this former notation that will be used in this work.
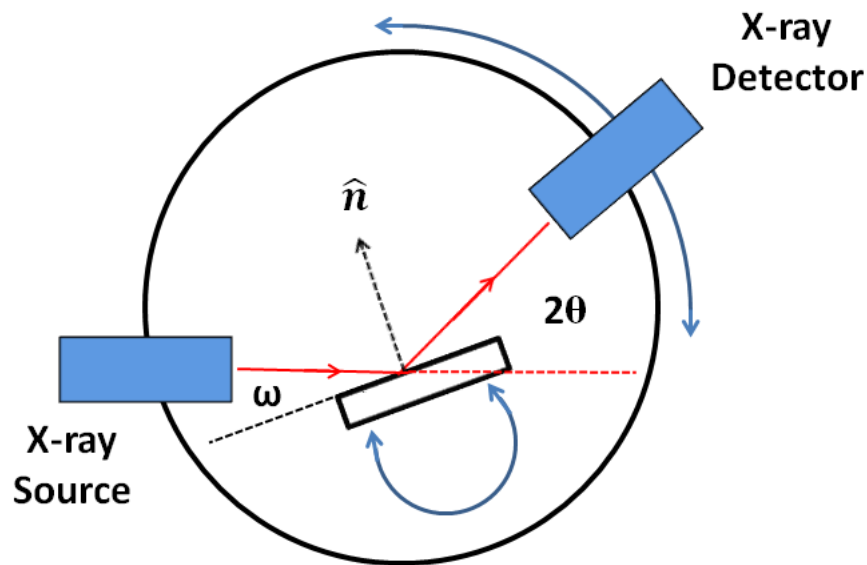
Figure 3-9 A schematic diagram of an XRD experimental set-up. The sample and detector angles are variable with the X-ray source in a fixed position. The angles between the sample plane and the incident angle is denoted 'ω', whereas the angle between the diffracted beam and the path of the beam if it was not affected by the sample is denoted '2θ'.

RSMs allow for the determination of both the in-plane and out-of-plane lattice parameter, for this coupled scans along a symmetric and asymmetric plane are required, in silicon these are commonly the (004) and (224) reflections respectively. Collecting sufficient data for a RSM is time intensive. While a single rocking curve can be obtained in under an hour, obtaining an RSM can require over 24 hours. This long measurement time is due to the low diffracted flux and the need to scan point or strip detectors slowly. 2D detectors can be used with more intense X-ray beams, such as at a synchrotron, but typically have a lower angular resolution. From a RSM one can determine the individual layer lattice parameters, the strain states individual epitaxial layers [114], (group IV) binary alloy composition, layer tilts and degree of crystallinity as indicated by the Bragg peak full-width-half-maximum (FWHM).

An XRD rocking curve is obtained by aligning to a particular crystal lattice plane and then scanning over a range of incident angles, with both ω and 2θ varying in a

coupled manner. An RSM can be constructed by obtaining multiple rocking curves, with initial ω value varied for each scan, in the vicinity of a known Bragg reflection of a material, typically the substrate, to map the area in reciprocal space of the sample under investigation [114,115].

3.5.6 Anton Paar DHS1100

In addition to the standard X-ray diffractometer sample stage, the Anton Paar DHS1100 domed temperature controlled stage, which is capable of heating samples up to 1100 °C, was also used during this work. The sample temperature is measured by a NiCr-Ni thermocouple underneath the sample mount. The temperature is measured with an accuracy of 1 °C. Sample temperature ramping was limited to a maximum of 5 °C/min. The sample is held in place by metallic clips, Figure 3-10. During a measurement the sample is covered by a graphite dome, Figure 3-11, which covers the sample without significantly attenuating the X-ray beam. The stage allows XRD measurements to be obtained *in-situ* with sample heating. Many standard annealing methods only allow measurements to be obtained *ex-situ* of either the as-

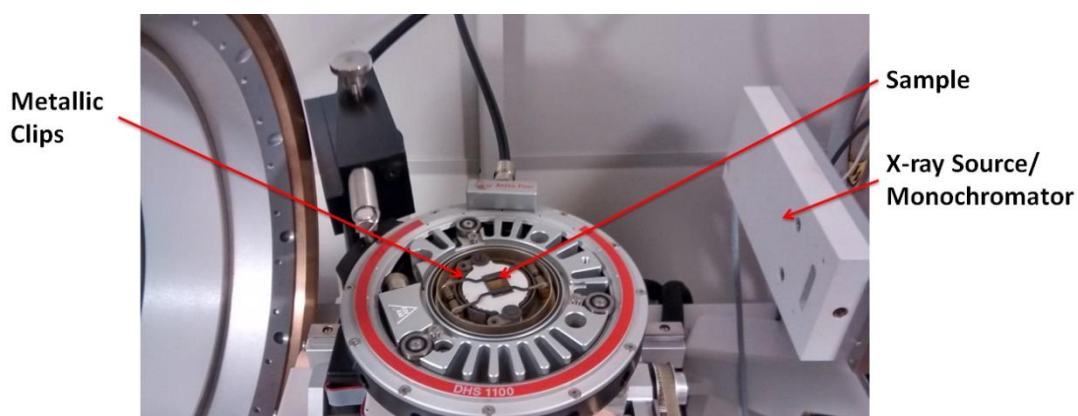Figure 3-10 Sample mounting for Anton Paar temperature controlled stage. The ~1 × 2 cm sample is held in place by metal clips on the stage above the thermocouple (shown). A graphite dome is then attached in place over the sample, shown in Figure 3-11.

grown material or after thermal treatments; this stage facilitates the additional observation the behaviour of material properties at multiple temperatures of the same sample. In this work, all measurements using the Anton Paar temperature controlled stage used a sample environment of air.
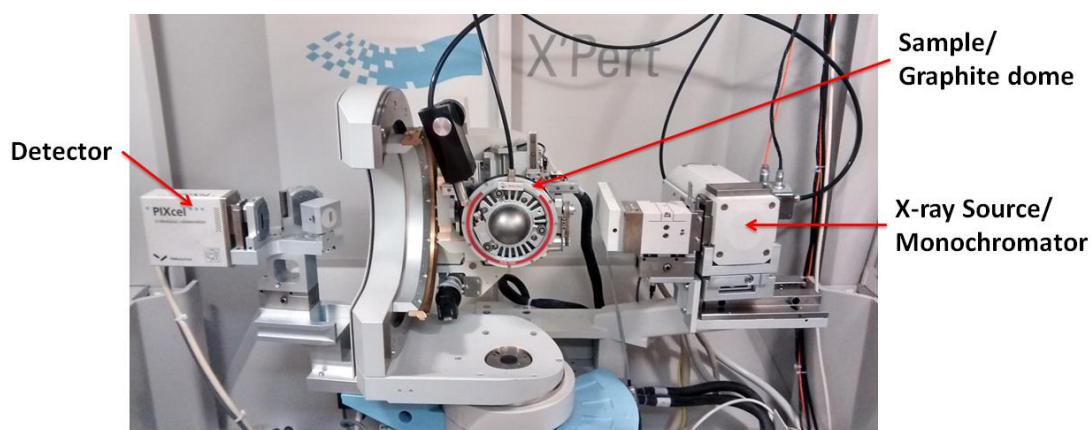
3.5.7 Measurement Attributes

Figure 3-11 The Panalytical X'Pert Pro MRD diffractometer configured with the Anton Paar DHS1100 with the domed graphite cover temperature controlled stage. A compressed air supply is used for sample cooling.

XRD provides a range of quantitate information of sample attributes and is a non-destructive method. The Bragg peak width infers crystal quality, and the Bragg peak position gives the presence of crystal layers. Group IV binary alloy composition can be determined by XRD if the appropriate modified Vegard's law is known, as with $Ge_{1-x}Sn_x$ binary alloys. However, ternary group IV alloys cannot have a unique composition determined by XRD. The thickness of strained layers can be determined, if "thickness fringes" are observed, but the layer thickness of strain relaxed layers cannot be determined. The *in-situ* thermal treatments with XRD measurements allow for the effect of changes of temperature on $Ge_{1-x}Sn_x$ alloy layer composition and crystallinity to be determined. Standard XRD does however struggle to characterize small 3D features, and relies on some foreknowledge of the

sample composition and structure and for low crystallinity samples it cannot determine the nature of the loss of crystallinity.

3.6 Synchrotron Based X-ray Diffraction

Synchrotron X-ray sources function by accelerating electrons with variable electric fields in a large circle, avoiding the limiting factors of lab based sources. Synchrotrons produce an extremely high intensity beam of X-ray radiation, and the wavelength can be selected. X-ray beam optics are used to select a narrow band of monochromatic beam with a small beamspot.

Synchrotron facilities allow for extremely high intensity beams, several orders of magnitude greater than possible with lab sources, to be achieved. This allows some measurements which normally require a significant scan time to be done in comparatively short time, which can facilitate the ability to examine time dependant phenomena not possible with lower intensity sources [116].

However, the high beam intensity can cause significant sample heating, which can be mitigated by sample cooling [81]. Despite this cooling, the high beam intensity increases the probability of beam damage to the sample compared to standard lab based diffractometers.

Though not part of this work, these incredibly intense beams facilitate the use of Fresnel lens and other methods of producing very small beam width, ~1 μm, allowing the isolation of signal from sample features on a micro and sub-micron scale [117].

As the X-ray beam wavelength is not limited to metal target emission lines, users can freely and reliably alter the x-ray photon energy such that x-rays can be used in techniques other than diffraction, such as X-ray absorption spectroscopy (XAS) and

extended X-ray absorption fine structure (EXAFS) which can probe the local bonding structure around specific species of atoms [118,119]. Though synchrotrons have many advantages over standard lab diffractometers, synchrotron facilities are very expensive to construct and maintain thus users typically have a limited measurement time.

For this work the synchrotron used was the Diamond Light Source, near Didcot, Oxfordshire, UK. This is a 3rd generation Synchrotron, with a 3 GeV electron beam (medium energy). Specifically, beamline I16 was used.

3.6.1 Sample Mounting and Temperature Control

During Synchrotron measurements the sample temperature was controlled by a high temperature cryostat, capable of producing sample temperatures of 20 K to 700 K. The cryostat was attached to a 6-circle kappa goniometer. The cryostat cryogen and vacuum shields each had a beryllium dome at the base, where the sample was mounted, as beryllium is a low atomic number element the X-ray beam transmits through with minimal attenuation, shown in Figure 3-13. The detector used was a 2-dimensional 100K 172×172 μm pixel detector. A standard focus setup was used, with an X-ray beam spot size of 30×200 μm, therefore results will be an average of this sample area. As samples are homogeneous at this scale, such averaging is reasonable.

The sample environment during measurement was a vacuum, ~10^{-6} mbar. A second shield was used to maintain a vacuum between itself and the first to provide thermal insulation from the environment, Figure 3-13.

Figure 3-12 A GeSn/Ge/Si sample mounted on copper stub via silver paste and mounted onto the high temperature cryostat sample cradle. To the right is the X-ray beam source, to the left is the flight tube to the detector.

Samples of $Ge_{1-x}Sn_x$/Ge/Si were cleaved ~1×1 cm squares which were mounted via a thermally conductive adhesive silver paste onto a copper stub. Prior to mounting in the cryostat the sample and stubs were cured at 100 °C for 1 hr, this is to ensure the adhesive stability of the silver paste and prevent out-gassing. After curing, the copper stub was mounted on the temperature controlled cryostat sample stage, as shown in Figure 3-12.

During each experiment run the sample was first cooled down to the base temperature of ~20 K. This cooling is to minimize the temperature of the cryostat cold head, which requires protection from high temperatures. Several temperature sensors were used to determine sample temperature *in-situ*.

Figure 3-13 The high temperature cryostat with (left) the inner cryogen shield mounted, to contain the cryogen (right) the outer vacuum shield mounted, which is used to maintain a vacuum for thermal insulation.

3.6.2 Measurement Attributes

In synchrotron XRD experiments, a huge quantity of information are gathered very quickly, all of the information that is attainable in lab based sources, discussed in the previous section, can be obtained but significantly more rapidly due to the much higher beam brilliance. However, available measurement time is limited and requires applying in months advance, thus such experiments are not ideal for quick turn-around between experiment design and execution. This diffraction method still cannot be used to directly measure layer thickness. Because of the wide range of experiments conducted at synchrotrons, and because each beamline set-up is unique, and each experiment produces potentially huge amounts of data, the data analysis itself is not standardized, increasing its complexity and time intensity. Figure 3-14 shows an unprocessed tiff image with a Bragg peak visible, this is the raw data from which the synchrotron results are extracted.

3.7 Transmission Electron Microscopy

As previously stated, imaging structures requires that the radiation have a wavelength on a similar scale to the features which are to be observed. Therefore, for nanometre scale features this makes visible light microscopy unsuitable, X-rays can be used for diffraction experiments but are not suitable for imaging. Transmission Electron Microscopy (TEM) is a commonly used method for imaging nanoscale structures, where imaging is achieved with monochromatic beams of electrons with a
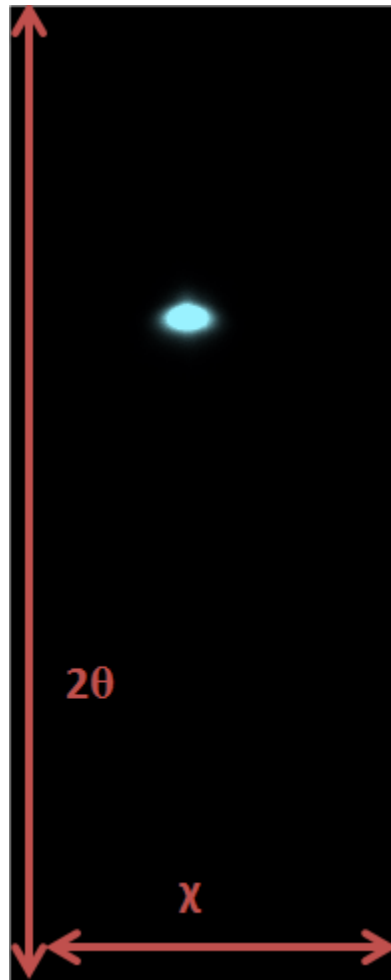

Figure 3-14 Unprocessed tiff image from Pilatus detector showing (004) peak from a GeSn epilayer. The vertical axis is in the 2θ direction and the horizontal axis in the χ direction.

de Broglie wavelength sufficiently small such that the features of interest are observable.

In this work cross-sectional TEM (X-TEM) imaging is used to determine $Ge_{1-x}Sn_x$ epilayer and Ge buffer layer thicknesses; to obtain qualitative information of the crystal quality by determining if the epilayer material is monocrystalline, polycrystalline or amorphous; determine the type, location and prevalence of lattice defects including differentiating between edge and threading dislocations which can be identified by inspection. TEM is a commonly used characterization method in materials science as it provides a wealth of knowledge about a material.

3.7.1 Theory

The minimum feature size resolvable by electrons is limited by the de Broglie wavelength used for imaging, which is proportional to the energy of the electron as given by equation 3-5 the general de Broglie wavelength, equation 3-6 the de Broglie wavelength for electrons. In TEM the electrons are accelerated to relativistic velocities, and this must be taken into account, as done in equation 3-7.

$$\lambda = \frac{h}{p} = \frac{h}{mv} \qquad\qquad 3\text{-}5$$

$$\lambda = \frac{h}{\sqrt{2m_0 eV}} \qquad\qquad 3\text{-}6$$

$$\lambda = \frac{h}{\sqrt{2m_0 eV\left(1 + \frac{eV}{2m_0 c^2}\right)}} \qquad\qquad 3\text{-}7$$

Where λ is the electron de Broglie wavelength, V is the accelerating voltage, h is Plank's constant, m_0 is the electron rest mass, e is the electron charge and c is the speed of light. For example, electrons subjected to a 200 kV accelerating voltage will

have a wavelength of 0.0025 nm, which is smaller than the features to be investigated in this work.

Unlike lab based X-ray wavelengths, which is limited to the emission lines of metal targets, in TEM the wavelength of electron beam used as a probe can be chosen simply by controlling the accelerating voltage, 200 kV is standard for imaging semiconductors. This value is a compromise, while a higher accelerating voltage decreases the electron wavelength, the increased electron kinetic energy can produce significant damage to samples. While lower electron beam energies, and hence larger wavelengths, do not facilitate as high resolution.

For many electron microscopes any additional resolution facilitated by using acceleration voltages above 200 kV cannot be utilised due to aberrations to the electron beam. Beam aberrations are caused by imperfect electron sources and imperfect electron lenses and reduce the attained image resolution. A schematic diagram of a transmission electron microscope is shown in Figure 3-15. The microscope requires many electron lenses and thus aberrations from each lens accumulate contributing to a corrupted, i.e. lower resolution, image. For particularly sensitive samples, such as many biological samples, lower accelerating voltages of 120 keV or 80 keV are commonly used in order to reduce sample damage from the electron beam, at the cost of attainable resolution. The theory and practice of TEM measurements is covered in detail in Williams and Carter, Ref. [120].

X-TEM observations are made through a cross-sectional volume of material, which must be thinned to be transparent to the electrons, as discussed below. All TEM in this work uses the JEOL JEM-2000 FX operating at 200 kV, unless otherwise stated.

Electron Source

Condenser Lens

Condenser Aperture

Sample

Objective Lens

Objective Aperture

Back Focal Plane

Diffraction Aperture
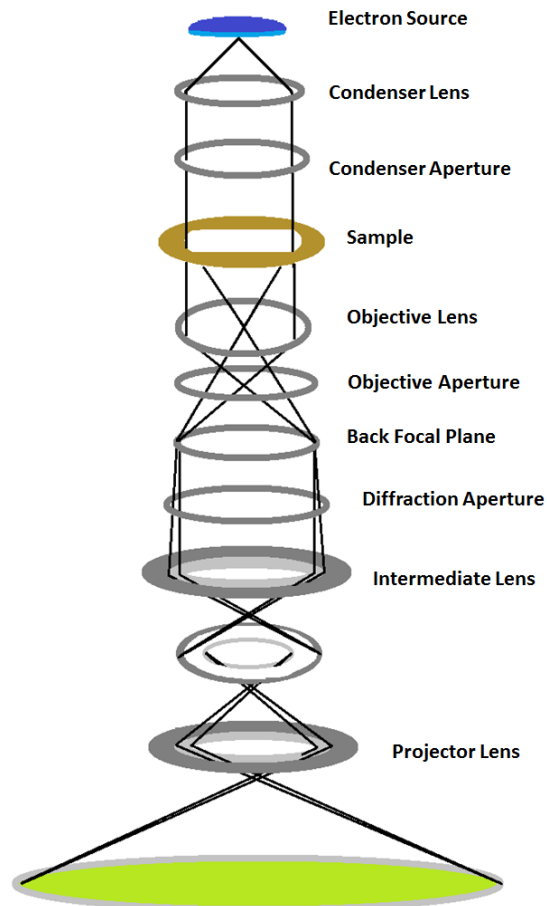
Intermediate Lens

Projector Lens

Figure 3-15 A schematic diagram of the configuration of transmission electron microscope, with series of electron lenses, with their purpose and also marked is the path of the electron beam. The electron source produces high velocity electrons, which are condensed, transmitted through the sample, focused and then either directly projected onto a CCD or phosphorus screen for either imaging or diffraction pattern.
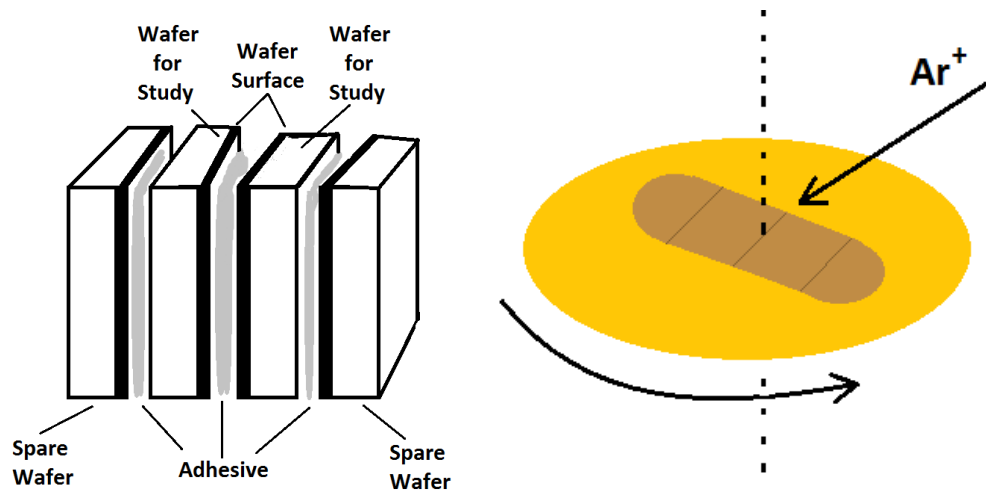
3.7.2 Sample Preparation

Figure 3-16 - Schematic diagrams of the stages in sample preparation for TEM. (left) Initial gluing of 'sandwich' surfaces together completed bar structure. Subsequently the bar is cut with a diamond saw, the sample is then attached to metal block, ground and then polished. Finally a TEM copper support ring glued to the sample surface. (right) Precision ion polishing system beaming process, with argon ions used to thin the central interface between the samples.

In this work TEM samples were prepared by the 'lapping' method, rather than using a focused ion beam. For this method wafers are cleaved to produce two approximate 1×1 cm squares. The surface is cleaned with acetone, then a thin layer of adhesive is spread across the surface, and the two pressed together. Both 'backs' of the sample are cleaned with acetone and a ~1×1 cm square of plain silicon wafer coated with adhesive is pressed to the back of the sample, as shown in left of Figure 3-16. The complete wafer bar is compressed as the adhesive sets. Once the adhesive sets, the structure is sawn in half to produce a cross-section, one half is attached to a metal block and then sanded down along the cross-section until transparent to red light. A copper ring is glued to the sample with the interface of interest at the centre of the ring. A precision ion polishing system is then used to further thin the central interface with argon ions, as show in Figure 3-16.

Samples which cannot be prepared by this lapping method, for example if they are particularly hard such as SiC, or too delicate such as electrical devices, can be prepared for TEM by cutting a cross-section and attaching it to a copper TEM grid using a focused ion beam-scanning electron microscope (FIB-SEM). While this method can be used for materials unsuited to the standard preparation method, it is significantly more time consuming and can induce significant ion implantation damage to the surface of the sample under investigation.
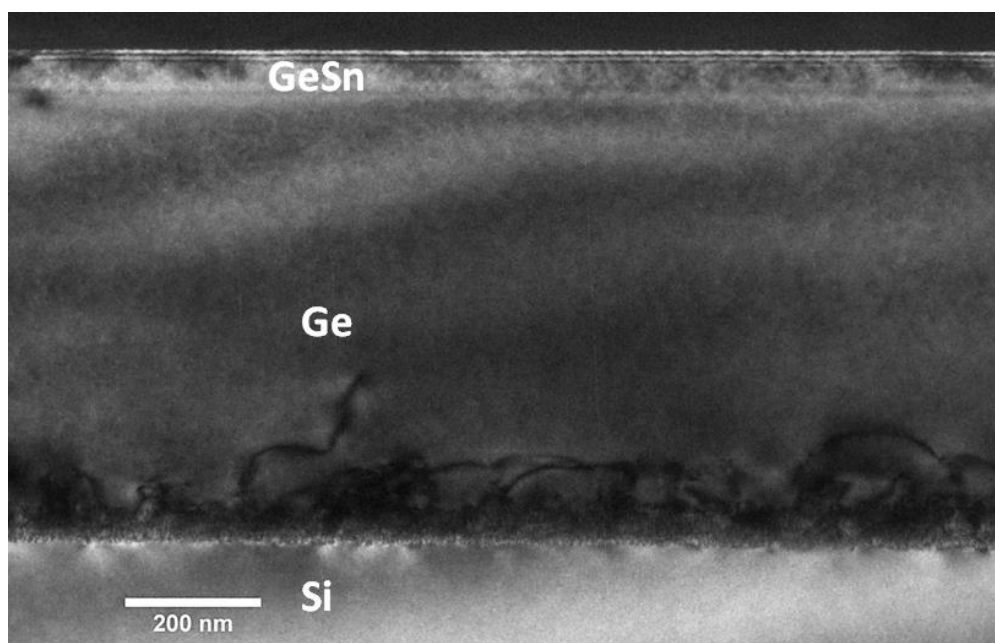
3.7.3 Imaging

Figure 3-17 A TEM image of a $Ge_{1-x}Sn_x$/Ge/Si structure in the (220) dark field diffraction condition. The different layers have a different contrast. The interface between the Ge buffer and the Si substrate is visible and the lattice misfit dislocations. At interface the GeSn epilayer and Ge buffer no defects are visible.

In TEM imaging is achieved with the electron beam being projected after passing through the sample. The electrons are detected by a charge couple device (CCD) or phosphorus screen, traditionally photos were obtained using photographic film, but this has become less common. Image contrast comes from the detected electron

intensity. Changes in image contrast occur in part due to the dependence on the material atomic number, allowing images to have rudimentary elemental contrast. The thickness of material also effects the contrast, with a hole in the samples giving a very bright signal and a thick sample appearing dark. A TEM image of a GeSn/Ge/Si structure is shown in Figure 3-17, each layer has a different contrast, the slightly undulating pattern of light and dark contrast is a thickness effect of the sample.

3.7.4 Imaging in a Diffraction Condition

When studying crystalline materials in TEM, a diffraction lens can be used to produce a diffraction pattern, containing 'Kikuchi lines' from many lattice planes [120]. In diffraction contrast imaging the sample is tilted to align on a particular lattice plane. An aperture is used to select a section of the beam from a particular diffraction condition, excluding signal from other contributions, including the straight through beam. This aperture increases the relative contrast of sample features under investigation. By aligning onto a particular lattice plane, particular sample attributes are emphasised. With Si(001) samples it is common to use to (004) and (220) to determine epilayer thickness with strong compositional contrast, and also to examine the prevalence of lattice dislocations, respectively.

3.7.5 Measurement Attributes

TEM is a commonly used characterization technique due to its versatility. It can be used to determine layer thickness, relative crystal quality, prevalence of alloy segregation, and any major surface features. An indication of alloy composition can be inferred from the contrast of layers, though with little accuracy other than the difference between layers. In this work TEM is the sole method able to identify lattice defects – the defect type, location in the heterostructure and the approximate

defect concentration. For TEM measurements, the sample is consumed during preparation and this process is time consuming.

3.8 Raman Spectroscopy

Raman spectroscopy is a materials characterization method which can be used to analyse thin films close to surfaces of solid samples, either crystalline or amorphous, and can also be used to characterize liquids or solutions of samples. Raman spectroscopy can be used to determine the composition of a heterostructure by observing the Raman-activated vibrational mode frequencies. Further information such as the alloy composition and lattice strain can be determined. Raman spectroscopy measurements can be obtained quickly, and it is a non-destructive characterization technique.

For a Raman spectroscopy measurement, a monochromatic light source (typically a laser) is incident on the sample surface. Of the photons which are scattered, the majority are elastically scattered, i.e. Rayleigh scattered; however, a minority of the incident photons will interact with polarizability of the electron density (the "electron
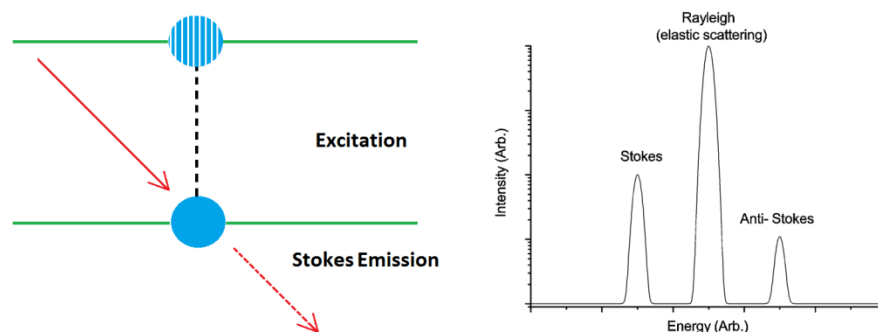
Figure 3-18 (left) Schematic diagram of the excitation of vibrational modes and the subsequent emission of a photon contrbuting to the Stokes signal. (right) The relatice intensities of Stokes, Rayleigh and anti-Stokes emissions, plotted on a logarithmic scale. Stokes emission is significantly less intense than Rayleigh, which must be filtered for analysis of the Stokes signal.

cloud") around a molecular bond near the sample surface. The interaction will induce the transfer of energy from the photon to excite the vibrational-rotational bond into a virtual energy state. The degree of the energy transfer is characteristic of the material and bond and the shift in the energy of the inelastically scattered photons compared to the incident photons is the "Raman shift". The Raman shift can be used to identify the atomic species and bond type of the sample material close to the surface of solid samples. The inelastically scattered photons which lose energy form the Stokes signal, shown in Figure 3-18. Some incident photons will interact with pre-existing excited states and will gain energy by the relaxation of the vibrational mode to the ground state. The detectable signal from Raman spectroscopy is limited to sample material close to the surface, constrained by the depth which the incident laser photons can penetrate into the material, interact with the sample and then the scattered signal reach the sample surface to be detected without subsequent scattering events.

Raman spectroscopy can be used to determine the approximate composition of the sample surface, from the observed Raman shift of any Stokes signals observed. The relative intensity of the different elements can be used to indicate the relative compositions at the surface, through use of a standard sample for comparison.

The incident photon wavelength from the laser must be tailored such that the energy is appropriate for exciting relevant modes in the sample material and penetration depth is suitable.

In this work Raman spectroscopy measurements were performed at the University of Warwick, using the Renishaw inVia Reflex Raman Microscope, shown in Figure 3-19, fitted with a 633 nm HeNe laser source the most appropriate energy for $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$ epilayers [121]. The penetration depth of 633 nm laser is ~80 nm in pure Ge, with the penetration depth decreasing with increasing Sn fraction in $Ge_{1-x}Sn_x$ [45]. The detector energy resolution was approximately 1 cm^{-1}. Raman spectroscopy was used to confirm the incorporation of Sn into the lattice of binary $Ge_{1-x}Sn_x$ alloys and the incorporation of Si and Sn in ternary $Si_yGe_{1-x-y}Sn_x$ alloys. In $Ge_{1-x}Sn_x$ alloy epilayers the shift of the Ge-Ge peak from ~300 cm^{-1} to lower values with increasing Sn fraction, but to higher values with increasing compressive strain, for strain free epitaxial layers the Raman shifts as given in equation 3-8 [6,34].

$$\Delta\omega(x) = -72x \quad cm^{-1}$$
<div align="right">3-8</div>

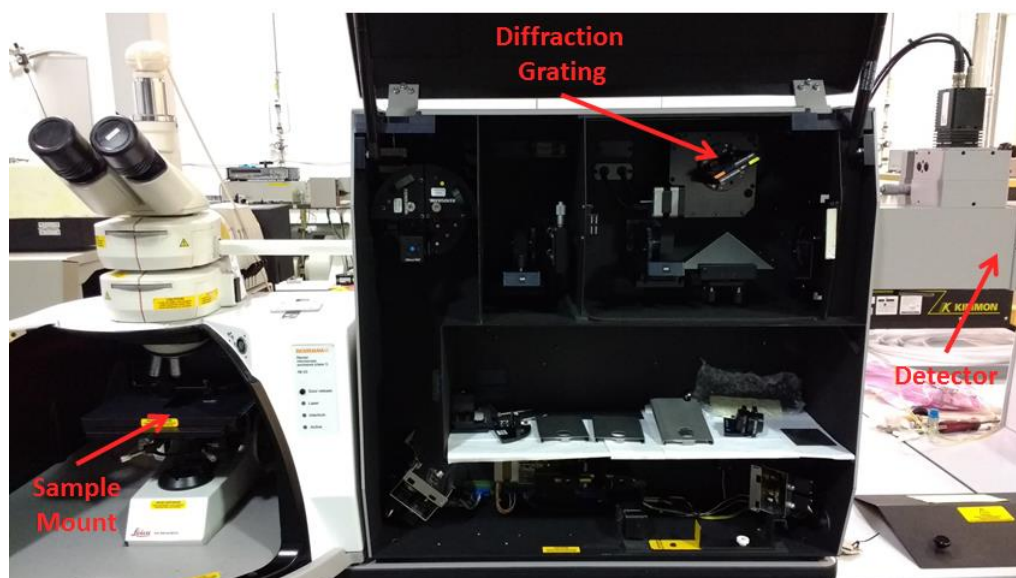Where 'x' is the Sn fraction and 'ω' is the Raman shift.

Figure 3-19 The Raman spectroscopy measurement configuration. Laser source is input from an external source, optics used to direct it onto the sample surface, with the reflected signal passed to a diffraction grating then onto the detector.
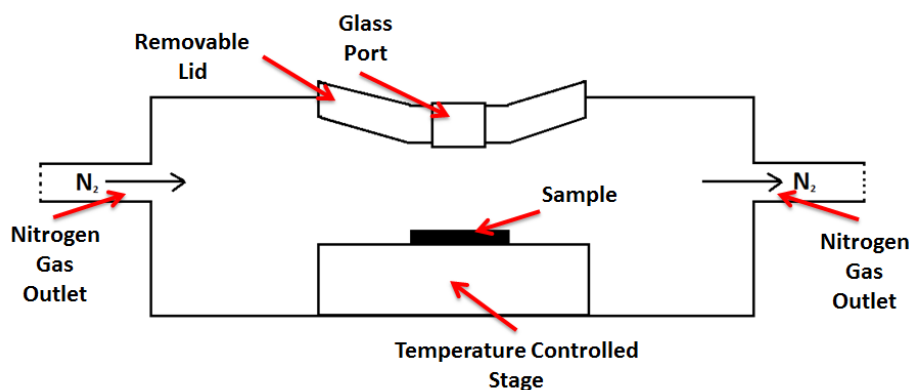
Figure 3-20 A schematic diagram of the Linkam THMS600 stage for Raman spectroscopy. The temperature controlled sample mount is cooled by an underflow of liquid nitrogen and heated by an internal heater. The sample atmosphere is kept dry with pure nitrogen gas to limit water ice formation.

3.8.1 Low Temperature Raman Spectroscopy

Higher thermal energy of the sample broadens the Raman peak, due to the increased spread of existing energy in the lattice vibration; increasing the uncertainty of peak location and neighbouring Raman peaks of a similar Raman shift can merge, such that two peaks will be incorrectly identified as a single peak.

To mitigate thermal effects, in this work a Linkam THMS600 temperature controlled stage, capable of maintaining temperatures in the range 77-873 K, was utilised for selected low temperature Raman spectroscopy measurements. For a measurement the sample is mounted on the sample stage, which is cooled to the target temperature by liquid nitrogen flow within the sample mount and heated with an internal electrical heater, shown schematically in Figure 3-20. The temperature is controlled by a temperature controller, accurate to ±0.1 K. The sample chamber is a nitrogen environment, preventing water ice crystal formation on the sample surface, which can generate additional Raman peaks which would complicate analysis and reduce

laser penetration into the sample. The laser reaches the sample via a window above the sample stage, shown in photos of the stage in Figure 3-21.
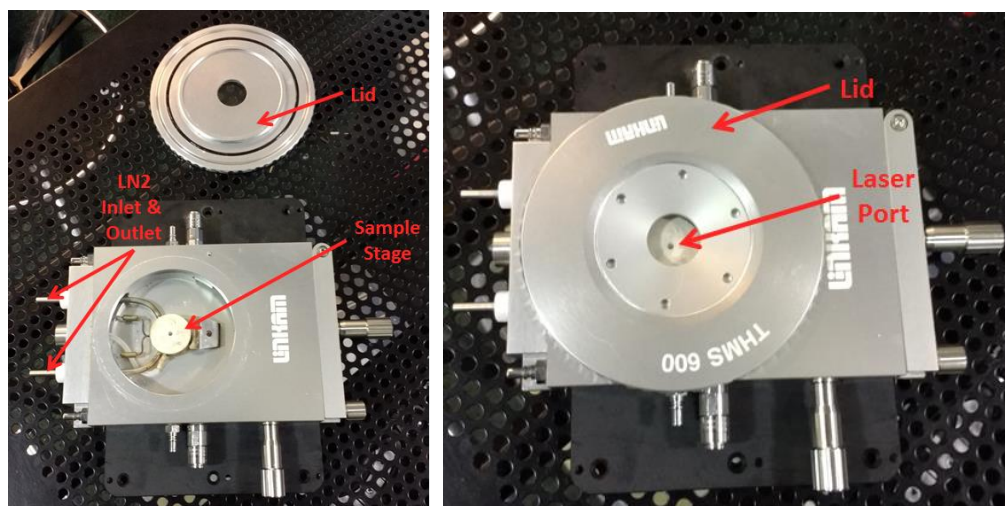

Figure 3-21 Photographs of Linkam low temperature stage (left) without lid, and (right) with lid attached. The sample mount is cooled by a flow of liquid nitrogen and nitrogen boil off is used to provide an inert and low humidity atmosphere.

3.8.2 Measurement attributes

Raman spectroscopy is able to measure the composition of the sample surface, and for a sample with a known and constant composition the lattice strain can be determined or mapped [49]. However, determining strain degree requires a known alloy composition, and even though the relation between strain and Raman shift is linear, the linear coefficient may be composition dependant [122,123]. Additionally, the laser penetration depth varies with $Ge_{1-x}Sn_x$ epilayer composition and for thin layers some signal will be contributed from underlying Ge buffer, which increases the error in composition for thin layers. Consequently unique alloy compositions cannot be identified solely from Raman measurements unless the layer sufficiently thick and fully relaxed. The incident laser beam can cause sample damage by localised heating, but this is typically not an issue with semiconductor samples as the

substrate can absorb much of the thermal energy. The energy resolution of detectors is also an issue with Raman measurements, with standard XRD facilities providing a more accurate lattice parameter and hence binary alloy composition and lattice strain than Raman. Raman can confirm the incorporation of atomic species in the epilayer and, unlike XRD, can provide information of the local bonding. If alloy composition is known, the incident laser can be focused to a small spot size in micro-Raman which can be used to probe changes on a micron scale, including sized features such as nanodots and nanowires [96,124].

3.9 Linear and Circular Transmission Lines

Linear and circular transmission lines were used in order to determine the characteristics of a range of electrical contacts.

Linear transmission lines consist of rectangular metal contact pads of constant dimensions fabricated at intervals with varied spacing, as shown in Figure 3-22. CTLM lines are similar to TLMs, but with circular rather than rectangular contact pads, in increasingly spaced concentric circles. The devices in this work had contact separations from 2 to 512 μm with intermediate values being powers of 2.

Current-Voltage (I-V) measurements are obtained at each contact separation distance, from which the electrical resistance can be extracted and contact type (Schottky, Ohmic). At smaller contact separations the resistance of the contact dominates the overall behaviour, at longer contact separations material resistance dominates. The contact separation is plotted against determined electrical resistance. By extrapolating to the resistance at zero separation, a value for the contact resistance can be obtained.
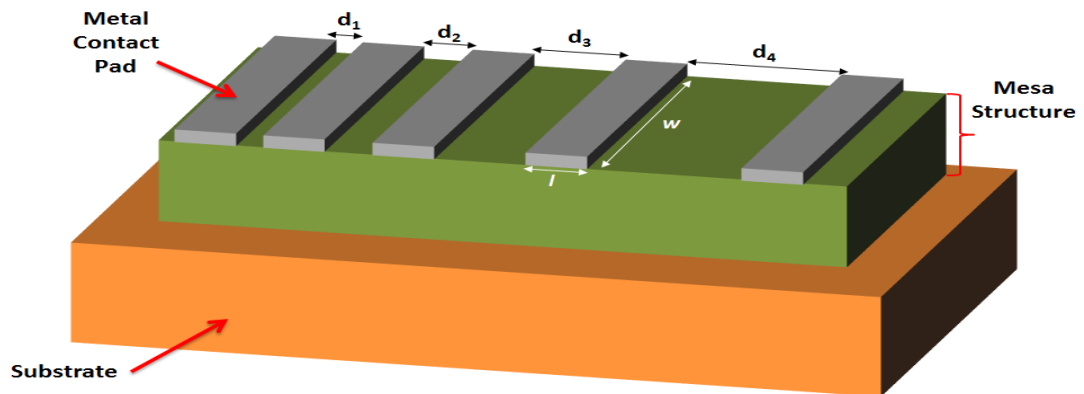

Figure 3-22 Schematic diagram of the TLM structure. The metal contact pads are of constant dimensions (thickness, width w and lenglth l) at increasing seperation between contacts ($d_1 < d_2 < d_3$). The mesa structure consists of the GeSn epilayer, the Ge buffer and some of the Si substrate.

3.9.1 TLM and CTLM Device Fabrication

The device processing steps are shown in the series of diagrams in Figure 3-23. Prior to any device fabrication, the sample surface is cleaned to remove any surface contaminates. With silicon-germanium materials surface cleaning is performed with dilute HF acid, however the chemical sensitivity of $Ge_{1-x}Sn_x$ alloys makes HF acid too aggressive. Therefore $\sim 1 \times 2$ cm sections of $Ge_{1-x}Sn_x$ epilayer samples are cleaned by being immersed in warm acetone and vibrated in an ultrasonic bath, then removed and dried with nitrogen gas.

Subsequently 'primer' is pooled onto the sample surface then dried with nitrogen gas, this step aids in ensuring any surface contamination is removed. A negative photoresist (AZ5124E) is then pooled onto the sample surface until completely covered. The sample is spun at high speed to produce a thin uniform coating of the photoresist, then heated (baked) on a hot plate for ~1 minute.

A glass plate which has been patterned with chrome with front contact mask, is cleaned with acetone. The mask is then aligned to sample, with the TLM lines orientated along the crystal planes. The mask is brought into physical contact with the sample surface. Physical contact is necessary to obtain the best possible definition of the mask features onto the sample. The sample surface is exposed to UV light for ~1 sec. Longer exposures can facilitate higher definitions, allowing for smaller contact separations, but can lead to the degradation of the contact pads.

After the front contact mask exposure the sample is baked for a second time, using similar conditions the bake. The entire sample, without any mask, is then exposed to UV for ~10 seconds. The sample is then submerged into a wet chemical developer for 1 minute, which removes any photoresist which has not exposed to UV.

The sample is then transferred to an electron-beam evaporator. The evaporator sputters a target material in a vacuum-like environment, in this work the metal for the electrical contact pads, the sputtered material then coats sample with an even coating with a deposition thickness which is controllable with a fairly high precision. After metal deposition, the sample is immersed in warm acetone and vibrated in an ultrasonic bath for ~1 min. This removes any metal deposited on the surface not in the area defined by the contact mask. The sample is then rinsed in deionized water and dried with nitrogen gas.

The contacts pads have now been fabricated, to produce the mesa structure additional processing steps are undertaken. The sample is again cleaned with the primer, dried with nitrogen gas and then a positive photoresist is pooled onto the sample surface and spun for a thin, homogeneous coating and then the sample is baked for several minutes on a hot plate.

The sample is then mounted into the mask aligner and a glass plate patterned mesa mask loaded. The mesa mask completely shadows each individual device, the metal contacts and the uncoated sample between contacts, but leaves material between the devices exposed. The mask is aligned onto features previously made and the sample is exposed to the UV source. The sample is then immersed in a chemical developer for ~1 minute then rinsed in DI water and dried with nitrogen gas, leaving the photoresist covering only the areas of the sample which are not to be exposed to UV light.

The sample is then loaded into the resistive ion etcher, where a radio-frequency pulsed plasma is used to etch the sample surface. The devices, which are covered by several microns of photoresist, are protected from the plasma and are not damaged by the process. The uncoated sample material between the devices is etched by the plasma down to the substrate, removing the $Ge_{1-x}Sn_x$ epilayer and Ge buffer. The samples are then cleaned in acetone, removing the remaining photoresist, and then rinsed in DI water and dried with nitrogen gas.

The height of the mesa is measured with a profilometer to ensure that sufficient material has been etched to completely remove the epilayer and buffer layer in order to electrically isolate each individual device.
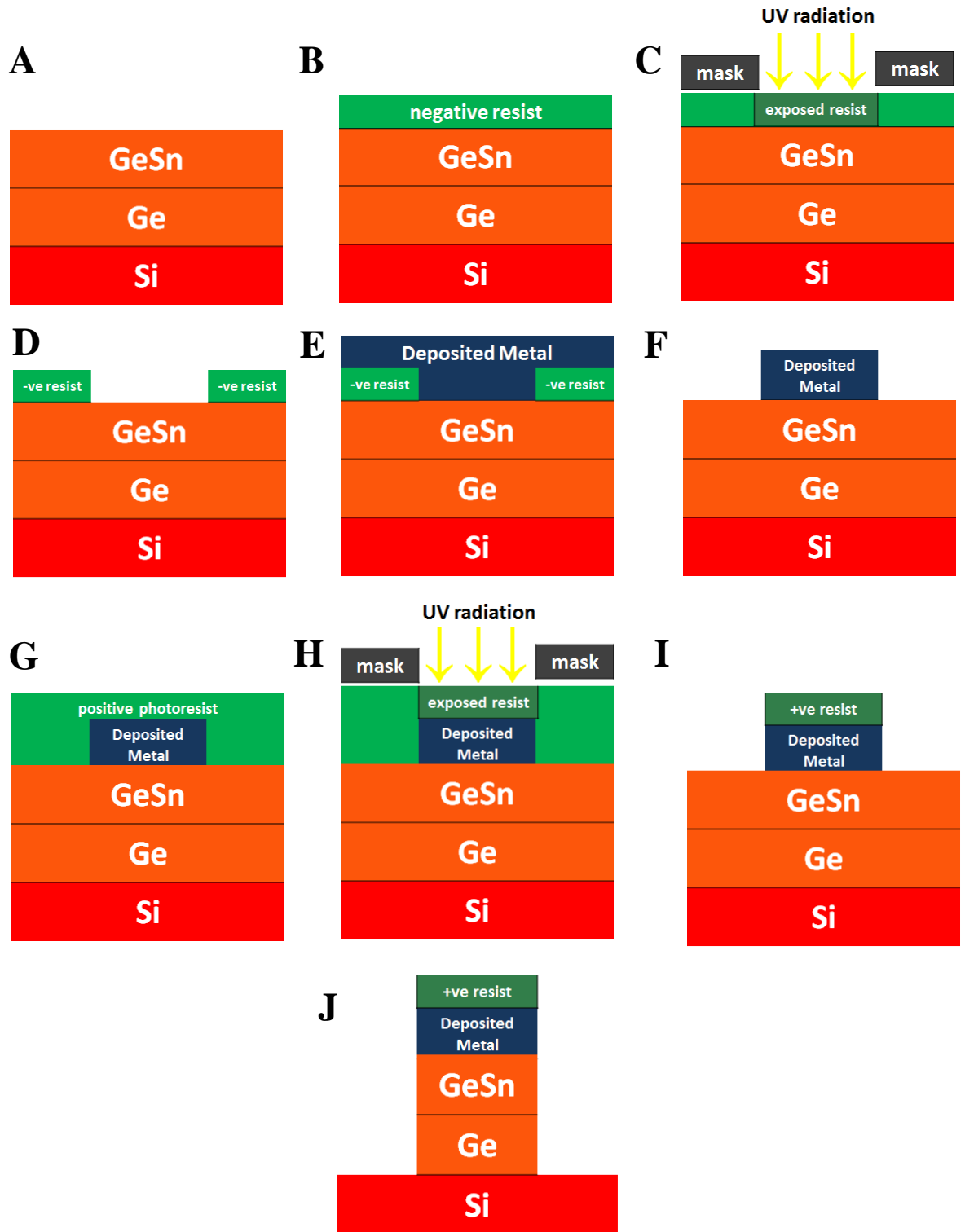
Figure 3-23 TLM device fabrication steps. A) Clean structure B) Spin coat negative resist C) Pattern front contacts D) Develop photoresist E) E-beam deposition of contact metal F) Lift off excess metal in acetone bath G) Spin coat positive resist H) Pattern mesa structure I) Develop mesa structure J) Etch away material between devices

3.10 Electrical Measurements

Depositing metal contacts directly onto a semiconductor surface typically results in a potential barrier and non-linear behaviour due to the formation of a Schottky contacts, with a rectifying non-linear behaviour as the bandstructure of the two materials do not align. Ohmic contacts, which have a linear response, can be formed by heavily doping the underlying semiconductors and by annealing the metal/semiconductor structure.

The formation of Ohmic contacts to $Ge_{1-x}Sn_x$ epilayers has previously been investigated, with publications examining a range of contact metals. Much of the previous research uses post-deposition thermal annealing to treat the electrical contacts, however the use of high temperature anneal processes for low Sn fraction alloy epilayers may not be transferable to higher Sn fraction epilayers [70]. For example, nickel has been used to form quality electrical contacts to GeSn layers, but requires high temperature treatments to form a Ni-GeSn alloy [125]. In this work we are investigating electrical measurements on a wide range of epilayer compositions, using both as-deposited metal electrical contacts and using lower annealing temperatures than examined in published works.

In order to test the quality of the electrical contacts it is necessary to conduct electrical measurements, in this work I-V scans were measured between neighbouring metal contacts. Details of using I-V scans from TLM devices on semiconductor samples is explained in depth is ref. [126]. At low contact separations the contact resistance dominates the measured resistance such that $R_{measured} \approx 2R_c$ (the factor 2 from the two contacts involved in the measurement). At larger contact separations the semiconductor resistance dominates, such that $R_{measured} \approx R_{semiconductor}$. For a homogeneous semiconductor the resistance would scale with contact

separation, thus a linear plot is expected between measured resistance and contact separation, intercepting the y-axis at twice the contact resistance.

Two point measurements were used for the I-V scans. Tungsten or beryllium-copper (BuCu) needles were used to contact the metal contacts. In an individual measurement the same type of needle was used to ensure it was symmetric.

In this work a Karl Suss PM5 probe station was used to control the needles, shown in Figure 3-24, and the Agilent 5146C Precision semiconductor parameter analyser was used as the conduct the I-V sweep.

The purpose of the electrical measurements is primarily to examine the characteristics of the electrical contacts but also to obtain data on the electrical properties of the semiconductor material. A broad understanding electrical properties of the material is useful to ensure that forming the electrical contact and subsequent thermal treatments have not caused severe damage to the material.

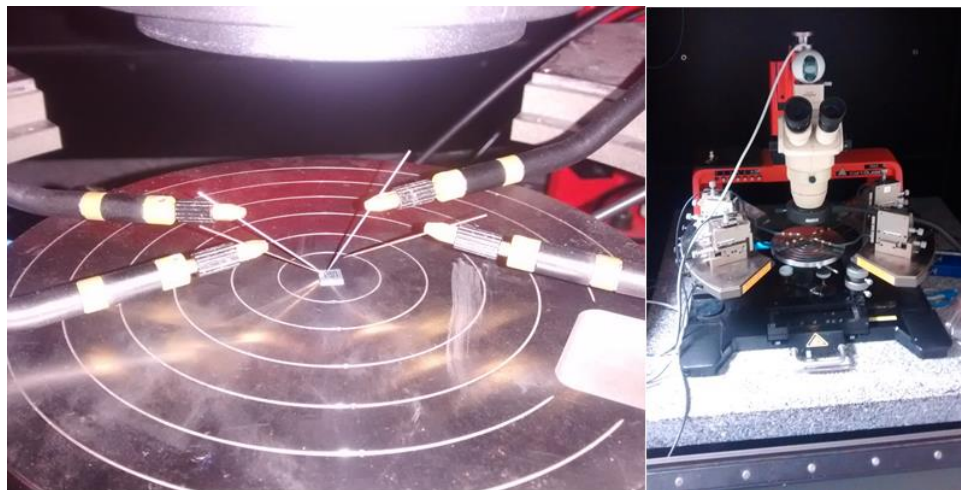During a measurement the metal probes are lowered to contact two neighbouring

Figure 3-24 Photographs of the a Karl Suss PM5 probe station. (Left) Needles and arms making contact to a device. (right) The stage, needle arms with translational controls and sample stage. The probe station itself is on a vibration dampening desk with a light excluding hood to prevent light induced excitation of charge carriers.

metal contacts on the TLM/CTLM surface. The electrical current is then varied and the resulting voltage between the probes determined at each current. Initially, a small current range is used to ensure the needle and metal contact pad have made physical contact while minimising the potential for current induced damage to the device. A larger current range is then used to acquire more detailed data.

3.11 Summary

The combination of the above characterization techniques allow for $Ge_{1-x}Sn_x$ alloy epitaxial layer composition, lattice strain state, thickness, crystal quality, surface roughness and features and the defect type and density between the epilayer and the Ge buffer, to be reliably and accurately measured. This allows the inter-relation of these material properties to be probed and the effect of growth conditions, thermal treatments and device properties to be identified. These properties are also used to identify any relations between the material properties and the electrical properties of TLM devices on these samples.

4 Germanium-Tin Epilayers Growth and Characterization

In this chapter materials characterization of strained and relaxed $Ge_{1-x}Sn_x$ epitaxial layers and related structures are explored. The samples investigated were produced by low temperature, 250 °C to 350 °C epitaxial growth of the $Ge_{1-x}Sn_x$ binary alloy onto Ge-buffered Si(001) substrates to form $Ge_{1-x}Sn_x$/Ge/Si structures. The material properties of the strained and relaxed $Ge_{1-x}Sn_x$ epilayers are determined using a variety of characterization methods to fully evaluate the material properties produced from a range of growth conditions.

Growth at 350 °C of pure Ge epitaxial layers on Si(001) substrates is calibrated, which is in the low growth temperature range necessary for $Ge_{1-x}Sn_x$ growth. The impact of varying several $Ge_{1-x}Sn_x$ epilayer growth parameters was investigated including varying growth temperature, growth duration, growth onto off-axis silicon substrates (via a Ge buffer) and varying the carrier gas used during growth. The effect on the $Ge_{1-x}Sn_x$ epilayer material properties due to modifying these growth conditions is compared.

4.1 Growth at Low Temperatures

Previous research indicates CVD growth temperatures equal to or less than 350 °C are necessary for incorporating Sn into the Ge lattice, with a lower growth temperature necessary in order to produce higher Sn fraction $Ge_{1-x}Sn_x$ alloys. In this work a growth temperature of 350 °C was used to produce $1 - 2$ at. % Sn alloys; the lowest growth temperature used was 250 °C, which produced up to 12 at. % Sn fraction alloys, in agreement with trends seen in previous publications.

At the University of Warwick a cold wall RP-CVD reactor is used for materials growth. RP-CVD is dominant growth method in industry and therefore developments in this work are more easily transferable. Cold wall CVD reactors raise the temperature of just the growth substrate, with the temperature controlled tightly, minimising material deposition on the chamber walls reducing the build-up of contaminates, and reducing gas consumption.

In CVD growth the carrier gas is a vital attribute, the gas ensures good mixing of the precursors and can play an intermediate role in growth mechanisms. Previous work has examined the use of H_2 and N_2 carrier gases with the Ge_2H_6 precursor gas used in this work as the Ge source, in order to determine whether the change in carrier gas affects the rate limiting step in the growth mechanism [103]. In this present work, H_2 was the predominant carrier gas used to grow $Ge_{1-x}Sn_x$ epilayers, and a comparative study using N_2 was also conducted.

4.2 Materials Characterisation of GeSn/Ge/Si structures

A variety of characterization methods have been used to evaluate the $Ge_{1-x}Sn_x$ epilayer samples in this work.

4.2.1 Characterisation of GeSn/Ge/Si by XRD

X-ray diffraction is a common materials characterisation method due to its low cost, non-destructive nature and the wealth of material information that can be obtained, as explained in chapter 3. Prior to an XRD measurement the sample is aligned to the Si substrate Bragg peak of the sample from the chosen lattice plane, the Si substrate is assumed to be fully relaxed.
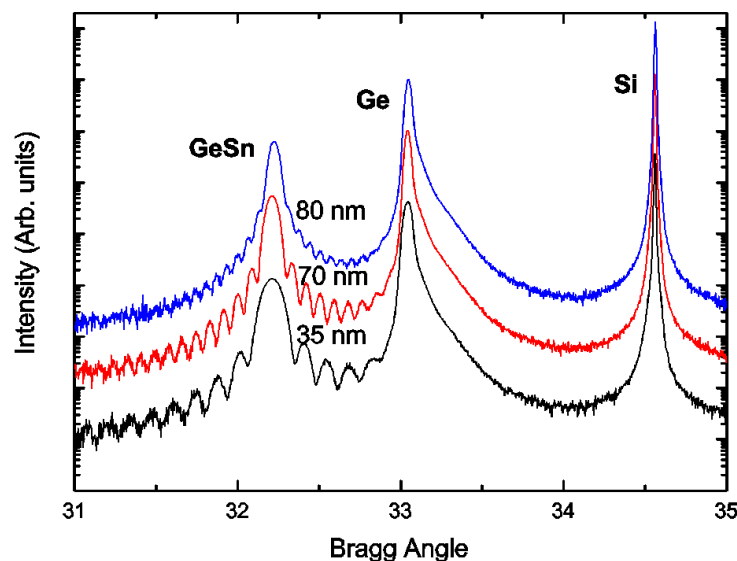
Figure 4-1 XRD rocking curve scans around the symmetric (004) Bragg peak for $Ge_{0.91}Sn_{0.09}$/Ge/Si(001) layers with epilayer thickness of 35 nm (black), 70 nm (red) and 80 nm (blue). Note the spacing between thickness fringes decreases with increasing thickness. The 35 nm and 70 nm epilayers are both fully strained, however the 80 nm epilayer has undergone slight lattice relaxation, this leads to a loss of intensity of the thickness fringes. Scans are offset for clarity and plotted on a logarithmic scale.
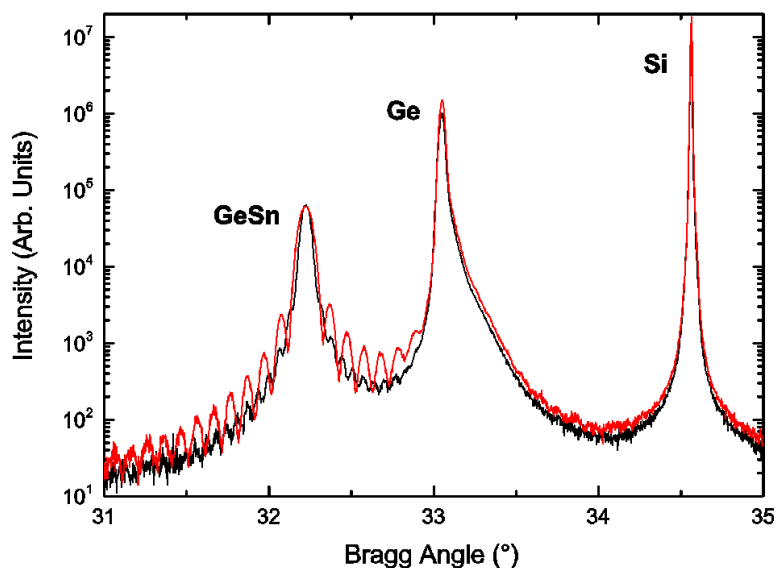

Figure 4-2 XRD rocking curve around the symmetric (004) Bragg peak for 80 nm thick 5.7% partially relaxed $Ge_{0.908}Sn_{0.092}$ epilayer sample (black) and 50 nm thick fully strained $Ge_{0.908}Sn_{0.092}$ epilayer sample (red). As the partially relaxed $Ge_{0.908}Sn_{0.092}$ epliayer relaxation is only slight, the epilayer Bragg peak is not shifted significantly to higher angles and thickness fringes are still observable – though the fringes are significantly reduced in amplitude compared to the fully strained epilayer. Intensity is plotted on a logarithmic scale.

Figure 4-1 shows XRD (004) rocking curves of three $Ge_{0.91}Sn_{0.09}$/Ge/Si structures where the $Ge_{0.91}Sn_{0.09}$ epilayer thickness is varied, but the epilayer remains fully strained in all samples. Note increasing the epilayer thickness decreases the observed separation between the 'thickness fringes' either side of the Bragg peak, but does not impact the Bragg peak position. All other things being equal, increasing the epilayer thickness also increases Bragg peak intensity, by increasing the diffraction volume. However, the Bragg peak intensity is also influenced by other factors such as degree of crystallinity. The Bragg peaks from the Ge buffer, ~33°, and the Si substrate, ~34.5°, are significantly more intense than the $Ge_{1-x}Sn_x$ Bragg peak as they make up a much greater proportion of the diffraction volume.

Figure 4-2 shows XRD (004) rocking curves of a partially relaxed epilayer $Ge_{0.908}Sn_{0.092}$/Ge/Si sample and a fully strained epilayer $Ge_{0.908}Sn_{0.092}$/Ge/Si sample. Note that the relaxation of the partially relaxed $Ge_{0.908}Sn_{0.092}$ epilayer is slight, only 5.7% relaxation relative to the Ge buffer. In the plot the Bragg peaks from the two epilayers have the same Bragg angle, as do the Bragg peaks for the Ge buffer and Si substrate. The significant effect of the slight epilayer relaxation is the dramatic decrease in intensity of the $Ge_{1-x}Sn_x$ Bragg peak thickness fringes. The relaxed epilayer Bragg peak is not observed to shift relative to the fully strained layer due to the lattice parameter only being altered by a very small degree by the lattice strain relaxation. The observed decrease in intensity of the thickness fringes is due to the lattice relaxation being achieved by the formation of misfit dislocations at the $Ge_{1-x}Sn_x$/Ge interface, which reduces the interface quality which in turn reduces the coherent reflection of x-rays from the $Ge_{1-x}Sn_x$/Ge interface which contributes to form the thickness fringes.

Figure 4-3 shows XRD (004) rocking curves from the $Ge_{0.884}Sn_{0.116}$/Ge/Si sample with a partially strain relaxed epilayer and a $Ge_{0.896}Sn_{0.104}$/Ge/Si sample with a fully strained epilayer for comparison. With this more significant degree of strain relaxation of the $Ge_{0.884}Sn_{0.116}$ epilayer than in the previous example, 14.7% relative to the Ge buffer, the thickness fringes around the $Ge_{0.884}Sn_{0.116}$ Bragg peak are no longer observable. Despite the $Ge_{0.884}Sn_{0.116}$ relaxed layer having a slightly higher Sn fraction than the stained epilayer sample, the relaxed epilayer Bragg peak has shifted to a higher Bragg angle. This shift of the epilayer Bragg peak is due to the relaxation of compressive strain in-plane leading to a reduction of the epilayer out-of-plane lattice parameter i.e. the epilayer lattice relaxation shifts the lattice closer to a cubic symmetry.

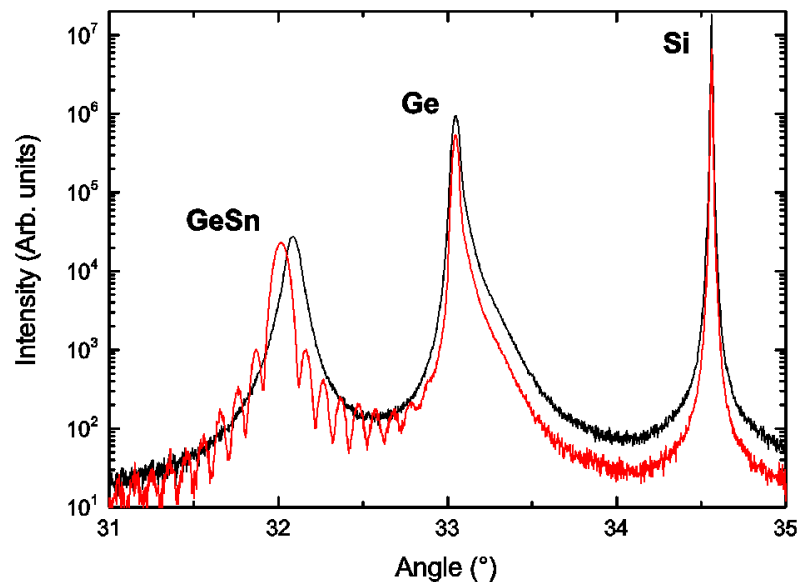The effect on varying the $Ge_{1-x}Sn_x$ epilayer composition on XRD (004) rocking

Figure 4-3 XRD Rocking curve around the symmetric (004) Bragg peak for 90nm thick 14.7% relaxed $Ge_{0.893}Sn_{0.107}$ epilayer sample (black) and 40nm thick fully strained $Ge_{0.896}Sn_{0.104}$ epilayer sample (red). Note that the partially relaxed $Ge_{1-x}Sn_x$ epilayer has a higher Sn fraction, but the associated Bragg is at a higher Bragg angle in the (004) scan – this is due to the layer relaxation thus the out-of-plane lattice parameter decreases and the in-plane lattice parameter increases.

curves is shown in Figure 4-4. The black plot indicates a $Ge_{0.95}Sn_{0.05}$/Ge/Si sample, the red plot a $Ge_{0.91}Sn_{0.09}$/Ge/Si sample and the blue plot a $Ge_{0.894}Sn_{0.106}$/Ge/Si sample. The increasing Sn fraction of the $Ge_{1-x}Sn_x$ epilayer shifts the epilayer Bragg peak to lower Bragg angles, due to the increasing out-of-plane lattice parameter with increased alloy Sn fraction.
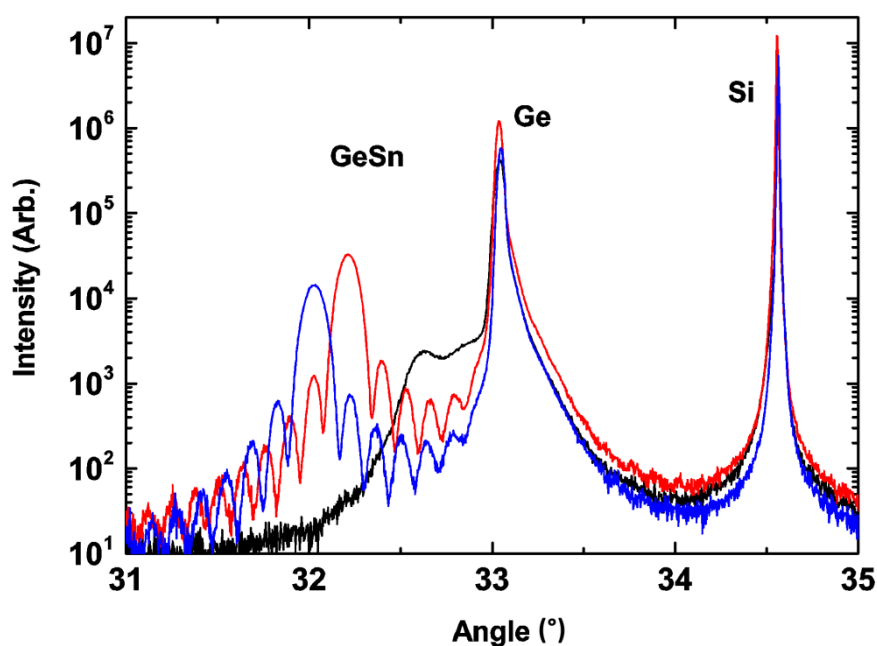

Figure 4-4 The (004) XRD rocking curves from $Ge_{1-x}Sn_x$/Ge/Si samples with a range of epilayer compositions. Plots from (black) 30 nm $Ge_{0.95}Sn_{0.05}$ epilayer (red) 40 nm $Ge_{0.91}Sn_{0.09}$ epilayer (blue) 40 nm $Ge_{0.894}Sn_{0.106}$ epilayer. Increasing the epilayer Sn fraction shifts the $Ge_{1-x}Sn_x$ Bragg peak to lower Bragg angles as the out-of-plane lattice parameter increases.

4.2.2 Surface Characterisation

The $Ge_{1-x}Sn_x$ epilayer surface was characterization by AFM, providing topological information such as average surface roughness, the nature of any surface features present and typical height variations.

A range of surface topologies are observed from the samples investigated in this work. In Figure 4-5 are AFM scans from a sample with a fairly smooth featureless

surface, from a pure Ge epilayer. Also shown are $Ge_{1-x}Sn_x$ epilayer samples with cross hatching, pits and crosshatching, pits and surface dots and a sample with only surface dots. A smooth featureless surface is optimal for a growth platform and indicates a high crystal quality. Crosshatching indicates dislocations, and thus epilayer relaxation. The pits in the sample surface are an indication selective etching of the surface. The surface dots indicate either island growth or alloy segregation.
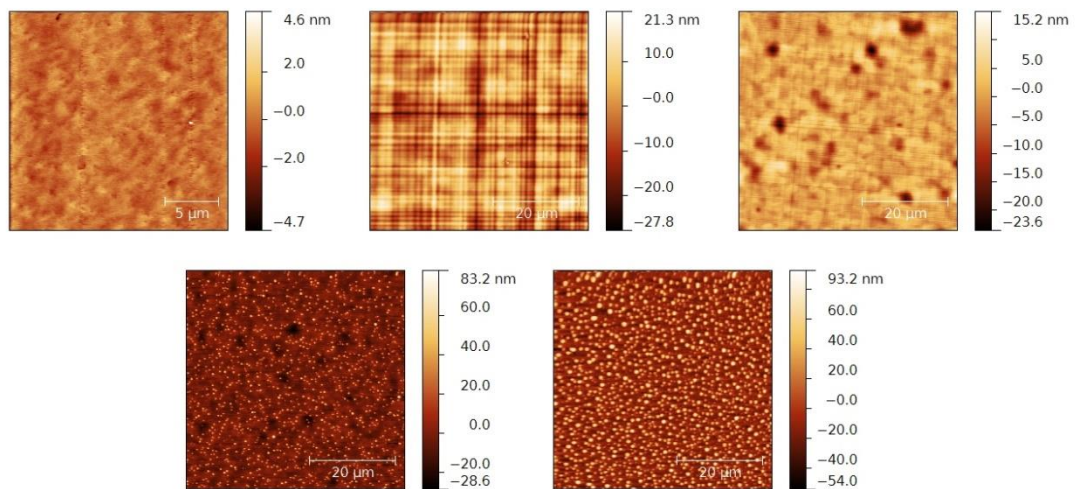

Figure 4-5 AFM scans from samples with a range of surface topologies. (top left) pure Ge surface, essentially featureless, roughness RMS = 0.5 nm. (top centre) cross hatching only, RMS = 7 nm (top right) Epilayer with pits and crosshatching, RMS = 3.3 nm (bottom left) surface pits and dots, RMS = 10 nm (bottom right) dots only, RMS = 20 nm

4.3 Calibration of Ge Grown at Low Temperature

To fully comprehend the growth characteristics of $Ge_{1-x}Sn_x$ alloys it is necessary first to calibrate the growth of pure Ge epitaxial layers at comparable low temperatures. For this work the growth temperatures chosen to study were 350 °C and 550 °C. This study of low temperature CVD growth of pure Ge is necessary in order to determine the effect of incorporating the Sn precursor into the growth process. Therefore the effect of the grown structure is decoupled from other significant growth factors. The

test of pure Ge growth allows the growth rate of the digermane precursor, which is not the standard for Ge epitaxial layers, to be tested and examine how this varies with temperature.

In this work three Ge samples were grown directly onto a cleaned Si (001) substrate at each temperature with varying growth times. With a 350 °C growth temperature, Ge was deposited for 5, 10 and 15 minutes; when using the higher growth temperature of 550 °C, Ge was deposited for 10, 20 and 30 minutes. Varying the Ge growth time at a constant temperature provides an indication of the material growth rate and growth dead-time. Growth dead-time arises as crystal growth does not initiate immediately from the input of precursor gases into the growth chamber, as a finite amount of time is needed for crystal growth to initiate. Dead-time can have a significant effect for very short deposition times, but has less impact for longer growth times that are used for producing thicker layers.
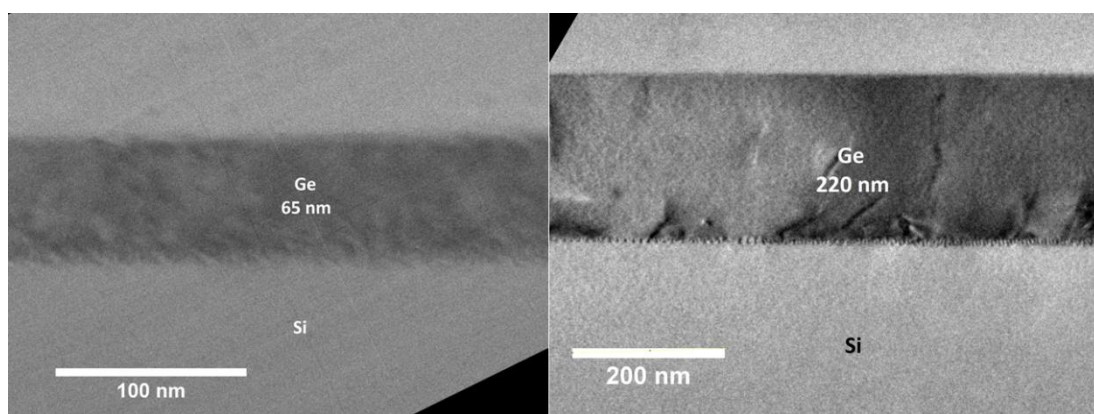

Figure 4-6 TEM images of Ge grown onto a Si substrate at different temperatures. (Left) Growth at 350 °C for 10 minutes producing a 65 nm Ge layer. Misfit dislocations are visible at the Ge/Si interface, which act to relieve strain due to the Si/Ge lattice mismatch. (Right) Growth at 550 °C for 10 minutes, producing a significantly thicker 220 nm Ge layer. Again, strain relieving lattice defects are visable in the Ge/Si interface and some in the Ge layer itself.

TEM was used to determine the Ge epilayer thickness, example images are shown in

Figure 4-6, and the Ge layer thickness of each sample was compared to growth time

to extract the growth rate, the plot shown in Figure 4-7. These results indicate a Ge

growth rate of 5.5 nm/min at 350 °C and 14 nm/min at 550 °C. For the growth

temperature of 350 °C the extrapolated thickness at zero time is 1.7 nm which is

sufficiently close to zero to be negligible, indicating the dead-time at 350 °C is

insignificant for the growth times used. For growth at 550 °C the extrapolated

thickness at a zero growth time is 70 nm, which is clearly unrealistic. This result

indicates growth in the first 10 minutes at 550 °C to be more rapid than subsequent

growth, with the growth rate later stabilizing at a lower rate. This suggests that Ge

growth on the cleaned Si substrate is faster than growth on the Ge epilayer during

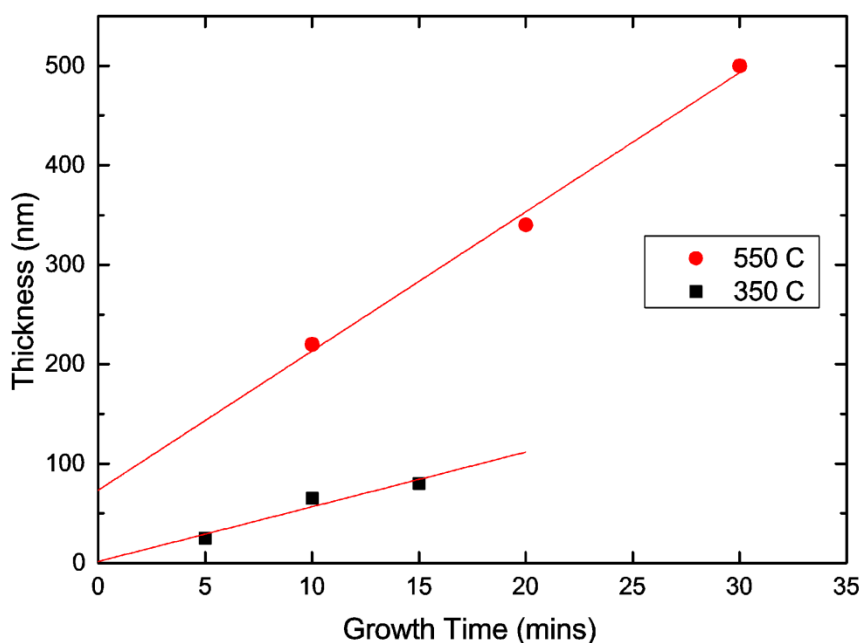growth, with a lower bound on the initial growth rate of 22 nm/min, and that as the

Figure 4-7 Ge epilayer thickness for a range of growth times with a growth temperature of (red) 350 °C and (black) 550 °C. At 350 °C the growth rate is 5.5 nm/min with an intercept of 1.7 nm. In contrast at the higher growth temperature, growth rate is significantly increased, at 550 °C the slope is 14 nm/min with an intercept of 73.3 nm.

Ge epilayer thickness increases the growth rate decreases and stabilizes in the range of growth times investigated at 14 nm/min.

The observation of a faster initial Ge growth while growing directly onto the Si substrate may be due to the deposition being onto a smoother growth platform. Subsequently, as the Ge epilayer thickness exceeds the critical thickness of relaxation during growth, the generation of strain relieving lattice defects and consequent surface roughening provides a less ideal growth platform for subsequent growth which reduces the growth rate.

4.4 Influence of Temperature on GeSn Growth

Following the preliminary work with Ge growth we now turn to the $Ge_{1-x}Sn_x$ layer. Previous work has demonstrated that decreasing the $Ge_{1-x}Sn_x$ growth temperature not only reduces the growth rate, but also increases the attainable Sn fraction [53]. The $Ge_{1-x}Sn_x$ alloy composition is also influenced by the precursor gas phase mixture composition, which must be controlled and tuned to account for the changes of the growth temperature. Increasing the growth rate at a constant growth temperature is believed to also increase the upper limit for the Sn fraction of $Ge_{1-x}Sn_x$ alloys, as segregation length decreases at higher growth rates [127]. Therefore, all other influences being equal, decreasing the $Ge_{1-x}Sn_x$ growth temperature has two competing effects, moving growth conditions further from equilibrium thus increasing the attainable Sn fraction, and decreasing the growth rate which decreases the attainable Sn fraction. During this work the $Ge_{1-x}Sn_x$ growth temperature was varied and the impact on the $Ge_{1-x}Sn_x$ alloy epitaxial layers determined.

At a growth temperature of 350 °C, which is approaching the upper temperature limit for growing $Ge_{1-x}Sn_x$ alloys using CVD seen in published work [9,14,69] the

produced epilayers have Sn fractions from 1 to 2 at. % Sn, with an epitaxial layer thickness between 150 nm and 300 nm, with all layers produced at this temperature being fully strained to the Ge buffer. While these Sn fractions exceed the equilibrium solubility of Sn into Ge, they are not significantly greater than the ~1 at. % limit. To investigate the effect of Sn incorporation into the Ge matrix, and indeed for the predicted properties which would be beneficial for devices to be exhibited, it is necessary to produce higher Sn fraction alloy layers. That being said, publications have demonstrated that $Ge_{1-x}Sn_x$ alloy layers with Sn low fractions demonstrate that even very low Sn fractions can improve the layer crystal quality compared to pure Ge grown under similar conditions [11,13].

By reducing the $Ge_{1-x}Sn_x$ growth temperature to 300 °C, the Sn fraction in the resulting epilayer was increased. Crystalline layers were produced with a composition of 5 - 6 at. % Sn and layer thicknesses from 100 nm to 170 nm. Epilayers grown at 300 °C were partially strain relaxed, relaxing 12 - 15% relative to the Ge buffer. These Sn fractions are several times higher than the equilibrium Sn fraction, indicating the growth conditions are sufficiently far from equilibrium to prevent alloy segregation. The Sn fraction of the alloy was varied within the 5 - 6 at. % Sn range by altering the Sn and Ge precursor ratio in the growth chamber. Epitaxial layers of $Ge_{1-x}Sn_x$ alloys with similar Sn fractions have been examined in other work in device applications, the attributes of Sn incorporation already providing improvements upon comparable devices using pure Ge [39,128].

By further reduction of the growth temperature to 270 °C, the attained Sn fraction was observed to increase beyond that obtained at 300 °C. The $Ge_{1-x}Sn_x$ epilayer Sn fraction ranged from 9 – 12 at. %. The epilayer thickness ranged from 50 nm to 90 nm. While a 50 nm $Ge_{0.91}Sn_{0.09}$ epilayer remained fully strained to the Ge buffer,

thicker $Ge_{1-x}Sn_x$ layers with higher Sn fractions underwent partial lattice strain relaxation. A maximum lattice relaxation was attained with a 90 nm $Ge_{0.884}Sn_{0.116}$ epilayer, which was 19% strain relaxed relative to the Ge buffer.

The absence of observed strain relaxation of the $Ge_{0.91}Sn_{0.09}$ epilayer may be attributed to the lower layer thickness and lower lattice mismatch with the Ge buffer compared to other samples produced at the same growth temperature. When examining the partially relaxed $Ge_{1-x}Sn_x$ layers produced at higher growth temperature, which have a lower Sn fraction and thus a lower lattice mismatch, it may not be immediately apparent why these have undergone relaxation when the $Ge_{0.91}Sn_{0.09}$ epilayer did not. We attribute this to two possible influences. Firstly, the partially relaxed $Ge_{1-x}Sn_x$ layers that are grown at 300 °C are thicker and, secondly, there is a greater temperature difference between their growth temperature and ambient than the $Ge_{0.91}Sn_{0.09}$ epilayer, increasing the effect of the thermal coefficient of contraction mismatch.

For the $Ge_{1-x}Sn_x$ epilayer samples grown at 270 °C, the variation in epilayer composition and thickness is controlled by altering the Sn and Ge precursor ratio. The Sn fraction achieved at this growth temperature is approaching the upper limit of high crystallinity $Ge_{1-x}Sn_x$ epilayers grown by CVD in the literature. The maximum epilayer lattice relaxation values are also observed to increase, despite the decrease in layer thickness compared to $Ge_{1-x}Sn_x$ layers grown at 300 °C. This can be attributed to the increase in lattice mismatch between the $Ge_{1-x}Sn_x$ epilayer and the Ge buffer from the increasing Sn fraction when growing at lower temperatures.

XRD rocking curves from a selection of samples grown at 350, 300 and 270 °C are shown in Figure 4-8.

In the 350 - 270 °C $Ge_{1-x}Sn_x$ growth temperature range examined so far, we have observed that Sn fraction increases as growth temperature decreases. However, this trend is not observed with the further reduction in growth temperature to 250 °C. At this reduced temperature the $Ge_{1-x}Sn_x$ alloy Sn fraction was not observed to increase further, but rather the Sn fraction becomes more erratic. A wide range of $Ge_{1-x}Sn_x$ Sn fractions are obtained at a 250 °C growth temperature, with Sn fractions up to 10.6 at. %, which is very close as the maximum Sn fraction for samples grown at 270 °C, with lower Sn fractions down to 5 at. %. The degree of epilayer relaxation is low, with a maximum relaxation of 6% relative to the Ge buffer. This may be due to the lower layer thicknesses or the reduced temperature difference between growth and ambient temperatures.

While further optimization of precursor flow rates and ratios may yield higher Sn fractions at 250 °C, with perhaps only a very small window of growth parameters which increase the alloy Sn fraction, such rigorous optimization has not been necessary with previous decreases in growth temperature and corresponding increases in alloy Sn fraction. This can possibly be attributed to the reduction in $Ge_{1-x}Sn_x$ growth rate due to the decrease in temperature from 270 to 250 °C having a greater impact on reducing the maximum alloy Sn fraction than the possible increase in alloy Sn fraction from growth conditions being further from equilibrium. The combined effect of these two influences leaves the upper limit of the Sn fraction unchanged with this reduction in growth temperature. If this is the cause further reductions in the growth temperature will not allow for greater Sn incorporation, and may lead to a degradation in materials growth.
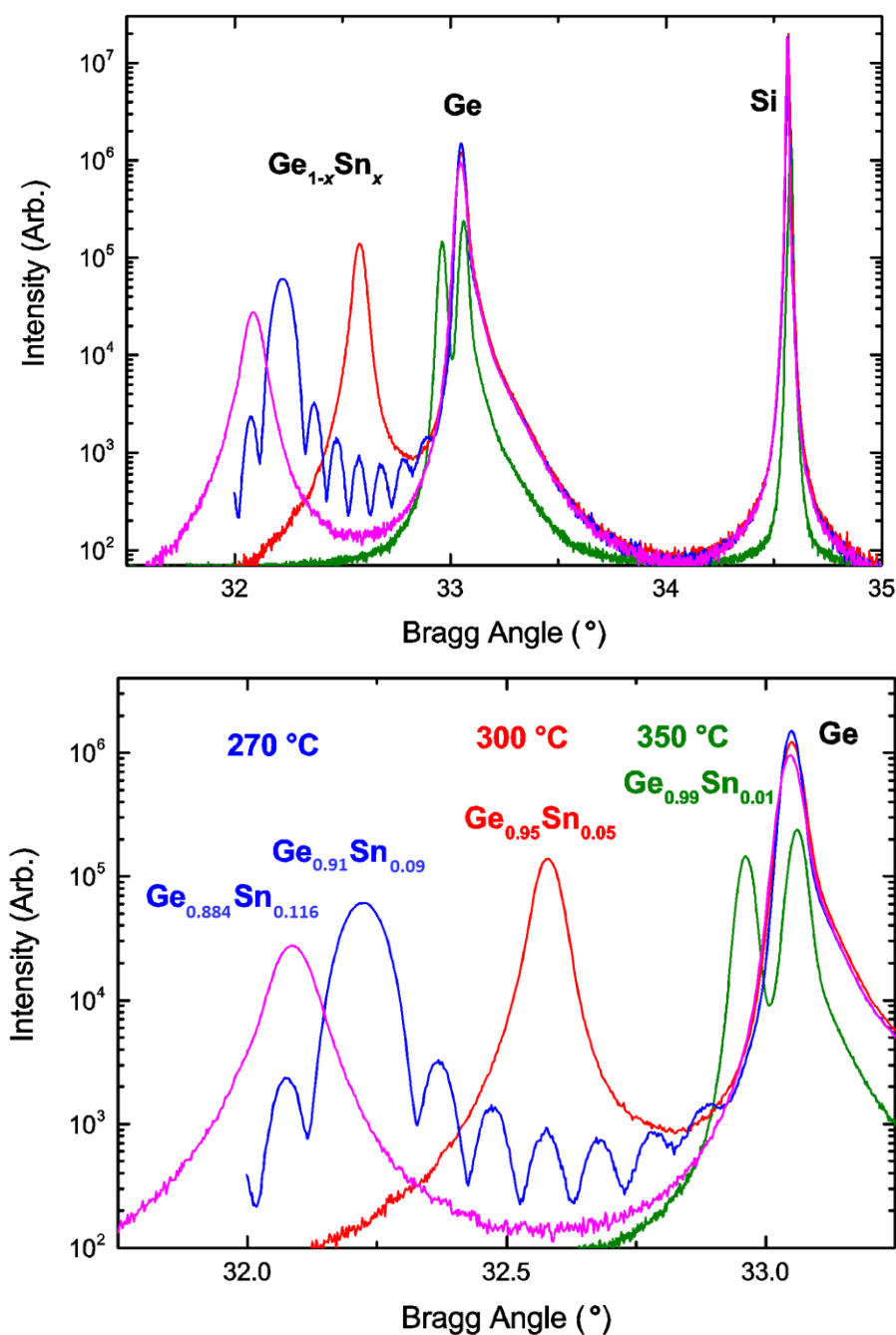
Figure 4-8 XRD (004) rocking curves from $Ge_{1-x}Sn_x$/Ge/Si samples grown at a range of growth temperatures. The trend of lower growth temperatures producing higher Sn fraction $Ge_{1-x}Sn_x$ epilayers is evident, though at low temperatures the alloy Sn fraction is also highly variable at the same growth temperature, indicating that precursor gas ratios, pressures, etc. play an increasingly important role. (Top) Broad spectrum from the samples. (Bottom) Rescaled spectrum to highlight the Ge buffer and $Ge_{1-x}Sn_x$ Bragg peaks.

Also of note the degree of strain relaxation of the $Ge_{1-x}Sn_x$ epilayers with $x \approx 0.1$

grown at 250 °C is much lower than strain relaxation of alloys of a comparable

composition grown at 270 °C, despite the epilayers grown at 250 °C being of a similar or even greater thickness. This may be attributed to the difference in lattice change upon sample cooling post growth, due to thermal contraction down to room temperature from growth temperature. Also, as stated previously, low temperature growth increases the critical thickness of relaxation by supressing misfit dislocation formation. Note that the difference in growth temperature is only ~10%, but has allowed for the same structure to be either fully strained or partially relaxed.

In addition to the effect of the growth temperature on the produced alloy Sn fraction, the epilayer thickness also decreases with decreasing growth temperature. This strong dependence of the growth rate on the growth temperature is indicative that the CVD growth in this study is operating in the kinetically limited growth regime, though this is not a major area of study of this work and further work would be necessary for confidence.

4.5 Carrier Gas

In this section the effect of the altering the carrier gas under otherwise identical growth conditions is examined. As previously discussed, the effect of carrier gas on growth warrants investigation as carrier gases can be a crucial intermediary during the growth process, will contribute to chamber pressure, and assist with good mixing of precursor gases in the chamber. Publications demonstrate that using N_2, as opposed to the more standard H_2 as the carrier gas under otherwise identical growth conditions, increases the Ge growth rate when using the Ge_2H_6 precursor at low temperatures [103]. This increase in growth rate is attributed to the growth surface being less hydrogen terminated with N_2 than H_2, increasing the density of active sites

which the Ge_2H_6 or fragments thereof can bond to, hence increasing the crystal growth rate.

However, the process of growing the alloy $Ge_{1-x}Sn_x$ is not the same as growing pure Ge. Although Ge_2H_6 is still a major contributor to the growth rate in Ge-rich $Ge_{1-x}Sn_x$, the addition of the Sn precursor, $SnCl_4$, alters the growth mechanism.

H₂ Carrier Gas			N₂ Carrier Gas		
Sample ID	GeSn Epilayer Thickness (nm)	Sn Fraction (at. %)	Sample ID	GeSn Epilayer Thickness (nm)	Sn Fraction (at. %)
A	40	10.6	D	0	-
B	35	10.6	E	0	-
C	110	10.6	F	0	-
G	50	8.6	J	30	5.0
H	55	8.0	K	35	8.5
I	75	6.0	L	0	-

Table 3 The layer thicknesses and composition of $Ge_{1-x}Sn_x$ layers grown under similar conditions with (left) H₂ carrier gas, and (right) N₂ carrier gas. Samples A – F were grown under similar conditions, expect for the change in carrier gas, likewise samples G – L were grown under similar conditions to each other.

From our investigation, the results of which are in Table 3, we consistently obtain a lower $Ge_{1-x}Sn_x$ layer thickness when using N₂ as the carrier gas as opposed to the more standard H₂ carrier gas. In a significant number of instances, no $Ge_{1-x}Sn_x$ epilayer growth is observed at all when using N₂ as the carrier gas. The reduction in thickness or absence of $Ge_{1-x}Sn_x$ indicates the growth rate is actually reduced when using the N₂ carrier gas.

Additionally, when $Ge_{1-x}Sn_x$ growth is achieved using the N₂ carrier gas, the $Ge_{1-x}Sn_x$ epilayers produced possess a different Sn fraction, in one instance half, compared to layers grown under otherwise similar conditions using the H₂ carrier gas. The decrease in Sn fraction may be attributed to the lower growth rate when

using N_2, as previously discussed it is believed that higher growth rates facilitate a higher upper limit to Sn fraction. At lower growth rates, Sn atoms are not 'locked in' to the layer as quickly by growth of overlayers, allowing Sn atoms to segregate to the growth surface, which inhibits further Sn incorporation.

In some instances of using the N_2 carrier gas, no $Ge_{1-x}Sn_x$ layer is grown at all on to the Ge buffer. This complete lack of $Ge_{1-x}Sn_x$ growth using N_2 carrier gas (in Table 3 samples D, E, F and L) was observed under equivalent conditions that with a H_2 carrier gas produced layers with both a particularly high Sn fraction, over ~10 at. %, and a more moderate Sn fraction, at 6 at. % (samples A, B, C, I). However, growth conditions which produced intermediate Sn fractions, ~9 at. %, when using the H_2 carrier gas are the conditions under which $Ge_{1-x}Sn_x$ layers are produced when using N_2. It is possible that different aspects of the extremes of growth conditions for the highest and lowest Sn fraction alloys inhibit $Ge_{1-x}Sn_x$ growth when using the N_2 carrier gas.

It is apparent that $Ge_{1-x}Sn_x$ growth conditions including growth temperature, precursor ratios, precursor flow rates, etc., used for successful growth when using the H_2 carrier gas are not necessarily suitable for growth when using the N_2. Thus attempts to replicate the growth of a target $Ge_{1-x}Sn_x$ layer characteristics when changing carrier gas would require the growth parameters to be completely re-calibrated. Additionally, the use of similar growth parameters has been observed to produce lower growth rates and in some cases layers with a lower Sn fraction compared to equivalent growth using H_2. From this study it is apparent that changing the carrier gas from H_2 to N_2 reduces that maximum Sn fraction attainable and also reduces the $Ge_{1-x}Sn_x$ growth rate without any observed benefits.

4.6 Fully-strained GeSn

In this work strained $Ge_{1-x}Sn_x$ epilayers grown onto Ge-buffered Si(001) substrates were investigated, the epilayers were produced at a range of growth temperatures, producing a wide range of Sn fractions and layer thicknesses. Fully strained epilayers are layers thin enough to not exceed the critical thickness of relaxation and are lattice matched to the Ge lattice. Strained layers are of interest due to their low defect density and the effects of bandstructure of lattice strain. All $Ge_{1-x}Sn_x$ layers investigated in this work are compressively strained, making the $Ge_{1-x}Sn_x$ bandgap L-Γ separation larger than a similar composition layer which is strain relaxed.

In the asymmetric XRD (224) RSM of strained epilayer samples, as example shown in Figure 4-9, the $Ge_{1-x}Sn_x$ epilayer Bragg peak is observed directly under the Ge peak, i.e. the epilayer and buffer have an identical q_x, indicating the epilayer real space in-plane lattice parameter is matched to the underlying Ge buffer. In the symmetric (004) RSM, example in Figure 4-9, the $Ge_{1-x}Sn_x$ epilayer Bragg peak is observed directly under the Ge Bragg peak, indicating that the epilayer is not tilted relative to the Ge-buffer. Note that the Ge buffer is under slight tensile strain due to the thermal coefficient mismatch between Ge and Si. In XRD rocking curves of strained epilayer samples, thickness fringes are observed in satellite positons either side of the $Ge_{1-x}Sn_x$ epilayer Bragg peak. The observation of thickness fringes indicates the epilayer surface is smooth and the epilayer/buffer interface has a low concentration of lattice defects.

A fully strained epilayer TEM image aligned along the (004) plan in dark field condition is shown in Figure 4-15. In this sample no strain relieving lattice dislocations are observable at the GeSn/Ge interface. The interface is observed as an uninterrupted straight continuous line, the epilayer surface is also smooth and there is no discernible Sn segregation.
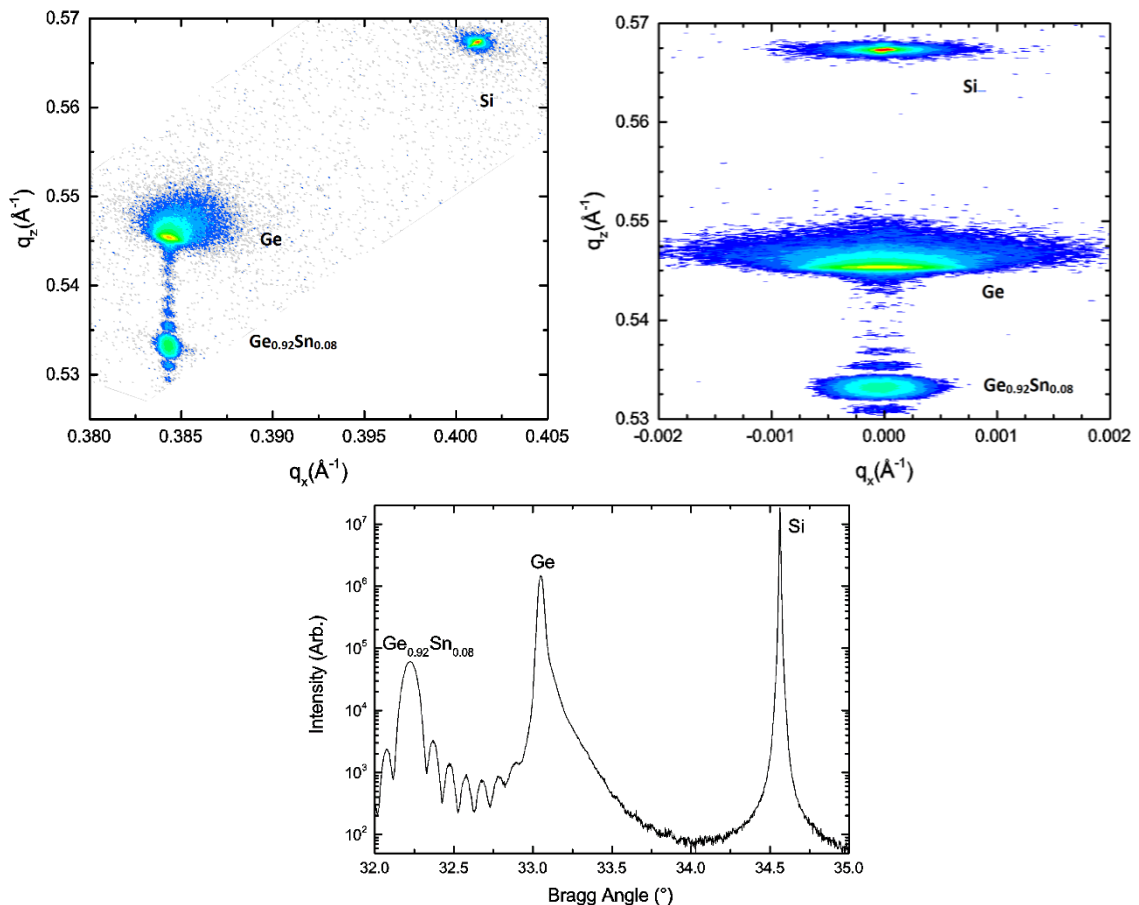

Figure 4-9 Various XRD scans from $Ge_{0.91}Sn_{0.09}$/Ge/Si (Upper left) Asymmetric (224) RSM, Note the GeSn peak is directly under the Ge peak and thickness fringes are visible. (Upper right) Symmetric (004) RSM (Lower centre) (004) Rocking curve, with strong thickness fringes.
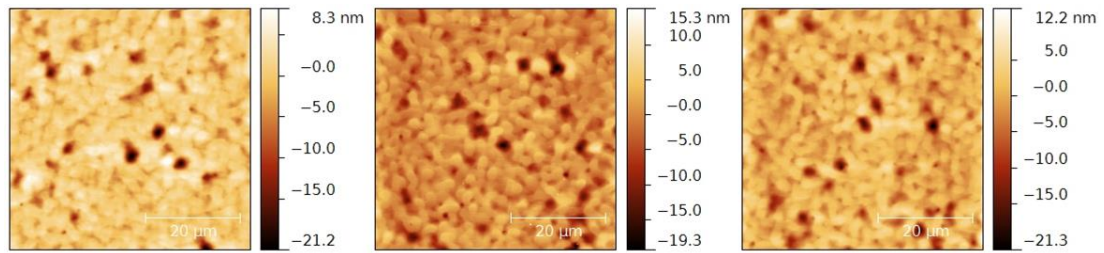
Figure 4-10 50 × 50 μm AFM scans of fully strained epilayer samples with a range of compositions (left) $Ge_{0.942}Sn_{0.058}$ (centre) $Ge_{0.908}Sn_{0.092}$ (right) $Ge_{0.896}Sn_{0.104}$. All samples have an RMS roughness of 3 nm. All samples have surface pit features, but no indication of crosshatching or other significant features.

The surface morphology of strained epilayer samples is relatively smooth, with a surface roughness ~3 nm, with the dominant surface feature being surface pits. These surface pits can be attributed to material etching during growth due to the production of HCl as a by-product during growth; this process is observed when using the $SnCl_4$ precursor to produce SnO_2 [129]. A representative sample of AFM scans of strained layers, with a range of epilayer alloy compositions is given in Figure 4-10.
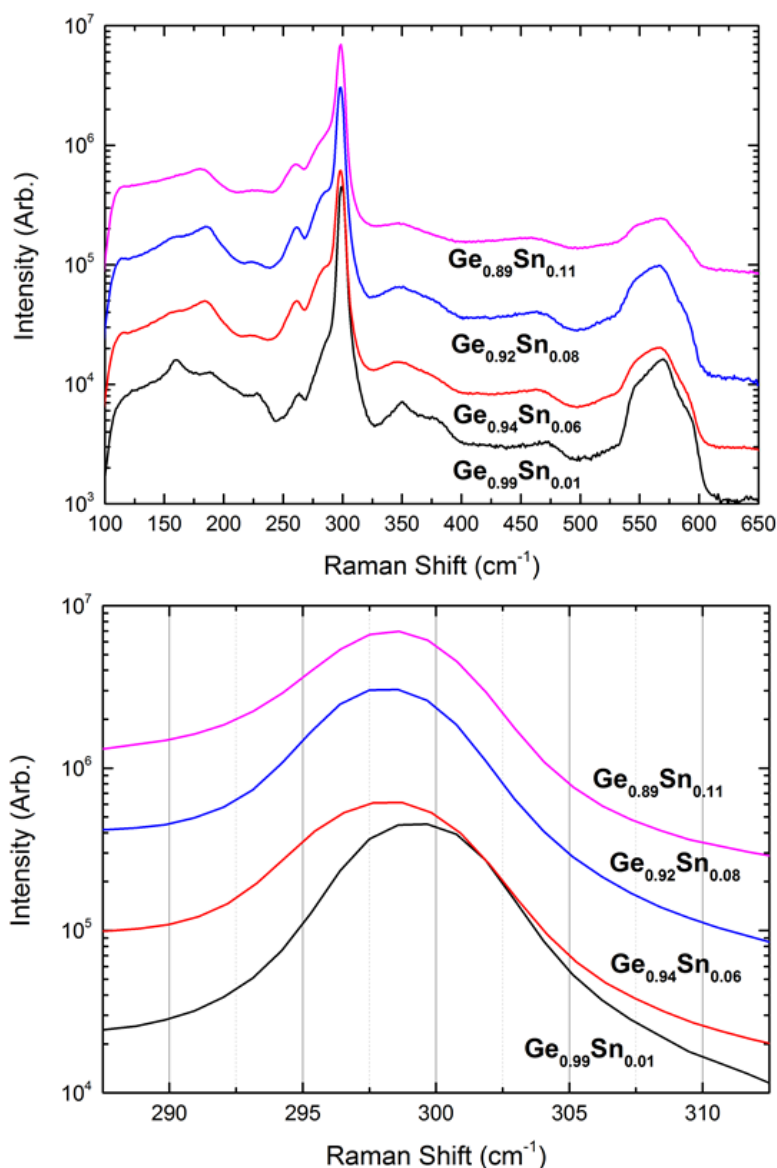
Figure 4-11 Raman spectra from several strained $Ge_{1-x}Sn_x$ epilayers with Sn fractions of 1 (black), 6 (red), 8 (violet) and 11 at. % (pink). The lower plot highlights the shift in Ge-Ge mode, note the Raman peak shifts from 1 at. % Sn to 6 at. % Sn but the peak shift is slight. From 6 at. % to 11 at. % Sn fraction no additional shift in the Ge-Ge mode is observed. This is attributed to the effect on Ge-Ge Raman mode position of increased layer compressive strain compensating for the increased Sn fraction. Sample intensities are offset in intensity (y-axis) for clarity.

Figure 4-11 Raman spectra from several strained $Ge_{1-x}Sn_x$ epilayers with Sn fractions

of 1 (black), 6 (red), 8 (violet) and 11 at. % (pink). The lower plot highlights the shift

in Ge-Ge mode, note the Raman peak shifts from 1 at. % Sn to 6 at. % Sn but the

peak shift is slight. From 6 at. % to 11 at. % Sn fraction no additional shift in the Ge-

Ge mode is observed. This is attributed to the effect on Ge-Ge Raman mode position of increased layer compressive strain compensating for the increased Sn fraction. Sample intensities are offset in intensity (y-axis) for clarity. Figure 4-11 shows Raman spectra from strained $Ge_{1-x}Sn_x$ epilayer samples for a range of compositions. The presence of the Ge-Sn Raman peak at ~260 cm^{-1} confirms the incorporation of Sn into the Ge lattice [121]. The Ge-Ge Raman mode, at ~300 cm^{-1}, of fully strained $Ge_{1-x}Sn_x$ epilayers is shown not to shift significantly with increased Sn fraction. It is expected that that this Ge-Ge Raman peak would

shift to lower wavenumber with increasing Sn fraction. The unexpected observation of a fairly constant Ge-Ge Raman shift value for all epilayer alloy compositions can be attributed to a balance between the tendency to shift to higher wavenumbers because of increased strain, from the increasing Sn fraction increasing the bulk lattice parameter, and the shift to lower wavenumbers because of the direct change in Sn fraction. This coupling of strain and alloy composition effects makes Raman spectroscopy unsuitable for determining the composition of strained $Ge_{1-x}Sn_x$ epilayers.

The maximum thickness observed by TEM of fully strained $Ge_{1-x}Sn_x$ epilayer samples for a range of compositions investigated in this work is shown in Table 4. These values place lower bounds on the critical thickness of plastic relaxation under these growth conditions.

Sn fraction (at. %)	1	6	8.5	10.6
Epilayer Thickness (nm)	300	75	50	40

Table 4 The maximum fully strained epilayer thickness observed in this work at a range of alloy Sn fractions

High crystal quality fully lattice strained $Ge_{1-x}Sn_x$ epilayers have been grown onto Ge-buffered Si(001) substrates with a range of epilayer thickness and Sn fractions. The material properties of the epilayers were controlled by modifying the growth temperatures and precursor mixture. For all growth temperatures investigated no evidence of polycrystallinity or Sn segregation is observed.

4.7 Partially Relaxed GeSn

Results of Raman spectroscopy measurements of both fully strained and partially relaxed $Ge_{1-x}Sn_x$ epilayer samples with similar Sn fraction are shown in Figure 4-12. From the lower panel, which emphasises the Ge-Ge peak ($\sim$300 cm^{-1}), this peak appears to move to lower Raman shifts for relaxed epilayer alloys for comparable Sn fractions, as expected.

For partially-relaxed epilayers an XRD rocking curve, example shown in Figure 4-14, cannot in isolation be used to determine the $Ge_{1-x}Sn_x$ epilayer composition, instead XRD RSMs are required to determine simultaneously the epilayer degree of strain relaxation and composition. In the asymmetric map, the $Ge_{1-x}Sn_x$ Bragg peak moves from directly under the Ge Bragg peak, for a fully strained alloy, to the line joining the Ge and Si Bragg peaks – i.e. a relaxed cubic lattice. The lattice relaxation occurs by the formation of misfit dislocations; these reduce the pristine crystallinity of the epilayer which leads to broadening of the $Ge_{1-x}Sn_x$ Bragg peak compared to a fully strained layer. An example of a symmetric and an asymmetric RSM is shown in Figure 4-14, note that the Ge buffer is slightly tensile strained due to the thermal mismatch between the Ge buffer and the Si substrate.
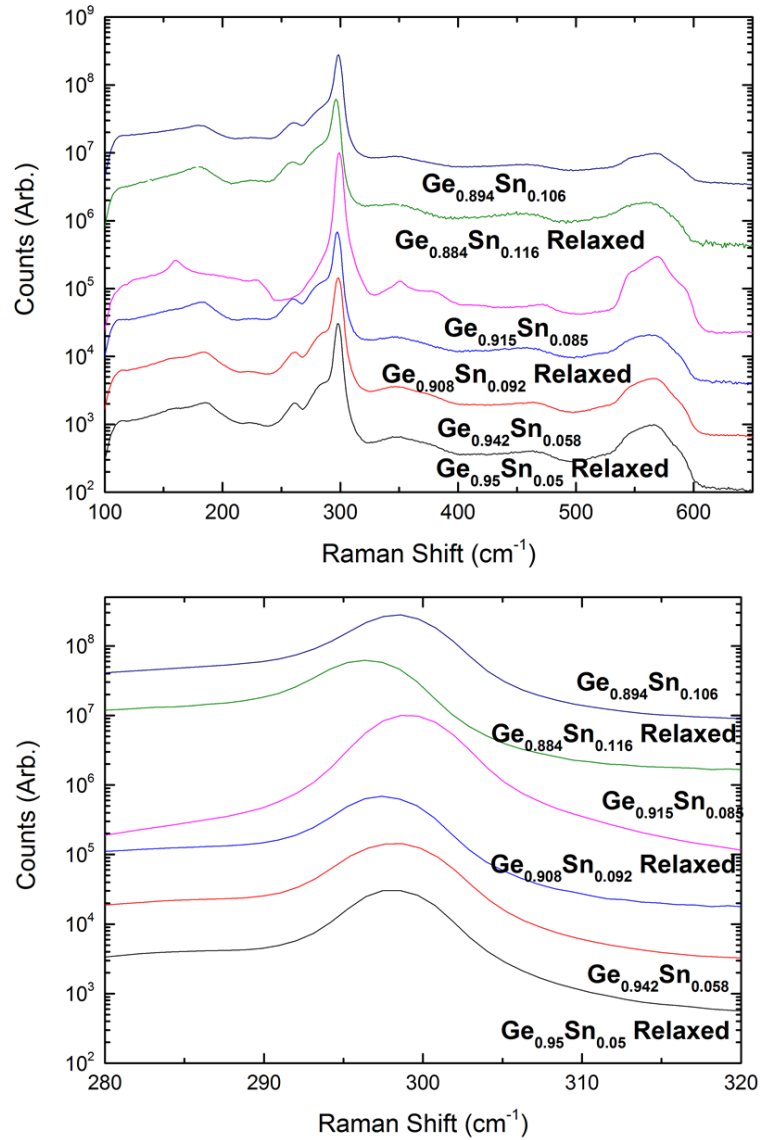
Figure 4-12 Raman spectra from $Ge_{1-x}Sn_x$ epilayers with a range of Sn fractions both strained and partially relaxed. The 5 at. % Sn relaxed epilayer has a similar Ge-Ge mode position to the 5.8 at. % Sn strained layer. However, the 9.2 at. % Sn partially relaxed epilayer is shifted to lower Raman shifts than the 8.5 at. % Sn strained epilayer. A similar behaviour is observed in the partially relaxed 11.6 at. % Sn epilayer and the 10.6 at. % Sn strained epilayer, with the relaxed epilayer Ge-Ge Raman mode being shifted to lower wavenumber than the strained layer of similar composition. Sample signal intensities are offset for clarity.
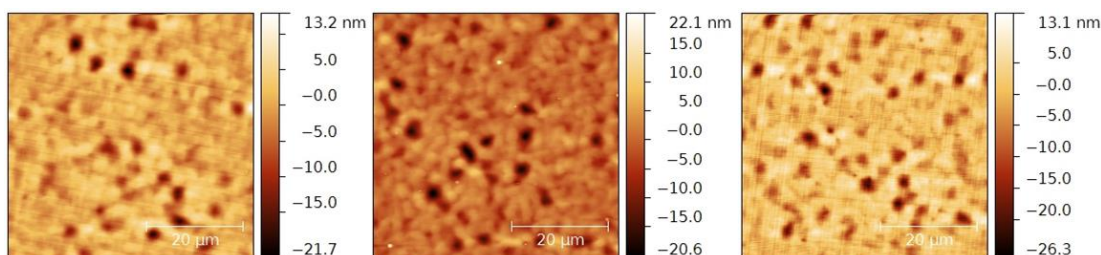
Figure 4-13 AFM scans of partially relaxed epilayer samples (left) $Ge_{0.949}Sn_{0.051}$, R=11.5%, RMS=3 nm (centre) $Ge_{0.908}Sn_{0.092}$ R=5.7% RMS=4 nm (right) $Ge_{0.884}Sn_{0.116}$ R=18.8% RMS=4 nm. Note cross hatching is observable for the for the R=11.5% and 18.8% samples, but not on the R=5.7% samples.
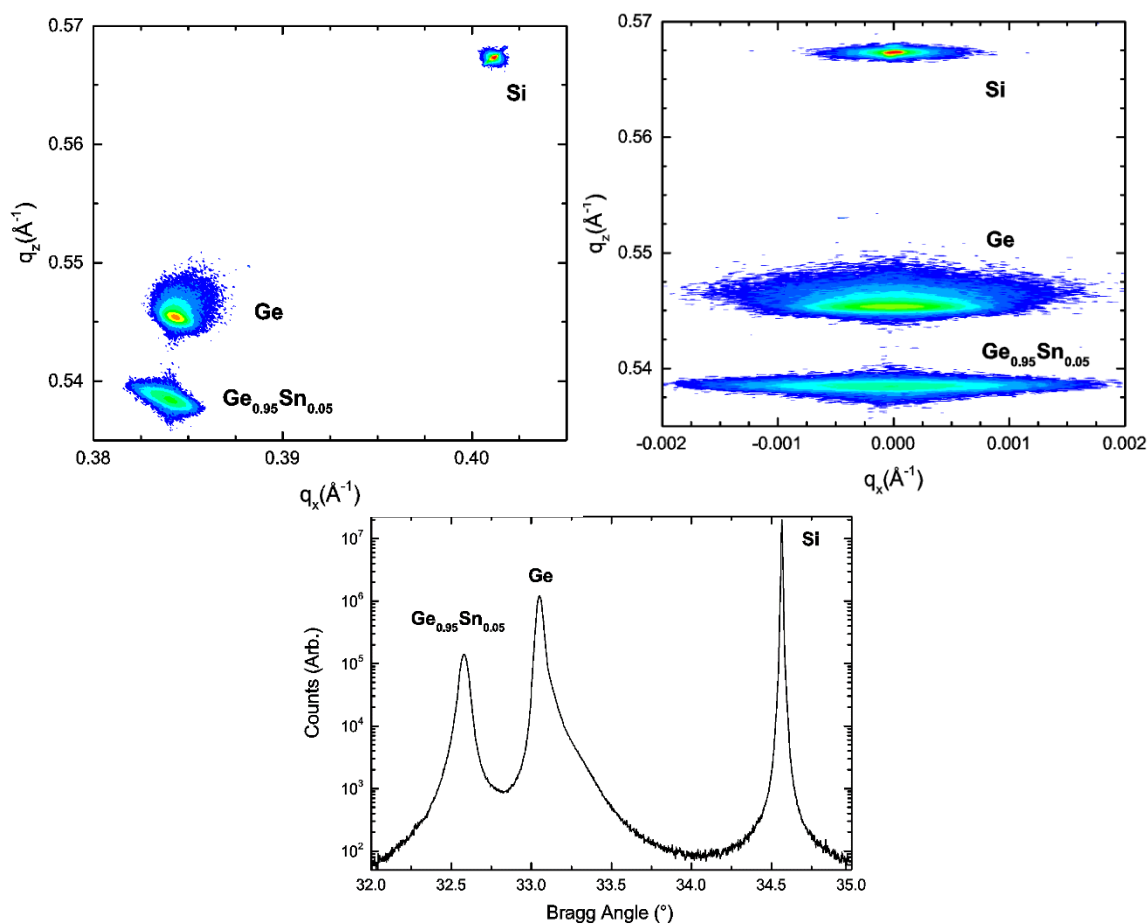

Figure 4-14 XRD scans from $Ge_{0.92}Sn_{0.05}$/Ge/Si, with the epilayer relaxed 15% with respect to the Ge buffer (Upper left) An asymmetric (224) RSM, note the GeSn peak is not directly under the Ge peak and has broadened along the relaxation line. (Upper right) A symmetric (004) RSM (Lower centre) A (004) rocking curve, without thickness fringes and a different Bragg peak lineshape.

In TEM images of partially relaxed $Ge_{1-x}Sn_x$ layers, Figure 4-15, strain relieving misfit dislocations are observed at the $Ge_{1-x}Sn_x$/Ge interface. These dislocations are confined to the interface and appear not to propagate up into the epilayer material; this is in agreement with other publications which indicate a tendency of GeSn/Ge structures to form (Lomar) edge dislocations, which propagate in-plane to relieve misfit strain [9,130].

Sn Fraction (at. %)	5.1	9.2	11.6
Epilayer Thickness (nm)	100	80	90
Degree of relaxation (%)	11.5	5.7	18.8

Table 5 Material parameters for a selection of the partially relaxed epilayer samples. These figures provide an upper bound on the epilayer thickness for the onset of relaxation at a range of alloy compositions. Relaxation is given relative to the Ge buffer.

When examining the surface topology of the partially relaxed epilayers, it is evident that the layers which have relaxed to a greater degree display cross-hatching features on the sample surface. This is to be expected with strain relaxation, but is not seen with the epilayer samples that are only slight relaxed, as shown in Figure 4-13. The surface roughness of the partially relaxed epilayers is comparable to that of fully strained epilayer samples, despite cross-hatching features; this is attributed to the surface topology being dominated by the pit features.

Even with relatively thick high Sn-fraction alloy epilayers, relatively low lattice strain relaxation values are achieved ≤19% with respect to the Ge buffer. To increase the degree of relaxation, the layer thickness would need to be increased beyond what has been produced in this work. Indeed, other groups have grown very thick layers of $Ge_{1-x}Sn_x$ and greater strain relaxation has been achieved; however, even with layers ~0.5 μm thick the residual compressive strain has not been completely removed [131].

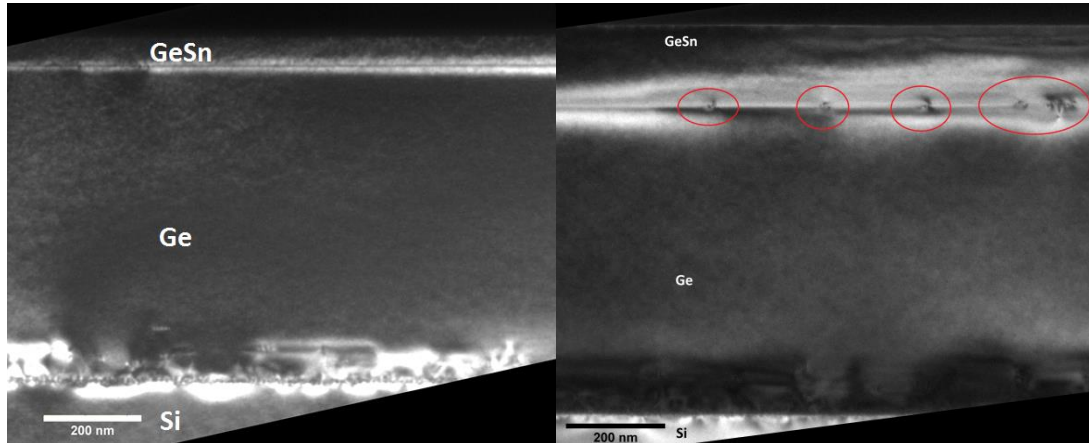Figure 4-15 Representative cross-sectional TEM images of Ge$_{1-x}$Sn$_x$/Ge/Si samples, both imaged in the (004) diffraction condition. (left) A fully strained Ge$_{1-x}$Sn$_x$ epilayer sample. No dislocations are visible at the GeSn/Ge interface. (right) A partially relaxed Ge$_{1-x}$Sn$_x$ epilayer sample, with misfit dislocations at the GeSn/Ge interface, (red circles).

Growing increasingly thick layers, beyond what has been produced in this work or reported in other publications, in order to increase strain relaxation has an effect on the material produced and the potential applications. Longer growth times would increase gas consumption, and other factors which would contribute to increased production costs. Increasing the growth time also increases the risk of significant surface segregation of the Sn adatoms during growth. To limit surface segregation, the Sn fraction of these particularly thick layers may need to be reduced.

4.8 Growth on Off-Axis Substrate

Offcut substrates are used to reduce the formation of antiphase domains when growing III-V semiconductor alloys onto group IV substrates, such as GaAs/Ge structures. However, when growing on the off-axis Si substrate, with the wafer cut at ~6° angle to the (001) crystal axis, it has been observed that thick Ge layers will have a lower crystallinity and rougher surface. This has been attributed to the predominance of particular Burgers vectors which reduce the probability of defect annihilation [41]. The different nature of misfit dislocation in GeSn layers, with the

dominance of edge dislocations at layer interfaces, may mean that this source of degradation of crystal quality when growing on off-axis substrates is not an issue.

4.8.1 XRD on Off-axis Substrates

As the Si substrate is cut off-axis to the [001] axis, when mounting the sample the on the X-ray diffractometer stage the sample edges do not match the crystal axis, but at an ~6° angle to the standard Si(001). During sample alignment, the scans must be significantly wider than standard, to ensure the Bragg peaks are scanned over. Rocking curves still scan along the (004) crystal orientation, simply that the plane is no longer directly perpendicular to the back of the wafer section. Similar to the growth direction during deposition no longer being purely in the <001> direction, as is the case with Si(001) substrates, but instead contains <100> and <010> components.

If sample angles are taken into account, i.e. measured Si (004) peak defined as being at the expected Bragg angle of bulk silicon for the XRD set-up then the angles of all other layer Bragg peaks will be compensated for.

4.8.2 Results of Off-Axis Growth

From the TEM images of $Ge_{1-x}Sn_x$ epilayer samples grown on off axis substrates roughening of the $Ge_{1-x}Sn_x$ epilayer surface is observed, see Figure 4-16, and evidence of Sn precipitation as globules of high contrast material is shown in Figure 4-17. The $Ge_{1-x}Sn_x$/Ge interface exhibits few lattice defects, despite the XRD observation discussed later in this section, indicating the epilayer has undergone partial lattice relaxation.

From the XRD RSMs in Figure 4-18 and Figure 4-19, we observe a reduced Sn fraction of the $Ge_{1-x}Sn_x$ alloy epilayer compared to material grown under similar

conditions using a standard on-axis substrate. Combined with the appearance of Sn precipitates on the surface of the off-axis material, this suggests that Sn atoms are inhibited from being incorporated into the crystal matrix during growth. The off-axis epilayers typically possess approximately 2-3 at. % Sn, which is greater than the equilibrium limit but significantly less than that achieved with growth on standard orientation substrates.
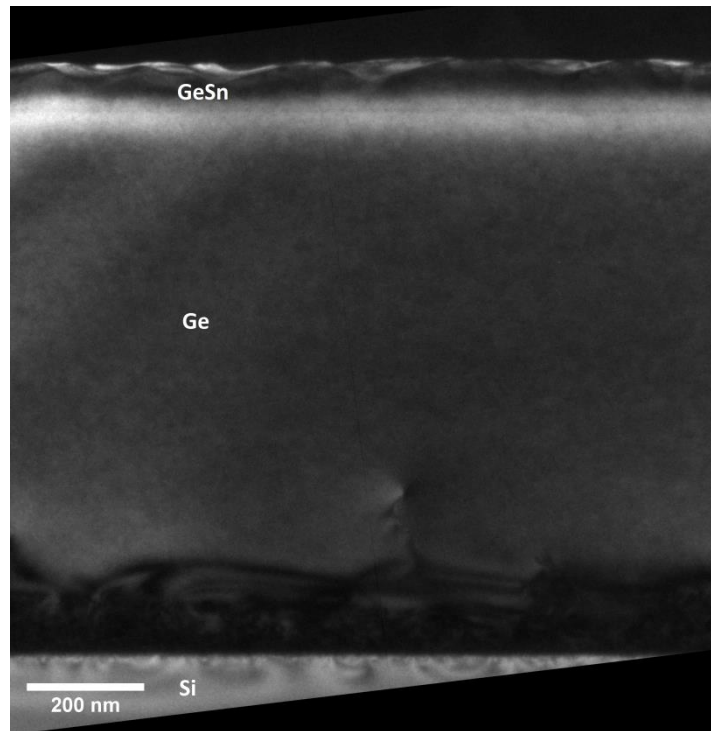
Figure 4-16 A TEM image in the (004) diffraction condition of GeSn/Ge/Si on an off-axis Si(001) substrate. No segregated regions are visable in the observed sample section, however the GeSn epilayer appears to have a rough surface. No dislocations are visable at the GeSn/Ge interface.
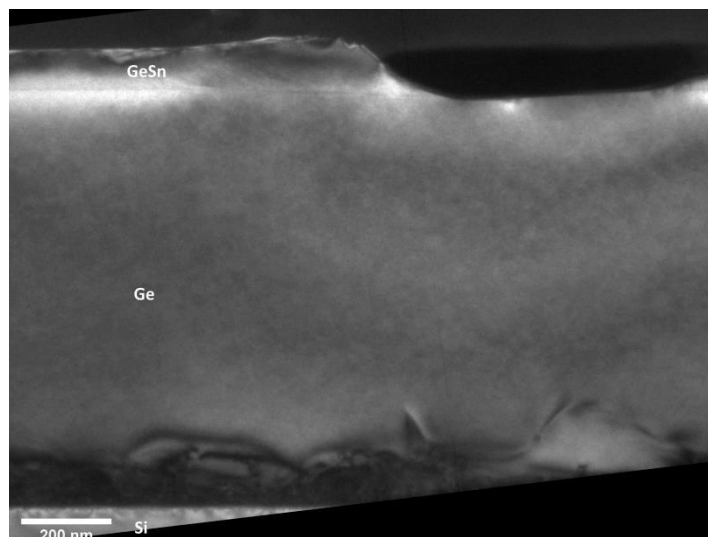

Figure 4-17 A TEM image in the (004) diffraction condition of GeSn/Ge/Si on a Si substrate cut at an angle to the (001) axis. High contrast material is visible at the epilayer, attributed to Sn rich material segregated from the crystal.
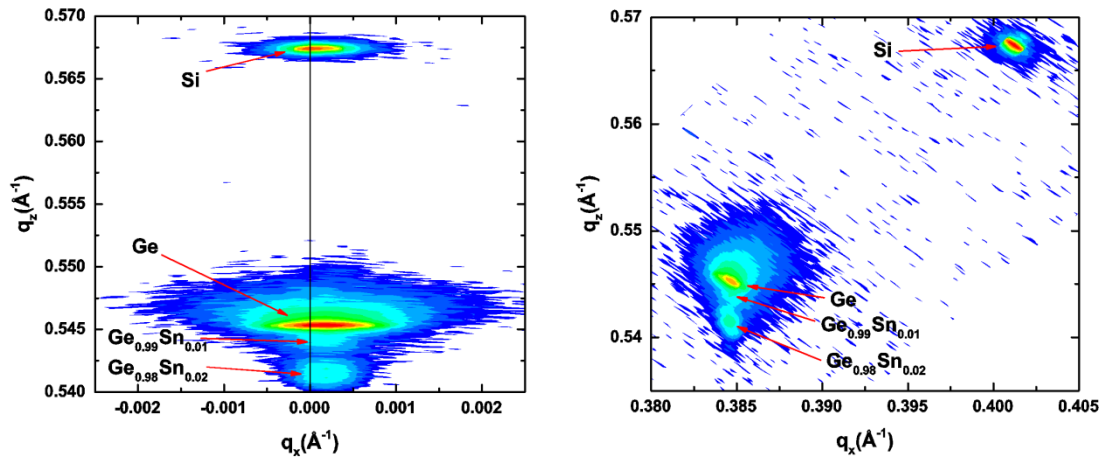
Figure 4-19 XRD RSM in the (left) (004) reflection and (right) (224) condition from the GeSn/Ge/Si sample, where the Si substrate is cut at an angle to the (001) axis. Two GeSn Bragg peaks are observed, indicating the epilayer is not monocrystalline.

Despite these $Ge_{1-x}Sn_x$ epilayers being thin and having a low Sn fraction, some strain relaxation is observed. Strain relaxation is not observed with thicker layers of $Ge_{1-x}Sn_x$ grown on standard Si substrates, but the lack of edge defects at the interface suggest the relaxation may be caused by the alloy segregation, which is detrimental to the crystal quality.

In many XRD RSMs, multiple $Ge_{1-x}Sn_x$ Bragg peaks are observed for each sample,
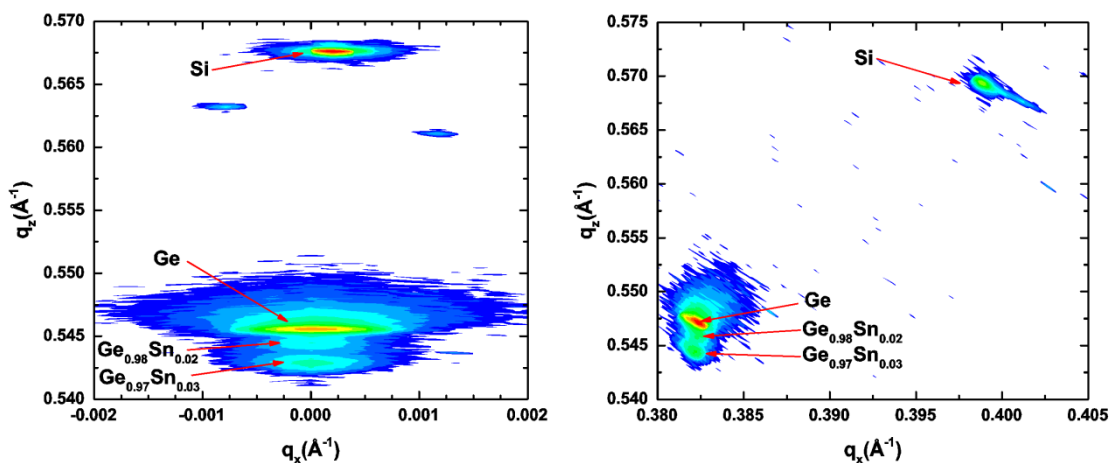

Figure 4-18 XRD RSM in the (left) (004) reflection and (right) (224) condition from the GeSn/Ge/Si sample, where the Si substrate is cut at an angle to the (001) axis. Two GeSn Bragg peaks are observed, of a different composition to the other off-axis substrate sample.
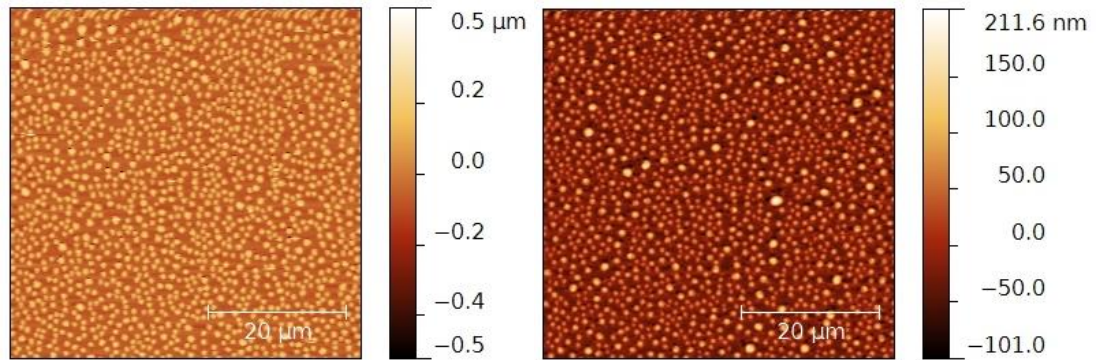
Figure 4-20 AFM Scans of GeSn/Ge/Si samples grown on offcut substrates.(left) RMS = 80nm, with nanodots approximately homogenously distributed. (right) RMS = 36nm, larger nanodots are observable, with regions devoid of nanodots around them.

typically two, indicating that the $Ge_{1-x}Sn_x$ layer is not a single crystal.

The surface topology of these samples, as shown in Figure 4-20, is very rough with a significant density of surface dots which are likely to be Sn precipitates. The size of these surface dots are of a similar scale to the Sn precipitates that were observed in the TEM images (Figure 4-17). Note that, in the left image of Figure 4-20. The surface dots are of a similar size and evenly distributed, whereas in the right image there are several larger surface dots, which have a greater than average distance to neighbouring surface dots. This may be attributed to the Sn precipitates agglomerating during growth, but more research is necessary to confirm this.

4.8.3 Summary of Off-Axis GeSn Growth

Though epitaxial growth on off-axis substrates is a potential route to increased layer relaxation, the strain relaxation is attributed to mechanisms which degrade the crystal quality. The reduction of the $Ge_{1-x}Sn_x$ growth rate on off-axis substrates also poses a serious problem exacerbating the low growth rates on standard orientation substrates. This may mean structures grown on off-axis substrates may be appropriate for

devices consisting of structures desired to have thin layers of relatively low Sn fraction $Ge_{1-x}Sn_x$ alloys.

The significant change in material properties observed with off-axis substrates indicates significant work is required to re-calibrate growth conditions with changes to the substrate. As a reduction in growth rate inhibits the maximum Sn fraction attainable it is necessary to compensate for this by tuning the growth conditions. Here growth conditions identical to those used for successful growth on standard substrates produced polycrystalline $Ge_{1-x}Sn_x$ growth and surface Sn precipitates which increased the surface roughness. In published articles, changing substrate orientation also changed the relation between $Ge_{1-x}Sn_x$ strain relaxation with other parameters [132].

If a method which increases the growth rate is implemented, such as the use of higher order precursors, this may enable growth of higher Sn-fractions on off-axis substrates. However, this method significantly increases costs, which are already increased by using off-cut substrates, which are more expensive than standard Si(001) substrates.

4.9 Summary

Both fully strained and partially relaxed $Ge_{1-x}Sn_x$ alloy epilayers have been grown by CVD onto Ge-buffered Si(001) substrates, with some limits of the critical thicknesses of relaxation for a range of alloy compositions identified. Decreasing the growth temperature from 350 °C to 270 °C has been demonstrated to increase the possible Sn fraction of the alloy to 12 at. %. However, further reductions of the growth temperature have demonstrated no further increase in alloy Sn fraction.

The epilayer alloy composition and layer thickness have both been shown to affect the strain state of the as-grown alloy, with layers of higher Sn fractions and higher growth temperatures having a lower critical thickness of relaxation. Strain relaxation in $Ge_{1-x}Sn_x$ epilayers produces dislocations which are predominantly in-plane and confined to the epilayer-buffer interface. Inducing significant $Ge_{1-x}Sn_x$ epilayer strain relaxation by growth of thick layers is challenging as even very thick layers lead to relatively low degree of relaxation. Additionally, very thick layers require extended growth times which are less economical, thus alternative methods of strain relaxation are worth investigation.

The use of nitrogen as the carrier gas has been demonstrated to have a significant impact on growth, in most cases resulting in no $Ge_{1-x}Sn_x$ growth at all. When $Ge_{1-x}Sn_x$ growth does occur the growth rate is reduced and the Sn fraction is altered compared to comparable growth conditions with the H_2 carrier gas.

Growth onto off-axis substrates has been demonstrated to lead to polycrystalline growth, a limited Sn fraction and alloy segregation with leads to a rough surface. This is not suitable for subsequent growth of other materials, including III-V alloys.

Successful CVD growth of the ternary $Si_yGe_{1-x-y}Sn_x$ has been demonstrated, the growth rate and Sn fraction are both reduced compared to binary alloy growth under comparable conditions. The Si precursor appears to compete with the Sn precursor during growth, reducing the Sn fraction.

5 Thermal Stability of GeSn Epilayers

This examines chapter the materials characterization of $Ge_{1-x}Sn_x$ epilayers when subjected to high temperatures.

The thermal stability of $Ge_{1-x}Sn_x$ epitaxial layers is an important area of investigation if the material is to be utilized in devices. High temperatures are used for multiple device fabrication processes, such as Ohmic contact formation. Thermal treatments are also a potential route for inducing relaxation in strained $Ge_{1-x}Sn_x$ epilayers. In similar materials rapid thermal annealing and other high temperature treatments are also used for crystal healing; where the degradation of layer crystallinity after a process such as ion implantation is subsequently partially restored with thermal treatments in order to enhance the crystalline semiconductor material and its electrical properties [133].

While there is strong motivation to investigate $Ge_{1-x}Sn_x$ at high temperatures, there are also inherent challenges due to the alloy's metastability. The majority of the $Ge_{1-x}Sn_x$ layers investigated in this work, and in published literature, have a higher Sn fraction than the equilibrium solid solubility limit of ~1 at. %: the greater the Sn fraction the further the material is from a stable state. Investigating the response to these supersaturated $Ge_{1-x}Sn_x$ alloys layers to high temperatures is necessary to understand the relationships between material parameters and the limits of alloy thermal stability. There exist multiple possible influences on the stability of $Ge_{1-x}Sn_x$ alloy layers, several of which are investigated in this work.

5.1 Motivation

Thick layers of high Sn fraction crystalline $Ge_{1-x}Sn_x$ have not yet been realised with full strain relaxation on Si or Ge. Moreover, the existing thick layers are expensive to

produce due to the low growth rate, necessitating long growth times. Thermal annealing is used in silicon-germanium hererostructures for strain relaxation and improving crystallinity, it is possible that similar techniques may be used in the germanium-tin system to induce strain relaxation and improvements in crystal quality [134].

Crystalline $Ge_{1-x}Sn_x$ alloy layers are metastable and high temperatures have been shown to cause segregation of the alloy components, occasionally with some interesting features [19,66,67,69]. A consensus has not yet been reached on whether strain relaxation occurs before loss of crystallinity, or what conditions are necessary to observe the $Ge_{1-x}Sn_x$ layer undergoing strain relaxation without material degradation. It would be of great utility for $Ge_{1-x}Sn_x$ applications to be able to induce strain relaxation without loss of crystallinity.

For $Ge_{1-x}Sn_x$ layers to be widely used in semiconductor devices, the acceptable thermal limits of the material without a significant change in the material properties must be determined. These limits will depend on the material properties of the alloy layers, which must be understood so that the appropriate thermal limits can be placed on the future development of device processing procedures.

Many publications in this area have focused on a narrow range of alloy compositions, with the thermal treatment methods varying between different studies. This investigation aims to study the effect of varying several $Ge_{1-x}Sn_x$ alloy layer properties, including a wide range of alloy Sn fractions, epilayer thicknesses, and as-grown strain relaxation states. In the investigation it will be desirable to use small temperature intervals between each characterization, in order increase the precision of the measurements. Published literature has suggested there exists a critical temperature at which material degradation occurs, but the use of wide thermal

treatment temperature intervals in the previous study prevented conclusive proof [69]. To meet these conditions we sought thermal treatment methods with *in-situ* materials characterization to support more standard *ex-situ* characterization post-treatment.

In addition to researching crystalline $Ge_{1-x}Sn_x$ response to thermal treatments, the formation of germanium-tin-oxide layers is also investigated. Tin-oxides are already widely used in consumer products, such as for glass coatings, and the material is well understood. There has also been a recent resurgence in interest of germanium-oxides for use as FET gate dielectrics and other uses. But while oxides of the constituent elements have been investigated, oxides of the crystalline $Ge_{1-x}Sn_x$ alloy have yet to be thoroughly investigated. This work undertakes some preliminary studies on germanium-tin-oxides, which could set the foundation for further investigations.

5.2 Lab Based Thermal Stability Studies

For investigations of thermal treatments of $Ge_{1-x}Sn_x$ epilayers an Anton-Parr DHS1100 temperature controlled stage was mounted on to a Panalytical X'Pert Pro MRD, for *in-situ* XRD rocking curves of $Ge_{1-x}Sn_x$/Ge/Si samples at higher temperatures. The $Ge_{1-x}Sn_x$ epilayer samples were thermally treated in an atmospheric environment while covered by a graphite dome. The attributes of this stage are discussed in detail in chapter 3.

For each $Ge_{1-x}Sn_x$/Ge/Si(001) sample, an initial XRD (004) rocking curve was measured with the sample at ambient an temperature of ~25 °C, using the temperature controlled configuration. The sample temperature was increased at a rate of 5 °C/min to 100 °C, the sample temperature was then maintained for 15 minutes to ensure temperature stability, after which a (004) rocking curve was measured at a

stable sample temperature of 100 °C. For subsequent measurements the sample temperature was increased at 5 °C intervals, using a temperature ramp rate of 5 °C/min followed by a 5 minute pause time to ensure temperature stability. After temperature stabilization a XRD (004) rocking curve was measured. These 5 °C measurement intervals were repeated up to the maximum sample temperature of 600 °C where a (004) rocking curve was measured and the sample gradually cooled to ambient temperature, using a ramp rate of -5 °C/min.

The 5 °C/min temperature ramp rate was chosen as a compromise between limiting the time interval between scans, ensuring sample temperature during scans was stable and limiting any thermal shock the sample is subjected to. Each iteration of increasing the temperature by 5 °C, stabilizing the temperature and acquiring a (004) XRD rocking curve required approximately 40 minutes.

5.2.1 Pre-Treatment Characterisation

Prior to any thermal treatments, all samples were first characterized with a range of methods, explained in chapter 3, for a comprehensive understanding of material parameters including epilayer alloy composition, epilayer thickness, degree of strain relaxation, crystal quality, etc. These parameters were determined such that the impact of high temperatures on the $Ge_{1-x}Sn_x$ layer parameters could be investigated.

5.2.2 Data Analysis

The initial data from each sample consists of a XRD (004) rocking curve scan from each measurement temperature, rocking curves from selected temperatures of a single sample are shown in Figure 5-1. Over 100 individual rocking scans are obtained from each sample, which is too much to be directly intelligible.
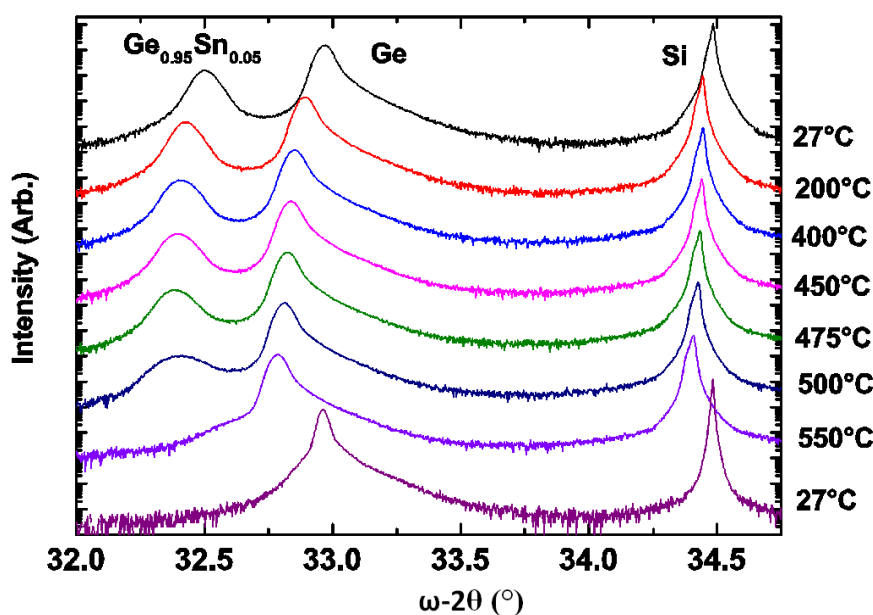
Figure 5-1 (004) rocking curve scans from selected temperatures from a Ge$_{0.95}$Sn$_{0.05}$/Ge/Si sample. The individual scans are offset in intensity (y-axis) to ease interpretation. As the temperature increases all Bragg peaks shift to lower angles, which is attributed to the thermal expansion of the lattice. The lowest scan was obtained at ambient temperature after thermal treatment process. As temperature increases the Ge$_{0.95}$Sn$_{0.05}$ Bragg peak intensity is approximately constant up to 200 °C, but decreases at higher temperatures, with the peak broadening and then essentially disappearing at 550 °C, indicating a total loss of crystallinity of the Ge$_{0.95}$Sn$_{0.05}$ epilayer.

Therefore peak fitting software was utilized to extract the Si substrate, Ge buffer and Ge$_{1-x}$Sn$_x$ epilayer Bragg peak 2θ position, FWHM and intensity at each measurement temperature. The Si and Ge Bragg peaks are not of great significance, as both layers are stable in the temperature range investigated, but serve as indicators to a change in configuration unrelated to changes in the sample, for example a large decrease in intensity for all Bragg peaks may indicate the sample being slightly misaligned from the maximum intensity half-beam position. These Bragg peak parameters were chosen as they are the most indicative of material properties. Figure 5-2, Figure 5-3 and Figure 5-4 show example plots of intensity, omega angle and FWHM, respectively, from each layer of a Ge$_{1-x}$Sn$_x$/Ge/Si sample.
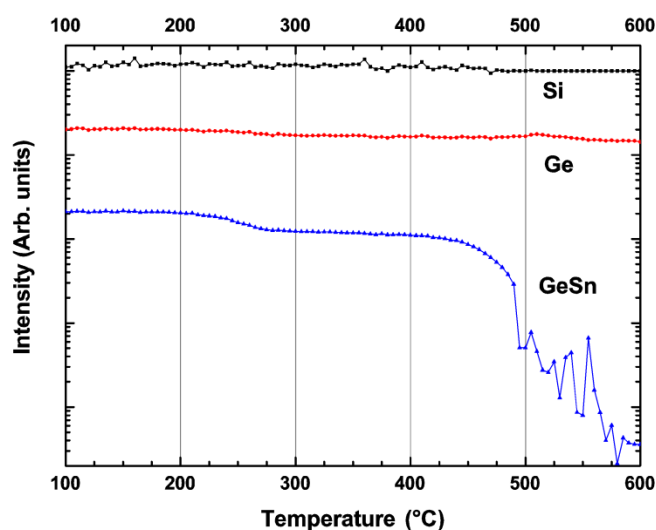
Figure 5-2. The *in-situ* Bragg peak **intensity** from the Si substrate (black), Ge buffer (red) and Ge$_{1-x}$Sn$_x$ epilayer (blue) of a Ge$_{0.95}$Sn$_{0.05}$/Ge/Si sample over the range of temperatures. Due to the large range of Bragg peak intensity between the layers the intensity is plotted on a logarithmic scale. The Si and Ge peaks are significantly more intense than the Ge$_{1-x}$Sn$_x$ layer peak due to the thicker layers contributing a larger diffraction volume. The Si and Ge intensity remain approximately constant, indicating stability up to the maximum temperature. The Ge$_{1-x}$Sn$_x$ epilayer however shows a non-linear loss of intensity with increasing temperature. The intensity is stable, then decreases sharply from 210 – 280 °C, is stable from 280 – 430 °C, then decreases rapidly from 435 °C essentially disappearing at 495 °C.

From this data we may extract several important material parameters: the Ge$_{1-x}$Sn$_x$ Bragg peak 2θ value corresponds to the composition and strain state of the alloy, the FWHM indicates the degree of crystallinity of the associated layer, and intensity is a consequence of the degree of crystalline order in the layer and its thickness.

In the example shown, the Si and Ge Bragg peak intensity and FWHM are essentially constant with temperature. The Si and Ge Bragg peak omega positions gradually shift to lower angles with increasing temperature, due to thermal expansion increasing the lattice size, which is a consequence of *in-situ* XRD measurements.

A different behaviour is observed for the Ge$_{1-x}$Sn$_x$ Bragg peak: by the maximum measurement temperature the Bragg peak intensity has decreased by several orders of magnitude, the peak has broadened significantly with the FWHM more than

tripling, and a notable increase in omega position has occurred. At 600 °C the Ge$_{1-x}$Sn$_x$ epilayer crystallinity has clearly degraded significantly, in a manner in which the Ge buffer and Si substrate layers have not. For the sample shown in this example, the crystallinity loss has neither been abrupt, as would be expected from a critical temperature, nor has the crystallinity degraded as a linear function of temperature.

Figure 5-3 The *in-situ* Bragg peak **omega angle** from the Si substrsate (black), Ge buffer (red) and Ge$_{1-x}$Sn$_x$ epilayer (blue) over the temperature range 100 to 600 °C. For all layers omega is observed to decrease with temperature, which can be attributed to thermal expansion of the crystal lattice. The substrate and buffer show only the effect of thermal expansion, the Ge$_{1-x}$Sn$_x$ epilayer however displays different behaviour with an increase in the Bragg peak omega position above 500 °C. This coincides with the temperature range of the complete loss of Bragg peak intensity seen in Figure 5-2.
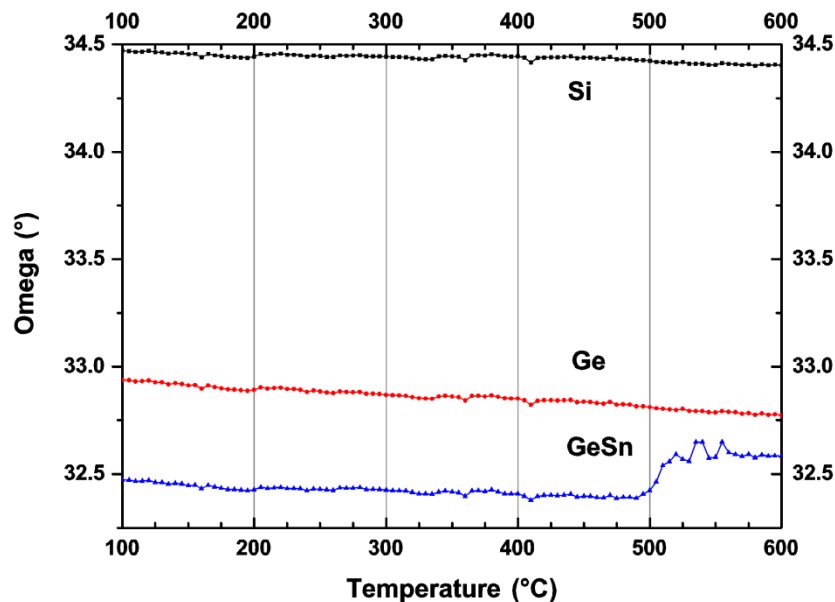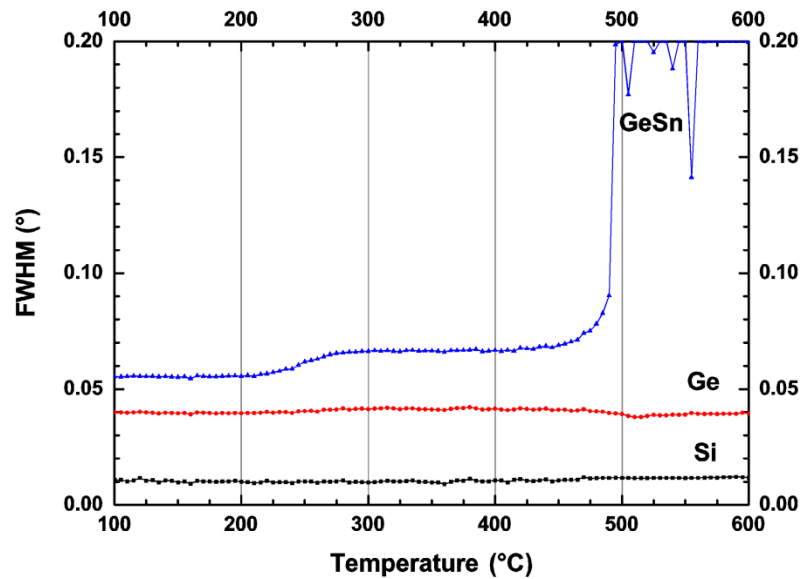
Figure 5-4 The *in-situ* Bragg peak **FWHM** from the Si substrate (black), Ge buffer (red) and Ge$_{1-x}$Sn$_x$ epilayer (blue) from 100 – 600 °C. Note the Ge buffer and Si substrate Bragg peaks FWHM remain essentially stable for all temperatures, indicating crystal quality is uneffected. The observed behaviour of the Ge$_{1-x}$Sn$_x$ epilayer is similar that seen for the Bragg peak intensity shown in Figure 5-2. The FWHM is constant at ~0.055° from 100 - 210 °C, broadens from 215 - 275 °C up to ~0.065°, is stable from 280 - 445 °C and then broadens again rapidly at higher temperatures, becoming essentially undecernable at 495 °C, coninciding with the total loss of the Bragg peak intensity.

5.2.3 Critical Temperature
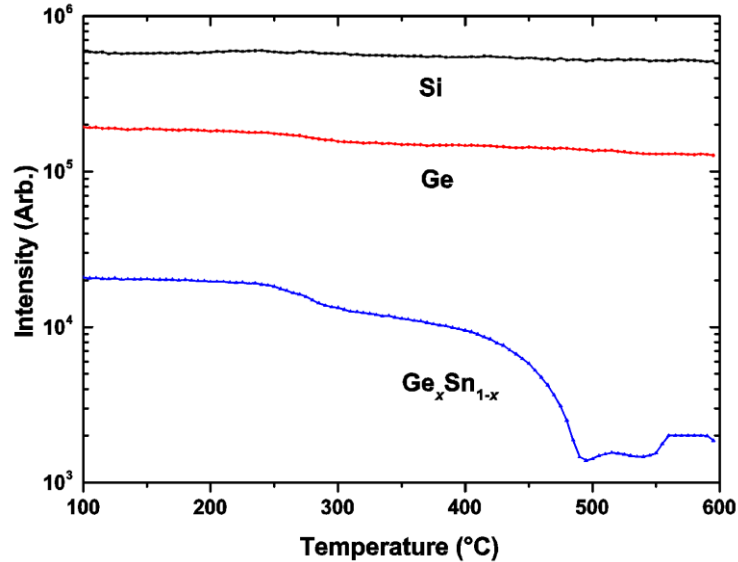
Figure 5-6 The (004) Bragg peak intensity from each layer of the $Ge_{0.94}Sn_{0.06}$/Ge/Si structure. The Si substrate and Ge buffer Bragg peak intensity decrease smoothly with increasing temperature to a limited degree, this attributed to the increased atomic vibrations due to the increased thermal energy. The $Ge_{1-x}Sn_x$ epilayer displays a more complex behaviour. The Bragg peak intensity is plotted on a logarithmic scale for clarity.

Figure 5-5 The (004) Bragg peak intensity from the epilayer of the $Ge_{0.94}Sn_{0.06}$/Ge/Si structure, on a linear scale. The intensity decreases sharply from 240 – 290 °C, then decreases more gradually to 410 °C, before decreasing rapidly at temperatures beyond 410 °C.

135
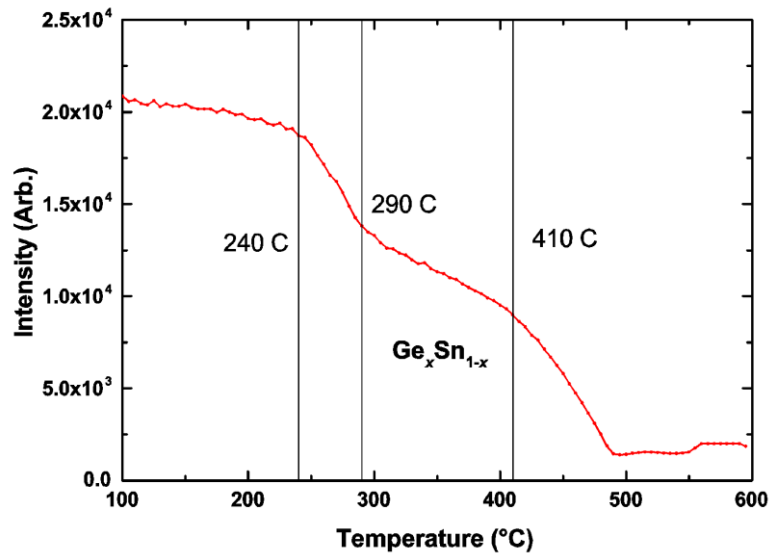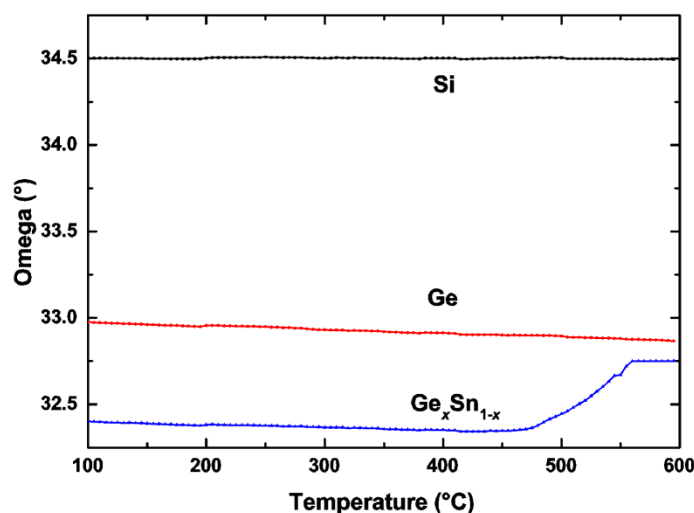
Figure 5-7 The XRD (004) Bragg peak omega position from all layers of the $Ge_{0.94}Sn_{0.06}/Ge/Si$ structure. The Si and Ge Bragg peak positions shift to lower angles with increased temperature due to thermal expansion as seen elsewhere. The $Ge_{1-x}Sn_x$ epilayer Bragg peak follows a similar behaviour until 475 °C, where it shifts to higher angles with temperature, which is attributed to Sn segregating out of the lattice.
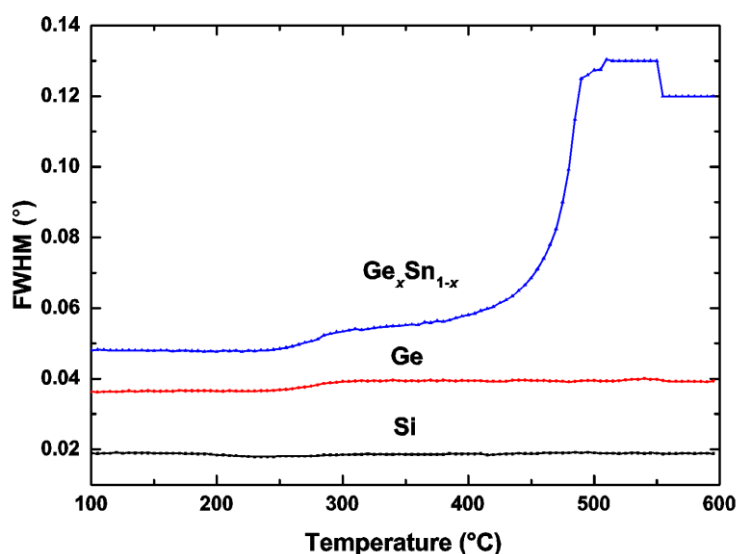
Figure 5-8 The (004) Bragg peak FWHM from $Ge_{0.94}Sn_{0.06}/Ge/Si$ structure for all layers. The Si and Ge Bragg peak widths are relatively stable with temperature. The $Ge_{1-x}Sn_x$ peak width increase slightly from 250 - 300 °C, then is fairly stable up to 400 °C and then widens rapidly as the temperature increases above 400 °C.

By examining the material properties of the relatively low Sn fraction $Ge_{1-x}Sn_x$ epilayers with temperature, as shown for a fully strained $Ge_{0.94}Sn_{0.06}$ epilayer (on a relaxed Ge buffer on a Si(001) substrate) in Figure 5-5, Figure 5-6, Figure 5-7 and

Figure 5-8, the layer is observed to be thermally stable up to high temperatures. Significant material degradation is observed as the sample temperature increases above ~400 °C, which is potentially due to oxidation of the layer from atmospheric oxygen. The $Ge_{1-x}Sn_x$ Bragg peak omega position, intensity and FWHM are relatively stable for much of the studied temperature range, then all indicate rapid material degradation at the same temperature range, providing confidence for the assertion that the change is a degradation of the epilayer crystal quality. The Si substrate and Ge buffer appear essentially unaffected by the thermal treatment. The behaviour shown here is similar to the behaviour observed in other low Sn fraction $Ge_{1-x}Sn_x$ epilayer samples, which were given as an example in the previous section, and appears typical for low Sn fraction $Ge_{1-x}Sn_x$ epilayer samples in this study.
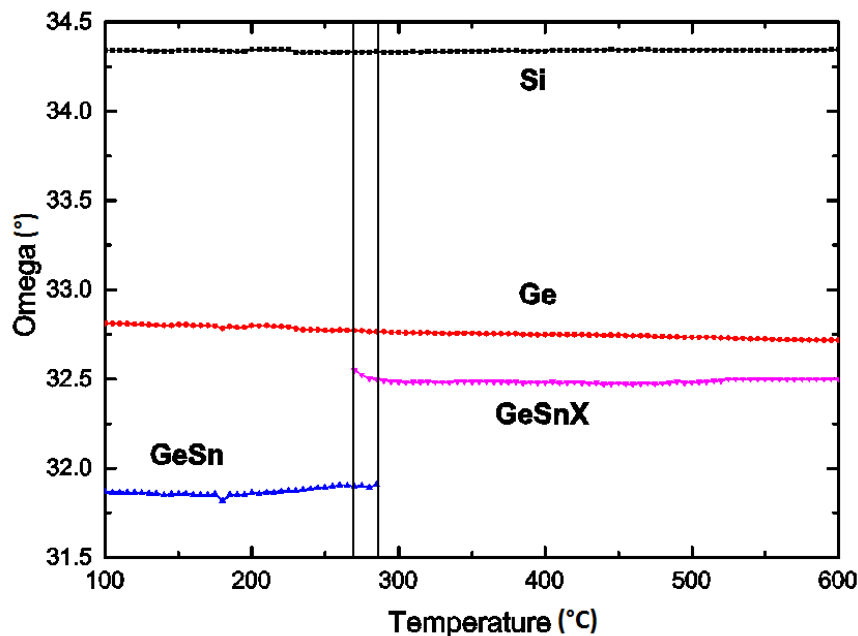

Figure 5-9 The XRD (004) Bragg peak omega position from each layer from a $Ge_{0.895}Sn_{0.105}$/Ge/Si sample. The Ge buffer and Si substrate Bragg peak positions are stable with temperature. At 270 °C a new Bragg peak appears, which is labelled GeSnX, between the original $Ge_{1-x}Sn_x$ layer and the Ge buffer. Above 290 °C the initial $Ge_{1-x}Sn_x$ Bragg peak essentially disappears.

137
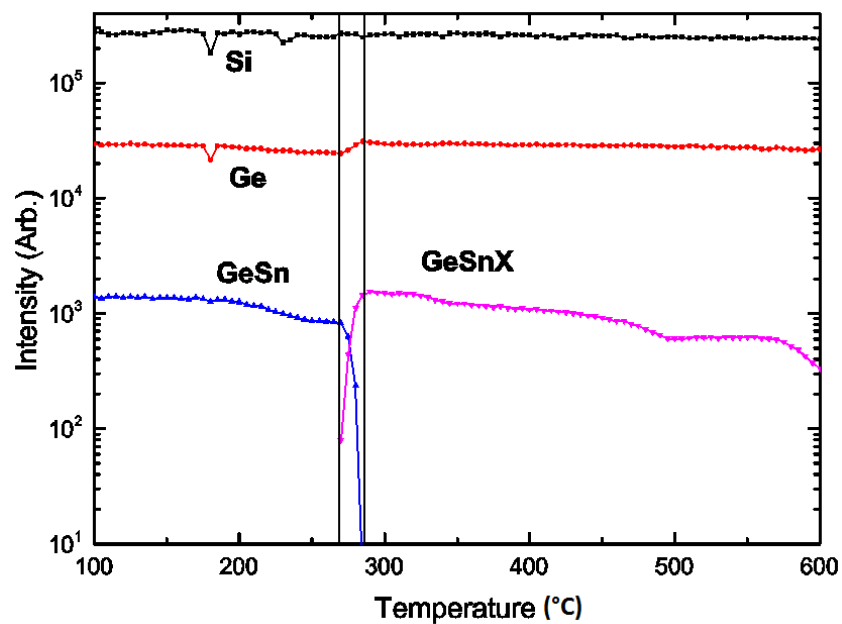
Figure 5-10 The XRD (004) Bragg peak intensity from each layer from a
$Ge_{0.895}Sn_{0.105}$/Ge/Si sample. While the Si and Ge Bragg peak intensities are
relatively stable with temperature, the $Ge_{1-x}Sn_x$ Bragg peak intensity is
initially stable and then drops dramatically from 260 – 275 °C. Within this
temperature range an additional Bragg peak appears, labelled GeSnX, which
increases in intensity with increasing temperature within this range.

A markedly different behaviour is observed with higher Sn fraction epilayers. Figure

5-9, Figure 5-10 and Figure 5-11 are the plots of the (004) Bragg peak FWHM,

intensity and omega position for each layer in a $Ge_{0.895}Sn_{0.105}$/Ge/Si sample, where

the $Ge_{0.895}Sn_{0.105}$ epilayer was fully strained to the Ge buffer prior to the thermal

treatment. Again, the Ge buffer layer and Si substrate appear to be stable for all

temperatures, with only minor changes to their Bragg peak intensities, FWHMs and

omega positions. However, the $Ge_{0.895}Sn_{0.105}$ epilayer degrades rapidly by all metrics

at a relatively low temperature and in a sudden manner. The $Ge_{0.895}Sn_{0.105}$ epilayer

Bragg peak FWHM, omega position and intensity are stable with temperature until a

sample temperature of ~270 °C, with only a minor shift in omega positon to higher

angles, which is opposite to what is expected from thermal expansion, and some

moderate peak broadening observed for temperatures temperature above ~200 °C. At
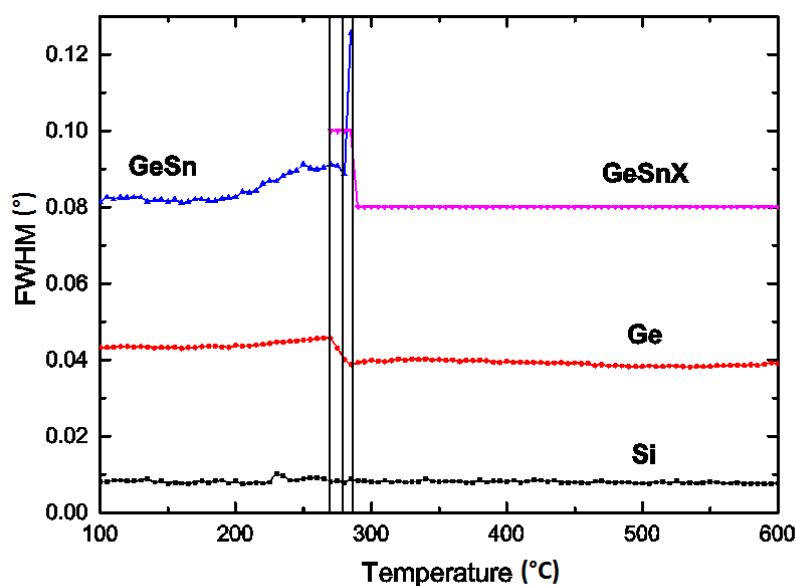
Figure 5-11 The (004) Bragg peak FWHM from each layer from a $Ge_{0.895}Sn_{0.105}$/Ge/Si sample. The $Ge_{0.895}Sn_{0.105}$ broadens with temperature above 200 °C. The Bragg peak appearing at ~270 °C has an essentially constant width with temperature. The Si Bragg peak has an essentially constant width for all temperatures, in contrast the Ge buffer Bragg peak appears to broaden above 200 °C and then narrow from 270 – 290 °C, then stabilizes at the new lower peak width.

temperatures above 270 °C, in a small number of temperature increase and measurement cycles, the $Ge_{1-x}Sn_x$ epilayer Bragg peak broadens significantly and the intensity drops by several orders of magnitude. During this temperature interval, from ~270 to 290 °C, an additional Bragg peak appears which is at an omega position between the Ge buffer and the initial $Ge_{1-x}Sn_x$ Bragg peaks and so is assumed to be a lower Sn fraction $Ge_{1-x}Sn_x$ alloy. If it is a $Ge_{1-x}Sn_x$ layer, the omega position indicates an alloy with a Sn fraction of ~1 at. %. This new layer is relatively stable up to high temperatures, remaining up to 600 °C, the maximum sample temperature in this study.

The appearance of this additional Bragg peak, coinciding with the loss of the initial $Ge_{0.895}Sn_{0.105}$ layer Bragg peak suggests the material responsible for Bragg peak is formed from the residual material of the degraded $Ge_{0.895}Sn_{0.105}$ layer. The new

crystalline material may be attributed to a $Ge_{1-x}Sn_x$ alloy which is capable of being stable under the experimental conditions, with $x \approx 0.01$ being close to that of the solid solubility limit, with the excess tin atoms segregating out of the crystal lattice altogether.

An abrupt loss of crystallinity with increasing temperature was observed for many high Sn fraction $Ge_{1-x}Sn_x$ epilayer samples, this was the case for a range of epilayer thickness, alloy composition, strained layer thickness and for both pseudomorphic and partially relaxed epilayers, which have lattice defects already existing at the $Ge_{1-x}Sn_x$/Ge interface. The temperature at which the loss in epilayer crystallinity was observed varied between samples. This characteristic of abrupt loss of epilayer crystallinity was not observed for the intermediate, 5 - 6 at. % Sn, composition alloys as shown in earlier plots, which have a very different response to high temperatures. These results are strong evidence for both the existence of a critical temperature for high Sn fraction alloy layers, and that a critical temperature does not exist for lower Sn fraction alloys; indicating there is a change in alloy response to thermal treatments with increasing Sn fraction.

5.2.4 Relaxation
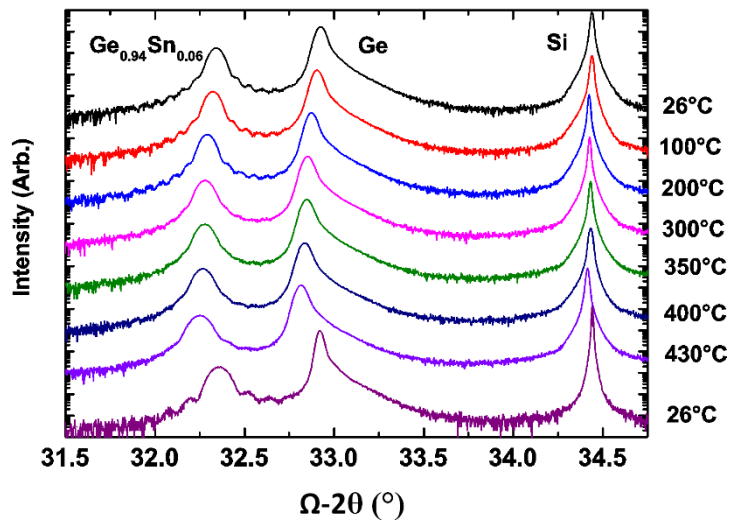
Figure 5-12 XRD (004) rocking curve plots from all layers of a $Ge_{0.94}Sn_{0.06}$/Ge/Si sample from selected temperatures. At lower temperatures the thickness fringes from the fully strained epilayer are observable. The fringes are still strong at 200 °C, and some fringes are discernible at 300 °C but have completely disappeared at 350 °C. This sample was taken to a maximum temperature of 430 °C, then cooled to ambient temperature. Scans at ambient temperature after the thermal treatments show the thickness fringes are again observable, although the layer has thinned due to growth of an amorphous surface oxide.

In standard XRD measurements, the disappearance of epilayer thickness fringes is indicative of the formation of sufficient strain relaxation induced misfit dislocations at the interface between the epilayer and the buffer. When heating the $Ge_{0.94}Sn_{0.06}$/Ge/Si sample, the thickness fringes of the $Ge_{1-x}Sn_x$ epilayer Bragg peak disappear at high temperatures, as shown in Figure 5-12; however, this cannot be attributed to epilayer strain relaxation, as the thickness fringes reappear upon sample cooling to ambient temperature. The fringes after the thermal treatment have a wider spacing, indicating the layer has thinned.

The reappearance of thickness fringes indicated that this configuration for thermal treatment with *in-situ* characterization method cannot be used to determine if layers

141

undergo strain relaxation during the thermal treatments. The loss of thickness fringes is not due to strain relaxation, but another cause, potentially the increased thermal energy and different thermal expansion of layers at high temperatures disrupts the coherent reflection of X-rays from the interface. However, the temperature at which material degradation occurs can be determined with *in-situ* measurements.

5.2.5 Thermal Treatment Surface Changes

AFM scans of several samples after the thermal treatment process are shown in Figure 5-13. For the lower Sn fraction alloy, as seen with the $Ge_{0.94}Sn_{0.06}$ epilayer example, the surface topology appears to very similar to the as-grown condition. The surface roughness is similar and the dominant surface features are surface pits in both cases.

In contrast, the surface topology of the higher Sn fraction alloy samples, $Ge_{0.895}Sn_{0.105}$ and $Ge_{0884}Sn_{0.116}$ epilayer examples shown in Figure 5-13, is radically changed by the thermal treatment process. The surface roughness increases significantly from the thermal treatment, and the dominant surface features have also changed with the surface pits no longer dominant. For the $Ge_{0.895}Sn_{0.105}$ epilayer taken to 600 °C, the dominant surface feature is a high density of surface dots, which are an order of magnitude in scale larger than the surface pits observed in the as-grown samples.

The $Ge_{0.884}Sn_{0.116}$ epilayer sample was heated to a maximum measurement temperature only slightly greater the epilayer critical temperature. The observed density of surface dots is much lower than the previous $Ge_{0.895}Sn_{0.105}$ sample, but each surface dot has a significantly larger volume. From these scans it can be seen that the surface dots have a trail running through them, and that surface pits exist

either side of the dot in the direction perpendicular to the trail. This surface topology is thought to be intermediate state, with further increases in sample temperature causing a change in surface topology to one similar to that observed from the $Ge_{0.895}Sn_{0.105}$ epilayer sample. This process would involve the high volume surface dots separating to form multiple lower volume. The presence of the trails only in the intermediate stage may indicate how the peaks initially form, with small Sn agglomerations connecting and Sn being transported along the trails at high temperatures to form the observed peaks.
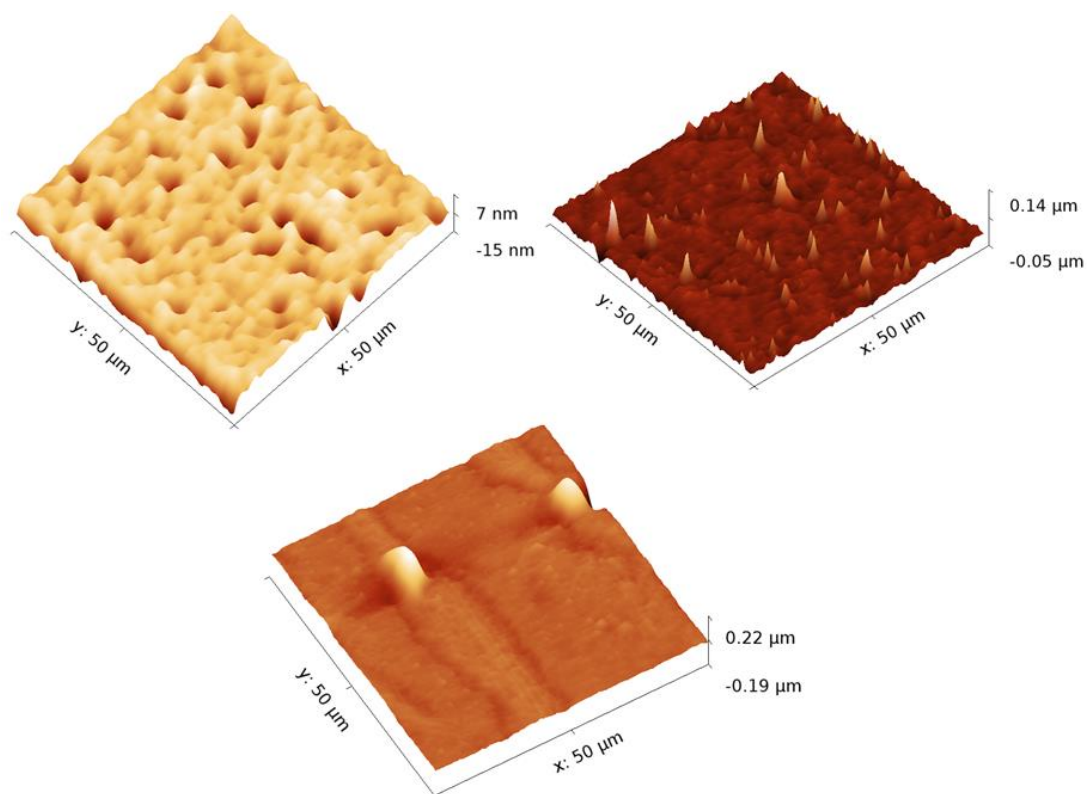
Figure 5-13 AFM scans of sample surface after the thermal treatment on the XRD temperature controlled stage. (Upper left) $Ge_{0.94}Sn_{0.06}$ epilayer sample surface, heated to 600 °C, without significant surface roughening with an RMS ~3 nm, the major surface features are pits as observed in as-grown samples. (Upper right) $Ge_{0.895}Sn_{0.105}$ sample surface, heated to 600 °C, the surface has significantly roughened, with an RMS ~9 nm, additionally the major surface features are large peaks on the surface. (Lower centre) $Ge_{0.884}Sn_{0.116}$ epilayer after XRD scan but stopping at a maximum temperature of 290 °C.
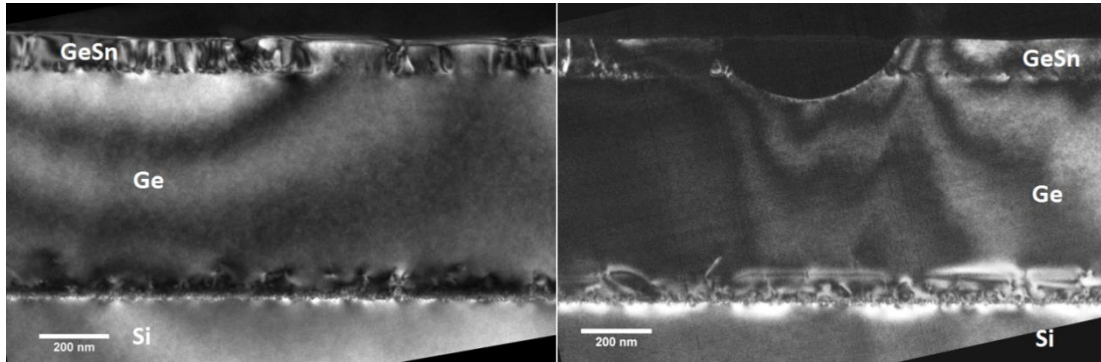
Figure 5-14 TEM images of $Ge_{0.884}Sn_{0.116}$/Ge/Si sample after XRD scan stopped at 290 °C. (left) (220) diffraction condition, the large concentration of defects are clearly visible. (right) (004) diffraction condition, in addition to the misfit dislocations to the right of the image, there is a large region of high density material at the interface, which has penetrated into the Ge buffer and is likely to be segregated Sn.

TEM images of the $Ge_{0.884}Sn_{0.116}$ epilayer sample after the thermal treatment, which was limited to 290 °C i.e. slightly above the critical temperature, are shown in Figure 5-14. From these images it can be observed that after exposure to temperatures slightly above the critical temperature the epilayer remains crystalline, though many lattice defects have formed, notably not all of these are edge dislocations that are typically observed in epilayer strain relaxation processes during epitaxial growth. Additionally, there is a globular-like feature of high atomic number material observable that is not confined to the epilayer, but penetrates into the Ge-buffer layer. This feature is attributed to segregated Sn, though it cannot be a surface dot feature observed in the AFM scan of the sample, as the globular structure does not protrude significantly above the epilayer surface. The structures observed may be a cross section through one of the "trails" observed in the AFM scans or a smaller feature.

The AFM and TEM imaging confirms that exceeding the $Ge_{1-x}Sn_x$ epilayer critical temperature is detrimental to the layer crystal quality. The observation of high atomic
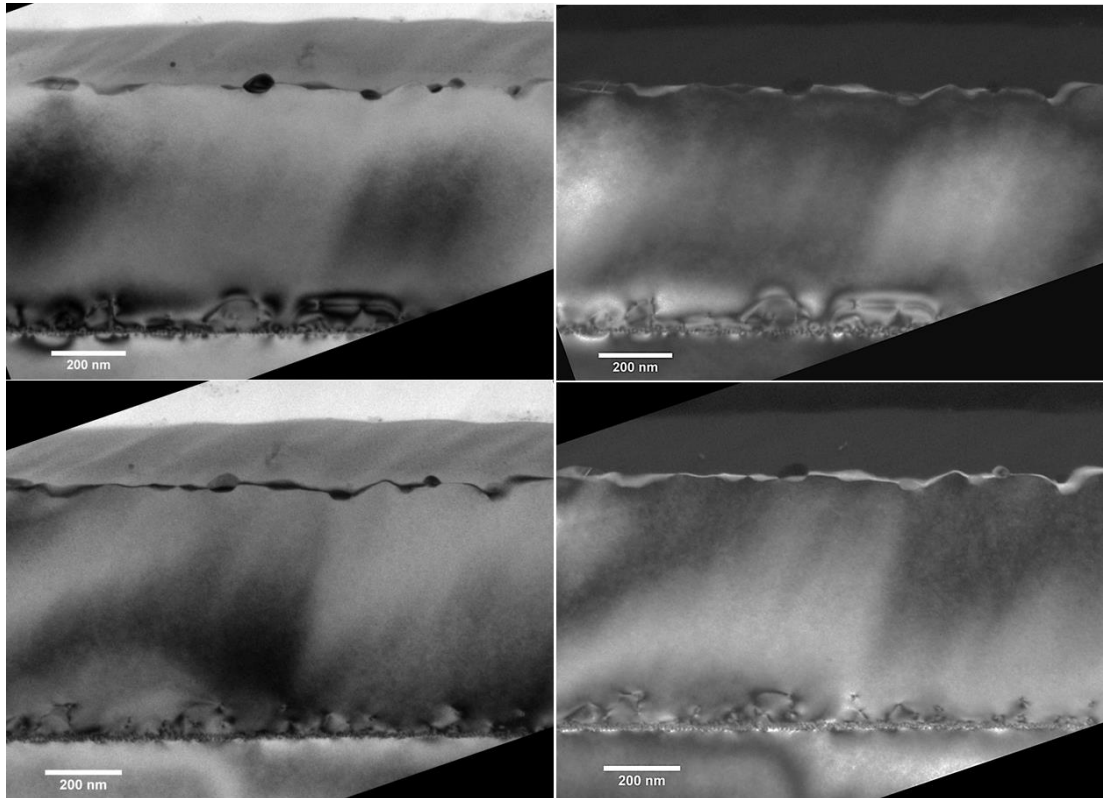
Figure 5-15 TEM micrographs of a $Ge_{0.95}Sn_{0.05}$/Ge/Si sample after undergoing the thermal treatment process up to 600 °C. (top left) bright field in (004) diffraction condition. High contrast material is clearly visible at epilayer/buffer interface. (top right) the same region of the sample in the (004) diffraction condition in dark field. The epilayer shows little contrast, indicating it is non-crystalline. (bottom left) bright field in (220) diffraction condition. (bottom right) and same region in dark field in (220) diffraction condition. Both bottom images show strong signal from the epilayer/buffer interface, indicating the area is highly defective.

number features supports the assertion that beyond the critical temperature Sn segregates out of the $Ge_{1-x}Sn_x$ alloy lattice.

Figure 5-15 shows TEM micrographs from $Ge_{0.95}Sn_{0.05}$/Ge/Si after thermal treatment up to 600 °C, for the (004) and (220) diffraction condition in both bright field and dark field contrast. The epilayer is clearly observable in the bright field contrast, with a rough surface. In the dark field images, the epilayer has a very low contrast, but it is discernible from the vacuum, indicating that the epilayer has become amorphous. This loss of layer crystallinity is attributed to the formation of GeSn-oxide by

incorporation of atmospheric oxygen into the GeSn layer at the surface and thermally driven diffusion of oxygen atoms into the layer.

The epilayer-buffer interface is far less well defined than typically observed in as-grown samples (Figure 4-15). Additionally, there are structures of high atomic number material observable at the interface, which is likely to be segregated Sn from the epilayer. The roughening of the interface is probably due to Sn atoms from the epilayer diffusing into the Ge buffer, forming a graded alloy region, which subsequently oxidises at elevated temperatures.

That the Sn-rich volume is confined to the interface in the lower Sn fraction epilayer is in contrast to what is observed for the $Ge_{0.893}Sn_{0.107}$ epilayer, shown in Figure 5-14, where the Sn-rich volume extends from below the epilayer/buffer interface to the epilayer surface. This difference is further evidence of a different response to thermal treatments between moderate and high Sn fraction $Ge_{1-x}Sn_x$ epilayers.

5.2.6 Alloy Composition, Epilayer Thickness and Strain State Effect on Critical Temperature

Sn fraction (at. %)	Epilayer thickness (nm)	Critical Temperature (°C)
9.2	70	310
9.2	50	310
9.1	40	-
8.5	35	-
10.5	40	275

Table 6 The critical temperatures, or lack thereof, of four $Ge_{1-x}Sn_x$ epilayers with approximately the same Sn fraction and an $Ge_{1-x}Sn_x$ epilayer with higher Sn fraction for comparison. For the ~9 at. % Sn epilayers with a thickness of 35 and 40 nm no critical temperature was observed. The 50 and 70 nm thick epilayers both exhibited a critical temperature behaviour, with the last stable temperature occurring at 310 °C. The 40 nm 10.5 at. % epilayer has a critical temperature of 275 °C.

By examining multiple samples with fully strained epilayers that were of a similar Sn fraction, ~9 at. %, but of a different thickness we can get initial data regarding the effect of epilayer thickness on thermal stability. Increasing the thickness of a strained layer increases the epilayer strain, but without behavioural contributions from any lattice defects, which are discussed later. A summary of the strained epilayer results is shown in Table 6. For both the 50 nm and 70 nm thick epilayer samples the critical temperature was determined to be 310 °C. For the thinner layers, 35 and 40 nm, no critical temperature exists. For these thinner epilayer samples the XRD results indicate a gradual degradation of the epilayer at temperatures well in excess of the critical temperatures of the thicker layers. It is apparent that the initial layer stress is vital for the existence of the critical temperature.

For the thicker samples despite the increase in epilayer thickness from 50 to 70 nm, the critical temperature does not change. This may indicate that once a threshold layer strain is reached, subsequent increases in layer strain do not contribute to the degradation mechanism and it is other factors which influence the critical temperature.
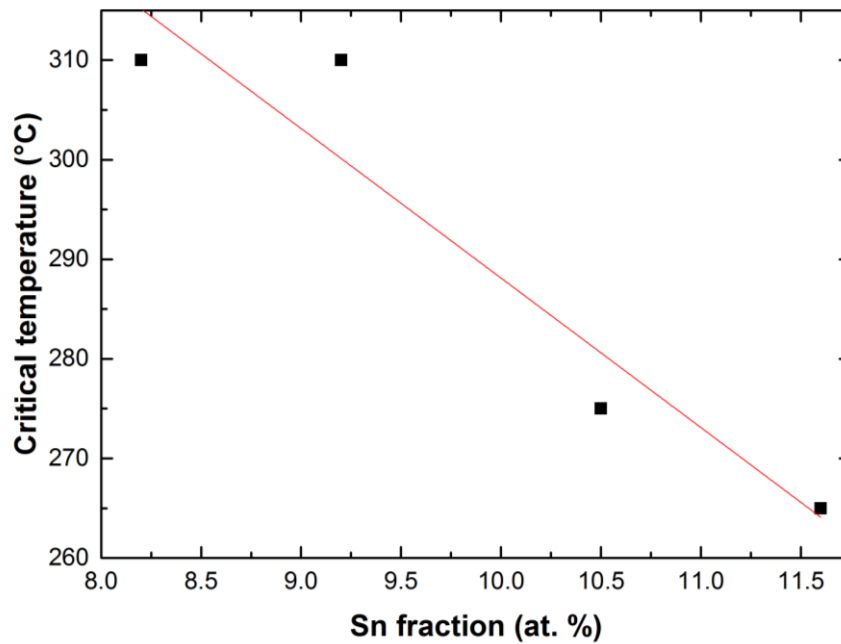
Figure 5-16 The variation of critical temperature with $Ge_{1-x}Sn_x$ epilayer Sn fraction. The trend is a decrease in critical temperature with increasing Sn fraction of the epilayer, as expected thermal stability increases with a more Ge like alloy. Note that samples investigated with a 6 at. % Sn epilayer displayed no critical temperature despite one being 'predicted' by extrapolation to exist at 350 °C, which would have been well within the investigated temperature range.

It should also be noted, that unlike the strained 40 nm 9.1 at. % epilayer, the fully strained 40 nm 10.5 at. % Sn epilayer does exhibit a critical temperature behaviour. Therefore the layer thickness is not the sole influence of whether a critical temperature behaviour is observed, rather for high Sn fraction alloys the Sn fraction influences the critical temperature. This difference in behaviour between the $x = 0.091$ and $x = 0.105$ epilayers may be explained by the increased lattice stress of the $Ge_{0.895}Sn_{0.105}$ epilayer due to the increased $Ge_{1-x}Sn_x$:Ge lattice mismatch and due to the $x = 0.105$ alloy being further from equilibrium composition.

Figure 5-16 confirms the behaviour, that increasing the Sn fraction of $Ge_{1-x}Sn_x$ alloy epilayers decreases their thermal stability. A simple linear fit of the data produces the relation given in equation 5-1

$$T_{critical} = 440 - 15x \qquad\qquad 5\text{-}1$$

where $T_{critical}$ is the epilayer critical temperature, the threshold temperature beyond which the crystallinity rapidly degrades, and x is the Sn fraction of the $Ge_{1-x}Sn_x$ epilayer in at. %. However, this equation is based on data from only four samples with epilayers of varied thickness and degree of strain relaxation and restricted Sn compositions, thus the reliability is not great. For a more reliable relationship, more samples with a wider range of epilayer compositions and with the same layer thickness are required.

While $Ge_{1-x}Sn_x$ layers of 6 at. % Sn have been demonstrated not to have a critical temperature, layers with 9 at. % do have a critical temperature; alloys with intermediate compositions still require investigation. This will both provide a wider range of alloy compositions to determine a more accurate relationship between critical temperature and composition, but will also help pinpoint the Sn fraction threshold at which $Ge_{1-x}Sn_x$ layers begin to display a critical temperature.

From the current data it can be predicted that $Ge_{1-x}Sn_x$ alloys with a Sn fraction of ~27.5 at. % would be unstable at room temperature (~30 °C) and that ~12.5 at. % Sn alloys would be unstable at typical growth temperatures ~250 °C. However, publications have demonstrated Sn fractions in excess of this limit, but this trend of increasing thermal instability may be indicative of an upper limit to the Sn fractions that can be achieved without further reductions in the growth temperature [15,131].

When comparing the 10.5 at. % Sn and 11.6 at. % Sn epilayer samples, the difference in critical temperature of 10 °C is appears to match the wider trend of the alloy composition range, see Figure 5-16. This is despite the 11.6 at. % epilayer is partially relaxed, 18.8% relative to the Ge buffer, with misfit dislocations at the $Ge_{0.884}Sn_{0.116}$/Ge interface whereas the 10.5 at. % epilayer is fully-strained. This

indicates that the layer thermal instability is not strongly effected by lattice defects to the extent present in this sample.

In summary, the existence of a critical temperature for high Sn fraction $Ge_{1-x}Sn_x$ epilayers has been demonstrated, with a different behaviour shown for low Sn fraction alloys. The value of the critical temperature at which rapid material degradation occurs has been determined for several samples with a range of material parameters, and has been shown to be a complex function of the epilayer Sn fraction and the layer thickness.

5.3 *Thermal stability study at a Synchrotron*

5.3.1 Motivation

In the previous lab based thermal stability studies the achievable sample conditions were limited to atmosphere. By using the facilities at a synchrotron, the thermal treatment of $Ge_{1-x}Sn_x$ alloy epilayer samples can be studies in an oxygen free environment, thus eradicating the effects of layer oxidation during the thermal treatment. To prevent the potential incorporation of any other atmospheric contaminates, this study uses a cryostat to create a vacuum-like environment for the sample during the thermal treatment while still allowing *in-situ* measurements.

By using a 2D detector the maximum intensity of the Bragg peak is captured even if the epilayer shifts due to epilayer lattice relaxation, by measuring the intensity of a slice through 2θ and χ. This allows for the detected epilayer Bragg peak intensity to more closely relate to the material properties during the thermal treatment. The synchrotron also has significantly higher incident x-ray beam intensity allowing for quicker measurements and better counting statistics.

It is also desirable to investigate the strain relaxation of Ge$_{1-x}$Sn$_x$ layers *in-situ* with the temperature treatment, which is not practical with a lab based X-ray diffractometer as individual RSMs require too much measurement time. These problems can be overcome with a synchrotron, which has improved peripheral equipment. This is not covered in this work, but could be investigated with a similar methodology.

5.3.2 Experimental Details

A range of Ge$_{1-x}$Sn$_x$ epilayer samples were investigated, all of a Ge$_{1-x}$Sn$_x$/Ge/Si(001) structure, with a range of Sn fractions, layer thickness and initial epilayer degrees of strain relaxation. These samples were also investigated in the preceding lab based thermal treatment with *in-situ* XRD study, allowing for direct comparison of the results between the two methods.

The samples were loaded into the high-temperature cryostat as described in chapter 3 of this work. The sample environment was then evacuated with a vacuum pump, leaving the samples is a moderate vacuum environment during measurements with the atmosphere being the helium cryogen. Hence, in contrast to the lab based study in the previous section, the samples investigated in the high temperature cryostat are in an oxygen free environment.

The diffractometer configuration was then calibrated at room temperature, with the sample Si substrate, Ge buffer and Ge$_{1-x}$Sn$_x$ epilayer symmetric (004) and asymmetric (224) Bragg peak reflection angles identified. The sample was then cooled to base temperature of ~20 K, and the temperature was stabilised for approximately 1 hour. This long stabilization time at a temperature below the measurement temperature is to ensure the cryostat cold head is as cold as possible, as

this limits the maximum temperature which can be investigated, as the excessive cold head temperatures end the experiment.

The sample was then heated to 200 K and 300 K with measurements at each temperature. Subsequently, the sample was investigated at more regular temperature intervals, initially with 20 °C increments at lower temperature range followed by 5 °C increments at higher temperatures, again with measurements at each temperature. The 20 °C temperature increments were used at lower temperatures as the layers are known to be stable at these temperatures from previous investigations. The smaller temperature increments were used as sample temperature approached temperatures at which interesting behaviour had previously been observed for each sample.

At each temperature the Si, Ge and $Ge_{1-x}Sn_x$ Bragg peaks in symmetrical (004) and asymmetrical (224) orientations were scanned over to measure main Bragg peak intensity, FWHM (indicative of crystallinity), omega position (for epilayer composition and thermal expansion).

5.3.3 Critical Temperature

The critical temperature is the threshold temperature beyond which sudden crystal degradation is observed, as detailed previously in this chapter. From previous investigations the expectation is for the $Ge_{1-x}Sn_x$ Bragg peak intensity to remain essentially constant with temperatures below the critical temperature, with some slight loss of intensity due to the increased thermal disorder of the crystal lattice, but without the loss interaction volume due to epilayer oxidation as observed with the Anton Paar study.

Figure 5-17 shows the temperature variation of the $Ge_{1-x}Sn_x$ Bragg peak intensity for samples with ~9 at. % Sn alloy epilayers of a range of thicknesses, each fully strained to the Ge buffer. A critical temperature is observed for 40 and 70 nm thick $Ge_{0.909}Sn_{0.091}$ epilayer samples, but not for the $Ge_{0.908}Sn_{0.092}$ 50 nm epilayer sample. The 40 nm epilayer has a critical temperature of 282 ± 5 °C, the 70 nm epilayer has a critical temperature of 307 ± 5 °C.

Similarly, Figure 5-18 shows the $Ge_{1-x}Sn_x$ Bragg peak intensities from several samples with a range of Sn fractions $Ge_{1-x}Sn_x$ alloy epilayers fully strained to the Ge buffer. The $Ge_{0.942}Sn_{0.058}$ 70 nm epilayer sample does not display a critical temperature. The $Ge_{0.909}Sn_{0.091}$ and $Ge_{0.894}Sn_{0.106}$ epilayers, both 40 nm thick, display critical temperatures of 282 ± 5 °C and 288 ± 5 °C, respectively. The only significant difference in the material properties of these two samples is the Sn fraction, but the critical temperatures are similar. However, unlike the $Ge_{0.909}Sn_{0.091}$ sample the $Ge_{0.894}Sn_{0.106}$ sample also shows a parasitic peak – as seen in the lab based study. This peak appears at the same temperature as the critical temperature for the main $Ge_{0.894}Sn_{0.106}$ peak, shown by the blue line.

Shown in Figure 5-19 are the $Ge_{1-x}Sn_x$ Bragg peak intensity results of a fully strained $Ge_{0.894}Sn_{0.106}$ epilayer sample and the partially relaxed $Ge_{0.884}Sn_{0.116}$ epilayer sample. These show a critical temperature of 288 ± 5 °C and 315 ± 10 °C, respectively. The significant material properties between these samples is that the $Ge_{0.884}Sn_{0.116}$ epilayer sample has a thicker epilayer and has existing lattice defects at the epilayer-buffer interface. The combination of these two factors appears to increase the critical temperature of the partially relaxed epilayer sample. Both of these samples show a parasitic peak, appearing at the critical temperature for the main $Ge_{1-x}Sn_x$ peak. This lower intensity peak, which is attributed to a lower Sn fraction alloy is seen here for

multiple samples when using the synchrotron set-up. This demonstrates that the parasitic peak, along with the critical temperature is not a oxidation driven process, as both a repeatedly seen in the absence of oxygen during the thermal treatments.

Comparing these results to those obtained using the Anton Paar stage, the critical temperatures of samples under vacuum vary from those under atmosphere, critical temperature is observed to both increase and decrease for samples. This is indicative of other factors influencing the critical temperature. This is supported by some samples which do not show a critical temperature in atmosphere, do under vacuum, as for the 40 nm $Ge_{0.916}Sn_{0.084}$ epilayer. Conversely some samples which have a critical temperature in atmosphere don't under vacuum as for the 50 nm $Ge_{0.918}Sn_{0.082}$ epilayer sample.
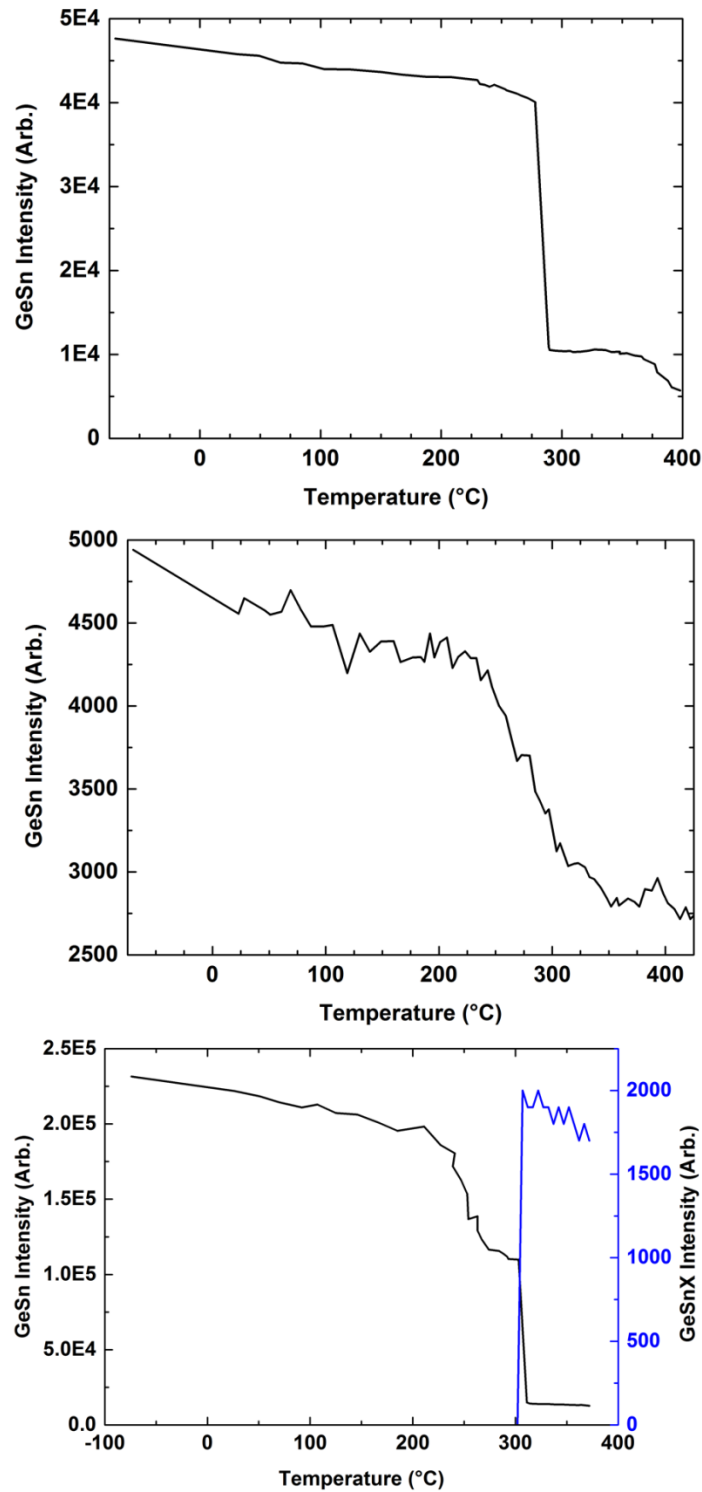
Figure 5-17 GeSn epilayer Bragg peak intensity vs. sample temperature.
(top) 40 nm thick $Ge_{0.909}Sn_{0.091}$ (centre) 50 nm $Ge_{0.908}Sn_{0.092}$ (bottom)
70 nm $Ge_{0.908}Sn_{0.092}$, with the parasitic peak shown as the blue line
appearing as the main $Ge_{1-x}Sn_x$ peak intensity has decreased. All epilayers
are fully strained to the Ge buffer.
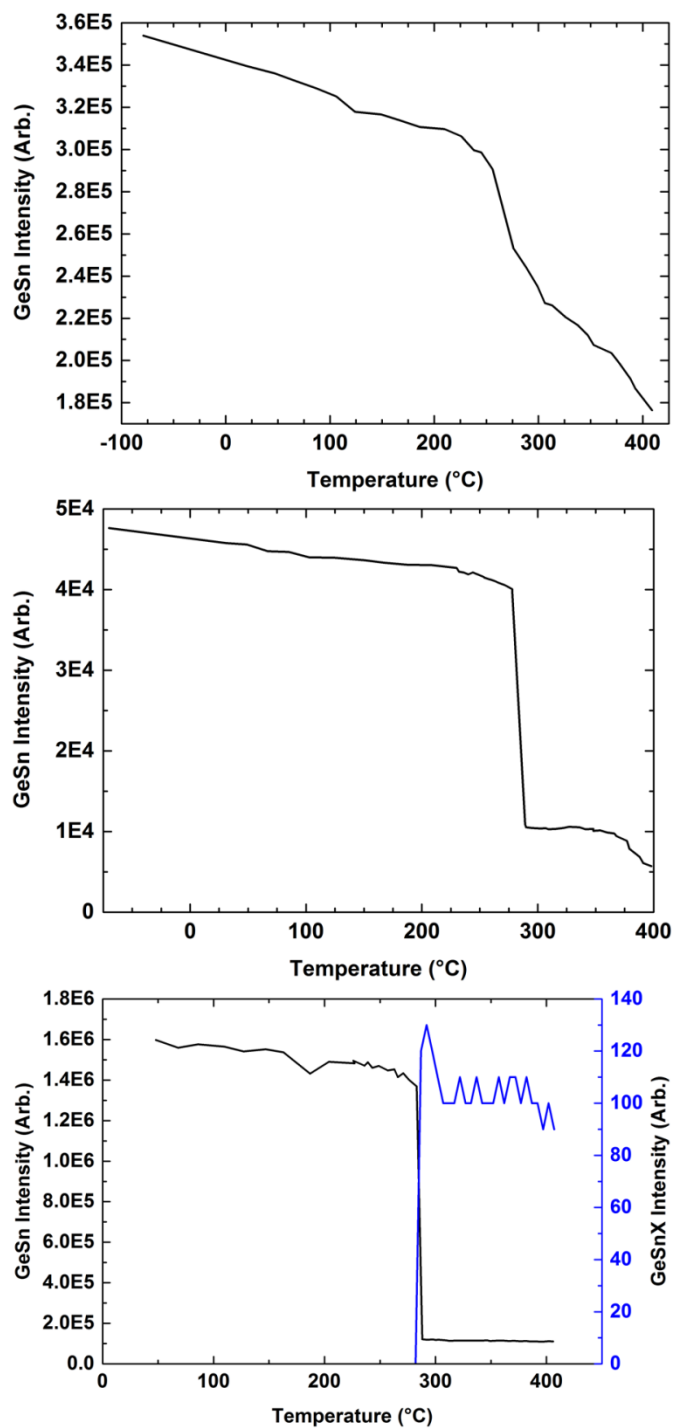
Figure 5-18 GeSn Bragg peak sum signal. (top) $Ge_{0.942}Sn_{0.058}$ 70 nm (centre) $Ge_{0.909}Sn_{0.091}$ 40 nm (bottom) $Ge_{0.894}Sn_{0.106}$ 40 nm, with the blue line indicating the parasitic peak intensity.
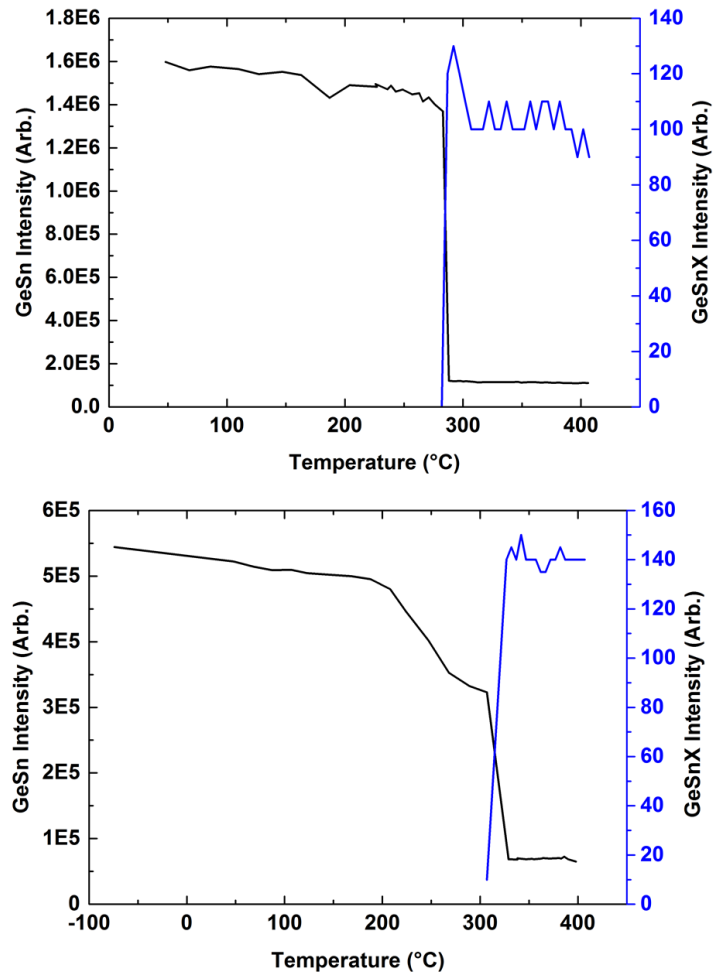
Figure 5-19 (top) fully strained $Ge_{0.894}Sn_{0.106}$ epilayer (bottom) Partially relaxed, R=19% relative to the Ge buffer $Ge_{0.884}Sn_{0.116}$ epilayer. The blue lines indicate the intensity of the parasitic peaks which appear at the critical temperature for both samples.

5.4 Oxidation

When exposed to atmosphere for prolonged periods, semiconductors develop a native oxide on their exposed surface. This native oxide is typically only a few nanometres thick, as seen in this work in the SIMS profiles of the ternary $Si_yGe_{1-x-y}Sn_x$ epilayer samples in section 7. The native oxide is amorphous and therefore unsuitable for subsequent growth of crystalline layers, therefore it is removed from Si and Ge substrates prior to sample growth. For both MBE and CVD, the oxide is chemically removed along with other surface contaminates using a series of wet chemical washes and pre-growth bake.

Another mechanism for inducing surface oxidation is heating samples in atmosphere or in another oxygen rich environment. The oxide is formed by oxygen incorporation at the surface and thermally enhanced oxygen diffusion into the sample, allowing thermally generated oxides to penetrate deeper into the layer than a native oxide developed on the surface at ambient temperature.

Semiconductor oxide layers have several applications, a thin oxide layer on a semiconductor can be used to protect the underlying semiconductor from the environment. Oxides have different dielectric constants than their semiconductor counterparts and can also be used to enhance metal contact properties, and this property has been utilized to enhance FETs devices, with germanium-tin-oxides currently undergoing investigation [135,136].

Germanium oxide is the closest starting point to investigate Ge-rich germanium-tin-oxides. Germanium oxide has applications as a semiconductor device dielectric in CMOS technology [137]. Germanium oxide layers can be formed by the controlled thermal oxidation of Ge, which requires high temperatures in an oxygen-rich environment, and this method is used to produce thin oxide layers [138].

The oxidation of pure Sn has also been investigated in published works. Tin has two common oxides, SnO and SnO_2, which are used as thin coatings on glass and other applications [106,139]. Sn oxides can be formed by the direct combustion of tin metal or in a more controlled manner using CVD, typically using $SnCl_4$ as the precursor, which is the same as used in this work for the tin source.

In this work $Ge_{1-x}Sn_x$ epilayers have been oxidized using the Anton Paar XRD temperature controlled stage, discussed in the previous section, to produce germanium-tin-oxide layers. This oxidation process uses sample heating in atmosphere, where the oxygen concentration is significantly lower than typically reported in published work studying the thermal oxidation of pure Ge.

Despite Sn atoms being a minority component of the $Ge_{1-x}Sn_x$ epilayer, they may facilitate the incorporation and diffusion of atmospheric oxygen atoms into the layer at an enhanced rate relative to oxygen diffusion in pure Ge.
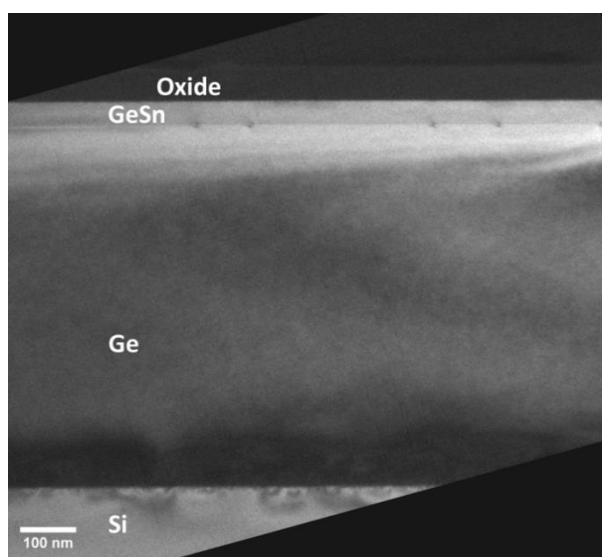

Figure 5-20 XTEM image of $Ge_{0.94}Sn_{0.06}$ post analysis on the XRD temperature controlled stage. The highest temperature the sample was taken to was 430 °C. Observable is that the crystalline GeSn layer has reduced thickness with the upper layer becoming amorphous (oxide). Also observable is an increase in dislocations at the GeSn/Ge buffer interface which indicate crystal relaxation.

As the thermal treatments on the Anton Paar temperature controlled XRD stage were carried out in atmosphere at very high temperatures, oxide layers were formed. While the $Ge_{0.884}Sn_{0.116}$ epilayer annealed at 290 °C showed little evidence of oxide formation (see TEM image in Figure 5-14 above), samples subjected to higher temperatures did show oxide layer formation.

Figure 5-20 shows a $Ge_{0.94}Sn_{0.06}$ epilayer sample after a thermal treatment with a maximum temperature of 430 °C. A representative selection of XRD rocking curves obtained during the thermal treatment of this sample are shown in Figure 5-12. In the TEM image it can be seen that the remaining crystalline $Ge_{1-x}Sn_x$ layer is thinner than prior to the thermal treatments, this result is in agreement with the change in XRD $Ge_{1-x}Sn_x$ Bragg peak thickness fringe separation. Above the remaining crystalline layer is a layer of amorphous material, an oxide of GeSn. The combined thickness of the oxide and remaining crystalline layer are in excess of the thickness of the initial crystalline layer. The oxide layer itself has a smooth surface and has a well-defined interface with the remaining crystalline $Ge_{1-x}Sn_x$, to the extent that XRD thickness fringes are still observed.

This has shown that for intermediate Sn fraction $Ge_{1-x}Sn_x$ alloy epilayers, thermal oxidation in atmosphere can be used to produce relatively thick oxide layers. The remaining crystalline material retains its high quality and the interface between the oxide and the crystalline alloy is very smooth. The oxide thickness is controllable with temperature and thermal treatment duration. The oxide growth rate is of the same order as that of pure Ge, though precise rates cannot be determined from this work. However, thermal oxidation of higher Sn fraction $Ge_{1-x}Sn_x$ alloys may be challenging, as the alloy segregates prior to the formation of an oxide. Further investigation is required to find out if oxides can be formed of the high Sn fraction

alloys using more favourable conditions, such as a longer duration anneal below the critical temperature in a more oxygen-rich environment.

5.5 Summary

The thermal stability of $Ge_{1-x}Sn_x$ epilayer samples has been investigated with *in-situ* XRD measurements and *ex-situ* TEM and AFM to investigate the changes of the epilayer.

Thermal treatments in standard atmosphere have been shown to oxidise the $Ge_{1-x}Sn_x$ surface at a comparable rate to that for pure Ge layers.

A critical temperature was observed for high Sn fraction alloys, Sn fraction ≥9 at. %, when thermally treated in atmosphere. Above this temperature the crystallinity of the epilayer degrades dramatically. For lower Sn fraction alloys, the epilayer degrades smoothly with temperature.

For samples which have a critical temperature, above the critical temperature Sn segregates out of the epilayer lattice to form large surface dots with trails; as the temperature increases further these dots decrease in size but increase in surface density; the segregated Sn goes from the epilayer surface and penetrates slightly into the Ge buffer. For lower Sn fraction alloys which do not have a critical temperature, the epilayer topology of the oxide post-treatment is similar to the as-grown material. Sn does segregate out of the epilayer lattice, but is confined to the oxide-buffer interface.

A critical temperature of epilayer stability is still observed with many samples in the synchrotron investigation, when the sample environment was free from oxygen. Curiously, a critical temperature is not observed for a sample for which a critical temperature was observed in lab based investigations. This disparity in result could

be attributed to the change in sample environment, undergoing thermal treatment at low pressure and in the absence of oxygen during the synchrotron study.

6 Electrical Contact Formation

The study of the formation of electrical contacts to $Ge_{1-x}Sn_x$ epilayers is a logical extension of the previous thermal stability study. Thermal treatments are commonly utilized to form Ohmic contacts and for other device processing steps of semiconducting materials. Part of the motivation for investigating the thermal stability limits of $Ge_{1-x}Sn_x$ is to determine the implications for the thermal limits for processes used in order to form Ohmic contacts to the alloy.

Standard methods of Ohmic contacts formation with Si and Ge use temperatures in excess of what $Ge_{1-x}Sn_x$ is stable to [140], therefore investigating Ohmic contact formation on $Ge_{1-x}Sn_x$ epilayers requires investigating a lower annealing temperature regime.

Current-voltage (IV) measurements from a range of contact spacings on TLM devices were used to investigating the effect of different contact materials, varying $Ge_{1-x}Sn_x$ epilayer composition, degree of epilayer strain relaxation, and extent of device thermal treatments.

6.1 Interpreting Results

The raw data consists of current-voltage sweeps, example plots are shown in Figure 6-1 from a $Ge_{0.884}Sn_{0.116}$/Ge/Si sample with a partially relaxed epilayer using Al contacts. The results displayed are from a range of contact spacings and for samples subjected to a range of thermal treatments. From these it can be observed that the plots become increasingly linear with annealing, i.e. increasingly Ohmic, especially at largest measured contact spacing of 512 μm. The electrical resistance values used in these plots were determined from data in the region of 0 V.

For this sample a decrease in the contact resistance is observed with increased annealing temperature for all contact spacings. The device response becomes increasingly Ohmic with increasing annealing temperature. This effect is particularly significant at lower contacts spacings, where contact properties dominate, indicating that the thermal treatment is mostly affecting the contact. However, the magnitude of the reduction in resistance with annealing increases as the contact spacing increases. This indicates that the thermal treatment does not solely affect the contact but also the material. Therefore some decrease in material resistance is occurring with annealing, potentially evidence of crystal healing due to the thermal treatment. The electrical resistance results are summarised in Table 7.

	4 μm Spacing	32 μm Spacing	512 μm Spacing
As-grown	250 Ω	745 Ω	4,500 Ω
200 °C	220 Ω	590 Ω	4,110 Ω
300 °C	60 Ω	255 Ω	3,330 Ω

Table 7 The electrical resistence of a partially relaxed epilayer $Ge_{0.884}Sn_{0.116}$/Ge/Si sample with Al contacts for a range of contact spacings. Data was obtained from samples annealed at for 1 hour in a nitrogen environment for a range of temperatures.

6.2 Contact Metals

In this study a range of contact metals were investigated, aluminium (Al), gold (Au) and silver (Ag), capped with a thin layer of gold to prevent oxidation. All the metals were deposited by electron-beam evaporation, as described in chapter 3. The different metals investigated have different electrical and thermal properties, such as melting temperature and diffusion coefficient, which will have an impact on the formation of an alloy between the contact metal and the underlying semiconductor.
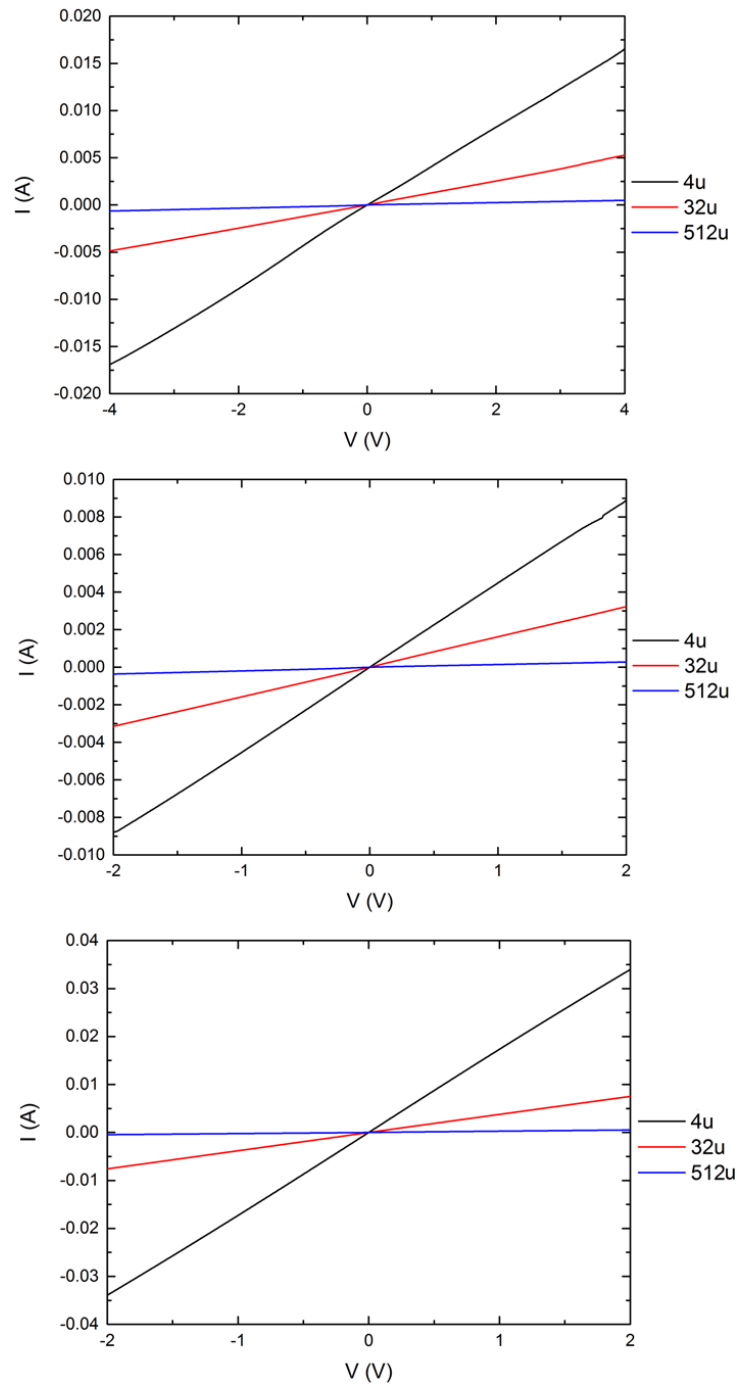
Figure 6-1 IV plots from $Ge_{0.884}Sn_{0.116}$/Ge/Si sample with Al contacts with TLM device. Shown are plots from 4 μm (black plots), 32 μm (red plots) and 512 μm (blue plots) contact spacings. The measured device was as-deposited (top), annealed at 200 °C (centre), or anneal at 300 °C (bottom). All device annealing was in a nitrogen atmosphere.

Figure 6-2 shows the results of this study, with the resistance vs spacing shown for a

range of epilayer compositions, for both as-deposited (solid lines) and after a thermal

treatment at 200 °C for 1 hour (dashed lines). The plot shows the results from aluminium, gold and silver contacts, from the upper plot downwards.

From inspection we can determine that aluminium contacts are the most affected by epilayer composition, with an increase in the Sn fraction of the $Ge_{1-x}Sn_x$ epilayers producing a decrease in the observed resistance at all spacings (apart from pure Ge which goes against this trend). Al contacts give the largest spread of contact resistance, predicted using the electrical resistance at the lower range of contact spacing. The contact resistance is anti-correlated with epilayer Sn fraction for all contacts. For $Ge_{1-x}Sn_x$ epilayers annealing is observed to generally reduce the resistance of Al and Au contacts.

With Au contacts, the epilayer Sn fraction has less impact on the electrical resistance than with other contact metals. Additionally, there is far less variation between profiles of the various samples with Au contacts than with the other contact metals. The contact resistance with Au samples are also consistently lower than with other contact metals; however, there is no clear relationship between epilayer Sn fraction and contact resistance or contact resistance. Annealing does appear to reduce the material resistivity and contact resistance of all samples, but not to a significant degree.

With the Ag contacts, we find a large spread of electrical resistance at small and large contact spacings. The effect of annealing on electrical resistance is inconsistent across the range contact spacings, resulting in observing both an increased and decreased resistance. It is possible that the thermal treatment is damaging the electrical contact quality. For the Ag contacts, the alloy Sn fraction has an inconsistent effect on measured resistance.
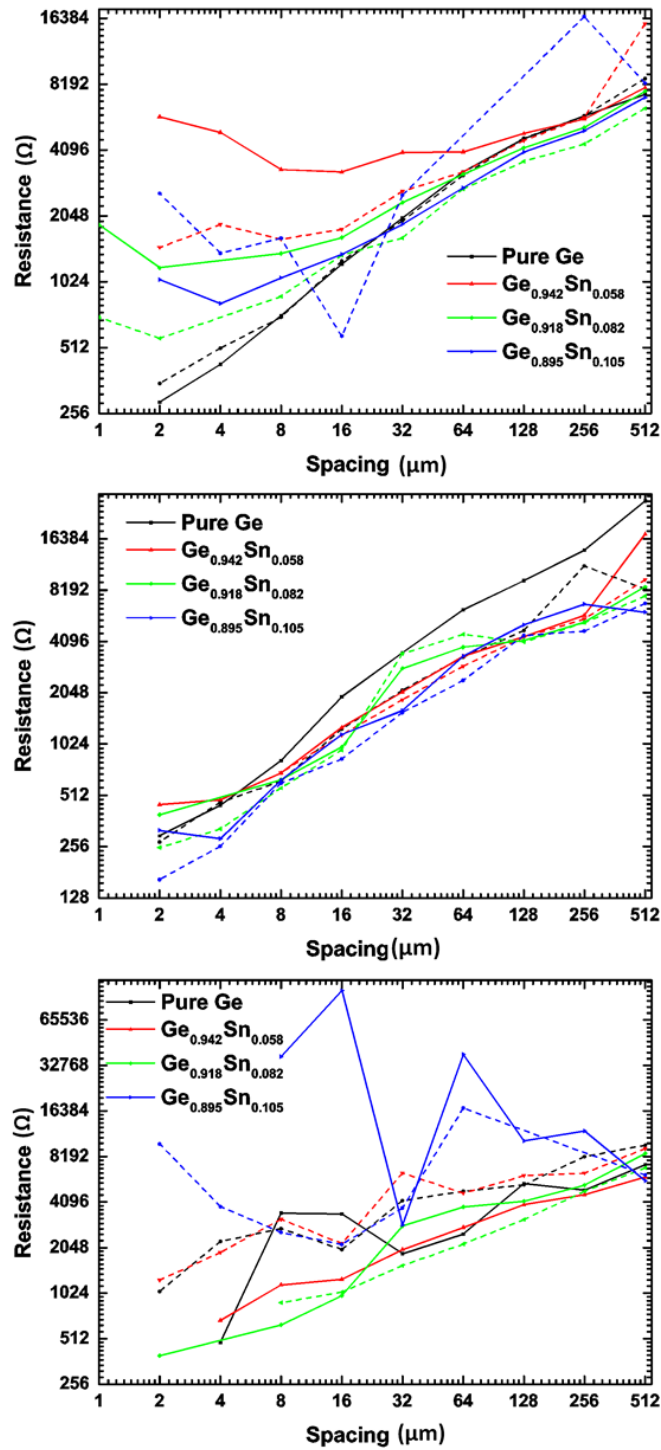
Figure 6-2 The electrical resistance with spacing between electrical contacts using (top) aluminium (middle) gold and (bottom) silver metal contacts for pure Ge and $Ge_{1-x}Sn_x$ epilayers for a range of Sn fractions. Both as-deposited deposited samples (solid line) and samples annealed for 1 hour at 200 °C (dashed lines) are shown. From inspection, gold contacts have the most consistently linear relation between contact spacing and resistance for all samples and the lowest contact resistance. On a log-log plot a linear relation such as an Ohmic contact should appear linear, with a gradient independent of semiconductor resistance.

By examining the contrast between the different contact metals the following conclusions can be drawn. Gold contacts produce the most consistent and reliable for different epilayer compositions and thermal treatments with the lowest contact. Further investigation is necessary for aluminium and silver contacts, potentially these contacts require very different treatments to produce an Ohmic response.

6.3 Annealing Metal Contacts

In this section the electrical properties of TLM structures with as-deposited metal contacts are compared to TLM structures which have been annealed. The samples were annealed at a constant temperature of either 200 °C or 300 °C for 1 hour in a nitrogen environment. Annealing was conducted in an inert environment to minimise any oxidation of the sample surface or metal contacts, using a tube furnace with a constant flow of high-purity nitrogen.

Annealing causes some atoms from a metal contact to diffuse into the underlying semiconductor epilayer, either Ge or $Ge_{1-x}Sn_x$, causing a localised alloying and therefore a less abrupt interface and reducing barriers to charge carrier flow. However, if the annealing temperature is too high there is a risk of damaging the $Ge_{1-x}Sn_x$ epilayer.

Figure 6-1 shows I-V plots from a $Ge_{0.884}Sn_{0.116}$ epilayer sample at a range of electrical contact separations for two annealing conditions. From these plots the I-V the gradient can be seen to change for all contact separations with increased degree of thermal treatment, indicating a decrease in the contact resistance.

The effect of annealing on both moderate, 5.8 at. %, and higher, 11.6 at. %, Sn fraction $Ge_{1-x}Sn_x$ alloy epilayer samples was also investigated. This range was chosen as earlier work indicates that an increased $Ge_{1-x}Sn_x$ Sn fraction increases its thermal

instability. The results of these investigates are shown in Figure 6-3, log-log plots have been used so that behavioural features over the entire range of contact separations can be discerned.

6.3.1 Contacts on intermediate Sn fraction layers

For the as-deposited intermediate Sn fraction epilayer sample (Figure 6-3, top panel, solid lines), both Ag and Au contacts have an approximately linear response, particularly at larger contact separation's. The same is not true for the Al contacts.

After a 200 °C anneal (dashed lines) the contact is altered. Au contacts have an increasingly linear response. The Al contact response becomes significantly more linear than observed from the as-grown sample, such that the Al contact now has a behaviour similar to that of the Au contact for separations ≥8 μm. However, the Ag contacts now have a less linear response than seen for the as-deposited sample, possibly indicating contact degradation, with higher electrical resistance at all contact spacings.

Increasing the degree of thermal treatment to a 300 °C anneal, the I-V response is further altered (dotted lines). The Au contact response becomes increasingly linear, and is now linear over the whole contact separation range, with a slight reduction in resistance across the entire range. By contrast, the Al contact samples display a less linear response than either as-deposited or 200 °C annealed samples, with the resistance increasing significantly at all contact separations.

Au contacts have a fairly constant contact resistance, with comparatively slight changes due to annealing compared to the other contact metals. Ag contacts show an increase in resistance when annealed at 200 °C, compared to as-deposited, at all

contact separations. Al contacts decrease in resistance when annealed at 200 °C, but resistance then increase with a 300 °C anneal.

6.3.2 Contacts on high Sn fraction layers

For the high Sn fraction partially relaxed epilayer, even without any thermal treatments, the I-V measurement results indicate the contacts are approximately Ohmic (Figure 6-3, lower panel, solid lines). Over the full contact spacings range, a predominantly linear relation between spacing and electrical resistance is observed for all contact metals.

When these samples are annealed at 200 °C for 1 hour (dashed lines), the behaviour of all contacts remains similar to the as-deposited samples. A slight reduction in resistance is observed for the larger contact spacings, which may be indicative of an improvement not in the contact but of slight crystal healing for this sample.

After 1 hour thermal treatment at 300 °C, the Al contacts appear to have an approximately linear relationship with spacing, whereas the Au contacts are less linear than the samples treated at lower annealing temperatures (dotted line). A decrease in resistance is observed when using the Al contact at all separations compared to lower annealing temperatures, in contrast to observations with moderate Sn fractions. At the largest contact spacing of 512 μm, both Al and Au contacts display an electrical resistance of ~3,300 Ω.

To compare the response to annealing TLM devices on lower Sn fraction with higher Sn fraction $Ge_{1-x}Sn_x$ epilayer samples we find several trends. The effect of annealing for both samples is not simple, but varies between contact metals.

For Al samples, the highest annealing temperature produces the lowest resistance for the higher Sn fraction sample, whereas an intermediate temperature is optimum for the intermediate Sn fraction sample.

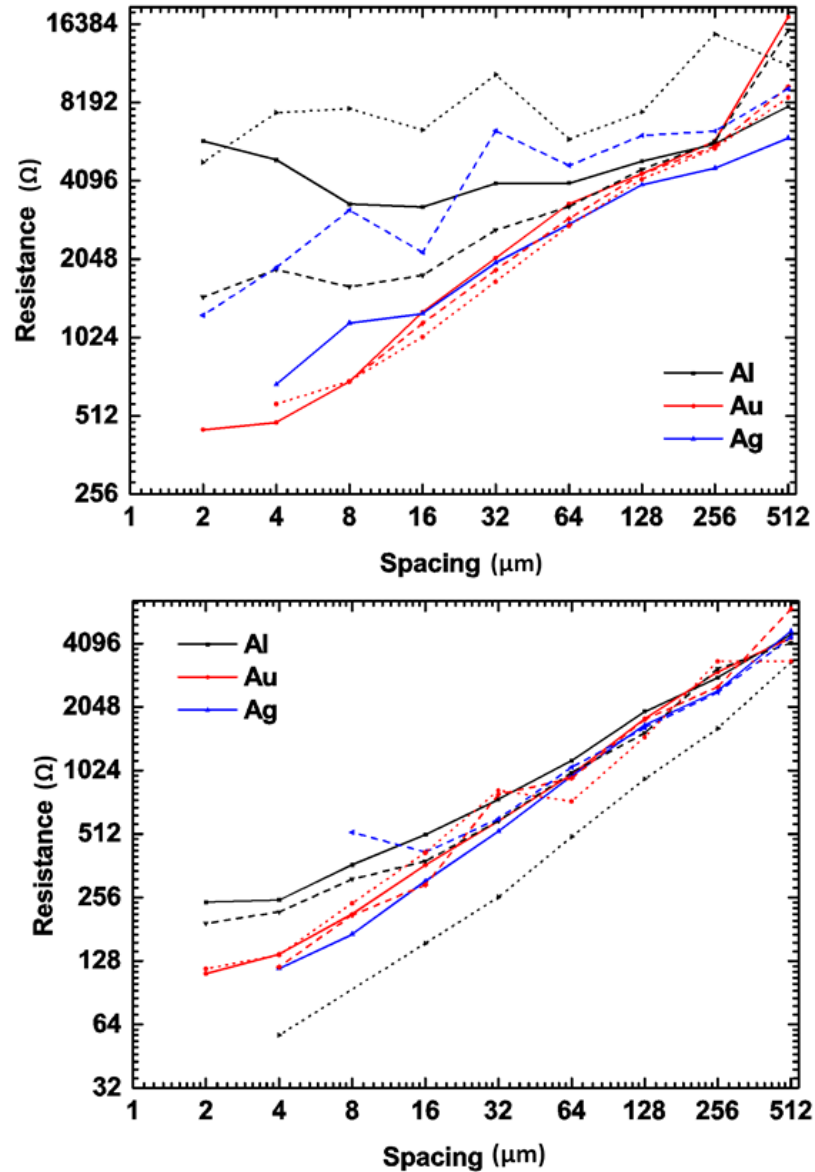Figure 6-3 The TLM electrical resistance as a function of contact spacing, displayed as log-log plots, with a range of contact metals on (top) fully strained epilayer $Ge_{0.942}Sn_{0.058}$/Ge/Si sample and (bottom) a partially relaxed epilayer $Ge_{0.884}Sn_{0.116}$/Ge/Si sample. Results are shown from the (full line) as-grown sample, (dashed line) annealed at 200 °C for 1 hr (dotted line) anneal at 300 °C for 1 hr.

A 200 °C anneal reduces the resistance of Al and Au contacts for both samples, but this is not the case for Ag contact samples which degrade by this treatment. The effect of a 300 °C anneal has a more mixed result for Au contacts, enhancing behaviour on lower Sn fraction $Ge_{1-x}Sn_x$ layers and degrading behaviour on higher Sn fraction alloy layers. From our previous thermal treatment study we know that 300 °C is close to critical temperature for the $Ge_{0.893}Sn_{0.107}$ sample. Changes in annealing conditions may alter the exact temperature. It is therefore possible that the different effect of the 300 °C treatment on higher Sn fraction alloys to lower Sn fraction alloys is due to degradation of the more thermally unstable samples. However, this requires further investigation before it can be confirmed.

6.4 Sn fraction

In this section the effect of $Ge_{1-x}Sn_x$ epilayer Sn fraction on the electrical properties of the devices is explored. The samples studied possess a fully strained $Ge_{1-x}Sn_x$ epilayer with a range of Sn fractions; a sample without the $Ge_{1-x}Sn_x$ epilayer, but with the contacts deposited directly onto the Ge buffer is included for comparison. Figure 6-4 shows I-V plots for Ge buffer, $Ge_{0.942}Sn_{0.058}$, $Ge_{0.918}Sn_{0.082}$ and $Ge_{0.895}Sn_{0.105}$ epilayer samples. Each plot shows Al (black), Au (red) and Ag (blue) contacts for as-deposited (solid lines) and after a 200 °C anneal for one hour (dashed line).

From these plots it can be observed, for all Sn fractions, that the resistance at the largest contact spacing, 512 μm, lies in the range of 5,000 - 8,000 Ω, for most contact metals. At the other extreme, at the typical smallest contact spacing of 2 μm, the pure
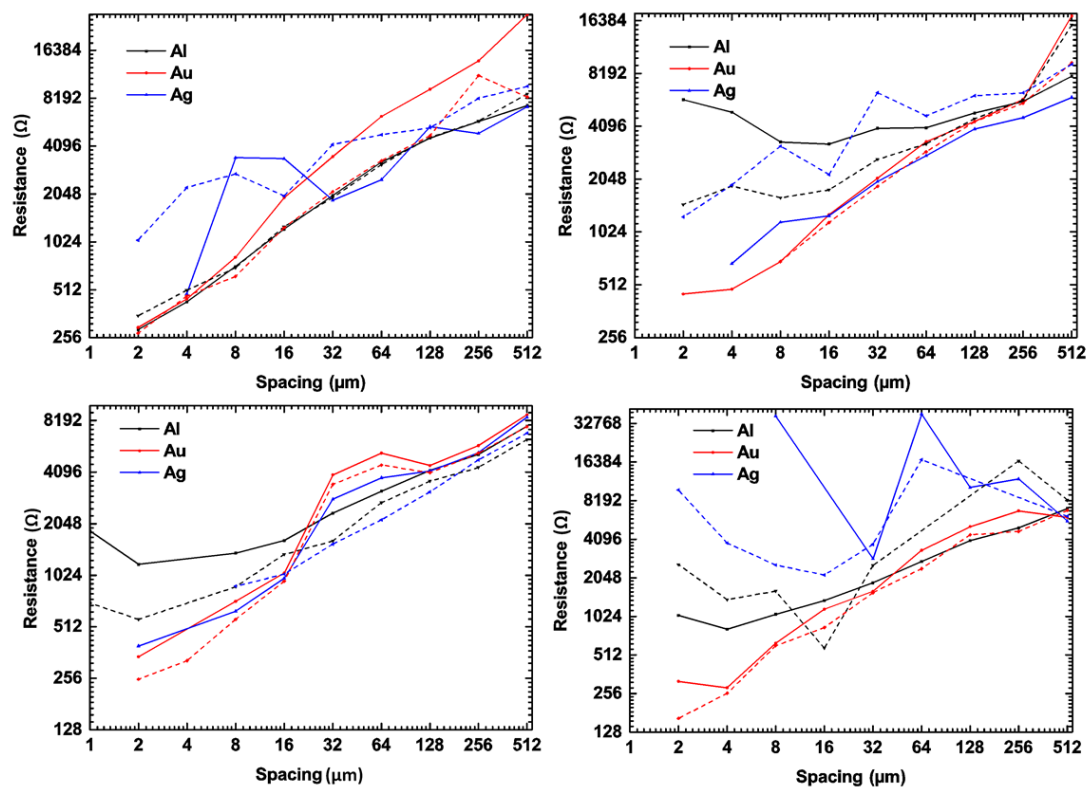
Figure 6-4 Electrical resistance as a function of contact spacings for a range of epilayer compositions. (top left) Pure Ge - with no $Ge_{1-x}Sn_x$ epilayer. (top right) $Ge_{0.942}Sn_{0.058}$ epilayer, (bottom left) $Ge_{0.908}Sn_{0.092}$ epilayer (bottom right) $Ge_{0.895}Sn_{0.105}$ epilayer. All $Ge_{1-x}Sn_x$ epilayers were fully strained. For all samples a range of contact metals was used, samples annealed at 200 °C are shown as dashed lines.

Ge and $Ge_{0.908}Sn_{0.092}$ samples have a similar resistance in the 250 - 500 Ω range for most contact metals, whilst the $Ge_{0.942}Sn_{0.058}$ and $Ge_{0.895}Sn_{0.105}$ samples have a wide range of values at this contact spacing. However, for both these latter samples Au contact measurements are within this range. So, in agreement with previous results, Au contacts provide the lowest contact resistance.

The $Ge_{0.918}Sn_{0.082}$ epilayer sample has the most consistent results for the different contact metals and thermal treatments. The $Ge_{0.942}Sn_{0.058}$ and $Ge_{0.895}Sn_{0.105}$ samples show significantly more spread in their results for variations in contact metal and thermal treatment, particularly at smaller contact spacings.

173

In an section [6.3], 5.8 and 10.6 at. % Sn $Ge_{1-x}Sn_x$ samples were subjected to two different thermal treatments. While here we again discuss contact annealing, briefly, the focus is on how the difference in epilayer composition determines the result of annealing, covering only one thermal treatment conditions, as-deposited and a 200 °C anneal for 1 hour.

For the pure Ge sample, annealing has little significant effect on the resistance of the sample with Al contacts, but consistently decreases the observed resistance when using the Au contact. Annealing the $Ge_{0.942}Sn_{0.058}$ sample decreases the observed resistance of the Al contact, has little effect for Au contact and has a negative effect for the Ag contact. For the $Ge_{0.918}Sn_{0.082}$ sample, annealing appears to systematically reduce resistance for all contact types and for essentially all contact spacings. For the $Ge_{0.895}Sn_{0.105}$ sample, the Au contact is not significantly affected and annealing has a mixed effect on both the Ag and Al contact samples. Due to the varied results for the range of samples, I conclude that the $Ge_{1-x}Sn_x$ composition does not dominate the effect of annealing for the treatments investigated, with other factors having a greater effect.

6.5 Strain Relaxation

In this section, the effect of the $Ge_{1-x}Sn_x$ epilayer strain relaxation on electrical properties of the TLM devices is investigated, and how strain relaxation impacts the effects of annealing. Samples were chosen to cover a range of $Ge_{1-x}Sn_x$ epilayer compositions. In each case, two samples of a similar alloy composition were studies with the epilayer in one being fully-strained and the other partially strain relaxed. The results from these samples are to be used to isolate the effect of strain relaxation on the electrical properties of the TLM devices for the range of contact metals

studied. The results are shown in Figure 6-5, with the solid lines denoting fully strained epilayer samples, dotted lines partially relaxed epilayer samples. The plots in the left column are from as-deposited devices and the right column samples annealed for 1 hour at 200 °C.
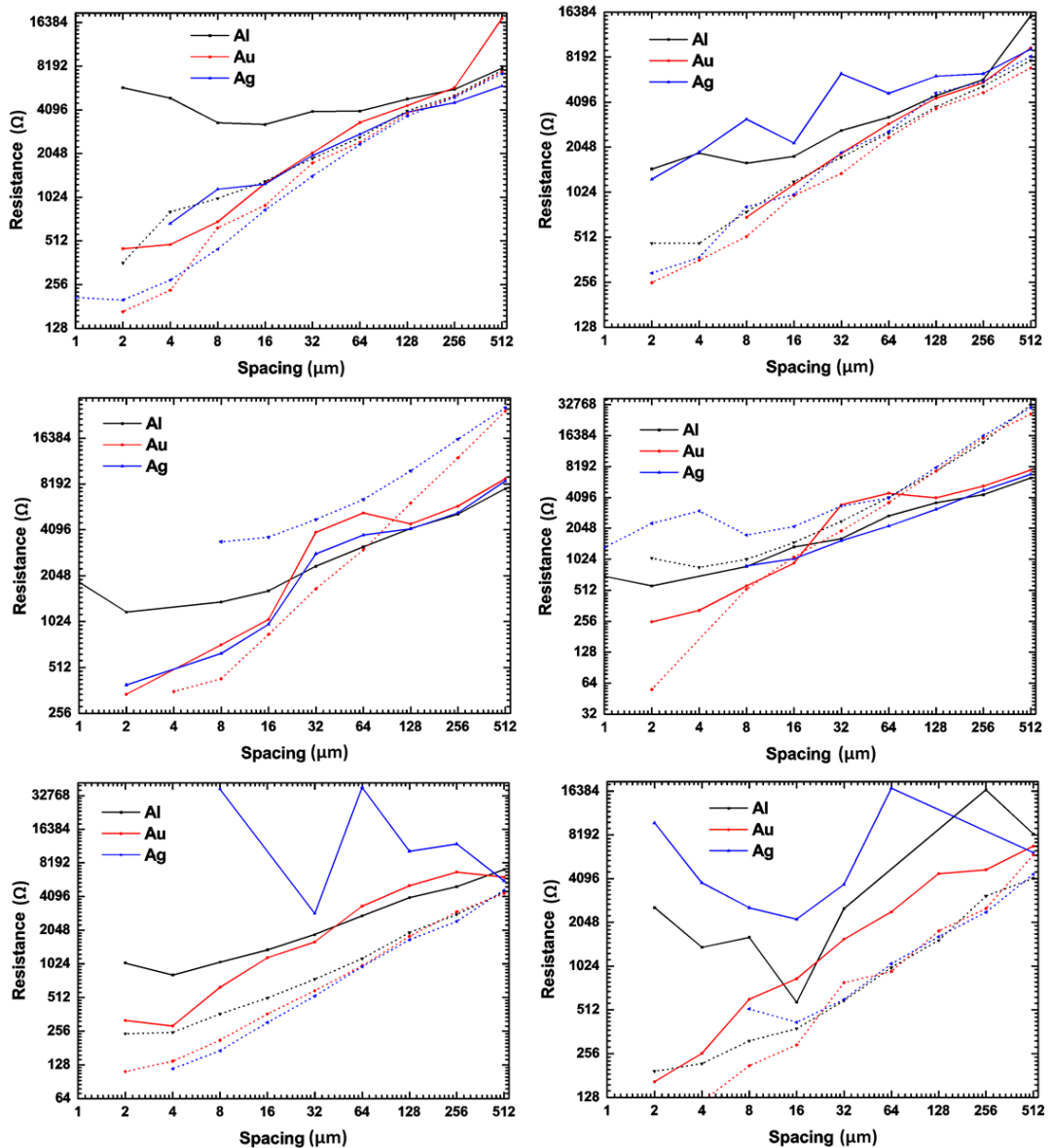

Figure 6-5 (Left column) As-grown samples, (right column) 200 °C annealed samples. (top row) ~5 at. % Sn epilayer samples, (middle row) ~9 at. % Sn epilayer samples, and (bottom row) ~10.5 at. % Sn. Solid line plots denote fully strained epilayer samples. Dotted line plots denote partially relaxed epilayer samples. The data is displayed as log-log plots.

Examining the samples with an Sn fraction of ~5 at. %, the relaxed epilayer samples have lower resistance, for both as-deposited and annealed samples. Additionally, the relaxed epilayer samples have a more consistently linear response across the full range of contact spacings, indicating either a higher contact or semiconductor electrical quality, a desirable trait.

Comparing the ~9 at. % Sn alloy samples, the relaxed epilayer samples have higher resistance, but possess a similar or increasingly linear response at larger contact spacing compared to the strained layer samples.

For the ~11 at. % Sn alloy samples, the relaxed epilayer samples have consistently lower resistance and show a more linear response to separation distance than strained layer samples.

For all alloy compositions the results consistently indicate a more linear response with partially relaxed epilayer samples. The resistance at a given spacing can be greater or smaller for strain relaxed samples.

6.6 Conclusions

Forming quality Ohmic contacts to $Ge_{1-x}Sn_x$ structures for consumer semiconductor devices should not pose a significant challenge, despite the low thermal budget available for processes due to the thermal instability of $Ge_{1-x}Sn_x$.

The properties of the electrical contact are influenced by contact metal, epilayer strain relaxation, thermal treatment and possibly $Ge_{1-x}Sn_x$ epilayer alloy composition. A significant amount of data is required to explore all of these variables in sufficient detail to draw confident conclusions.

Thermal treatments of contacts requires more investigation, including reducing the temperature interval between annealing temperatures and increasing the range of

annealing durations studied. However, improvements of contact quality have been observed with 200 °C anneal for 1 hour in an inert atmosphere. To identify to what degree this improvement is due to crystal healing and what from enhancement of the contacts, samples could be thermally treated prior to TLM device fabrication.

Strain relaxation in the epilayer has been observed to improve the quality if the electrical contacts, resulting in more Ohmic behaviour. It is also possible that lattice relaxation reduces the resistivity of the metal, but results are not conclusive. Strain relaxation may affect the diffusion of the contact metal atoms or it may be due to the bandstructure modifications from strain relaxation.

Au is the most stable contact type of those studied, whereas the Ag contacts used in this study where of a lower quality. It is possible that alternative device fabrication methods would improve Ag contact quality, but this itself is indicative of more complicated fabrication methods being necessary for Ag contacts. Au contacts consistently gave the lowest contact resistance, most linear behaviour and best behaviour without any thermal treatments.

7 Conclusions and further work

In this chapter, this work is concluded and possibilities for further work are discussed for each of the main areas of study presented in this thesis; the growth of thin strained and strain relaxed $Ge_{1-x}Sn_x$ layers, and in this section $Si_yGe_{1-x-y}Sn_x$ layers, studies of the thermal stability of $Ge_{1-x}Sn_x$ epilayers, and the formation of Ohmic contacts to $Ge_{1-x}Sn_x$ epilayer with a low thermal budget.

7.1 Conclusions

Samples of strained and relaxed $Ge_{1-x}Sn_x$ epilayers have been grown by RP-CVD onto Ge buffered Si substrates. The requirement for low growth temperatures has been confirmed, with a reduction in the growth temperature necessary for increasing the Sn fraction of the alloys. H_2 is determined to be superior to N_2 as a carrier gas during $Ge_{1-x}Sn_x$ growth, as using N_2 reduces the growth rate which reduces the attainable alloy composition and inhibits the production of high quality monocrystalline layers.

Growth on off-axis substrates requires re-optimization of the growth conditions, as using the growth conditions used with standard substrates produced lower quality $Ge_{1-x}Sn_x$ layers. However, even with additional optimization of the growth parameters there are issues with a reduced growth rate and the observation of polycrystalline growth, which suggest off-axis substrates will not be effective method for the integration of III-V semiconducting alloys onto Si platforms.

Thermal treatments of lower Sn fraction $Ge_{1-x}Sn_x$ layers are observed to degrade the material smoothly with increasing temperature. However, moderate and high Sn fraction alloys are observed to have a critical temperature, below this temperature the layers are essentially stable but above this temperature the crystal quality rapidly

degrades. This critical temperature is dependent on $Ge_{1-x}Sn_x$ epilayer Sn fraction, thickness and strain.

Aluminium, gold and silver metal contacts have been fabricated and tested on a range of $Ge_{1-x}Sn_x$ alloy epilayer samples. Of the metals tested, gold was the optimal contact material. A more Ohmic contact response was found for partially relaxed epilayer samples. Annealing was observed to improve the $Ge_{1-x}Sn_x$ crystal quality, even for low temperature anneals.

7.2 Further work

In this section the possibilities for extending this work and the direction of $Ge_{1-x}Sn_x$ research in the medium term future are discussed.

7.2.1 Increasing Sn Fraction

Further increases the Sn fraction of crystalline $Ge_{1-x}Sn_x$ alloy epilayers which can be reliably produced CVD are likely to continue as the field matures. The crucial factor to increasing the attainable Sn fraction is creating the conditions for a sufficiently high growth rate at the very low growth temperature. Increasing the maximum Sn fraction limit while maintaining a high $Ge_{1-x}Sn_x$ crystal quality has been an on-going challenge, especially as thick layers are commonly sought in order to induce strain relaxation of the layer.

Existing publications have explored using increasingly novel precursors to supply the Ge, and Si when growing the ternary alloy at these low temperatures, with higher order germanes giving promising results. The lower activation energy of these precursors means that the low thermal energy conditions during growth do not inhibit the growth rate to the same extent as more standard precursors. Whether similar

gains in growth rate can be obtained by altering the Sn gas precursor remains to be seen, a significant research effort was applied in the initial research of $Ge_{1-x}Sn_x$ growth by CVD to find a suitable Sn source, initially using SnD_4 and more recently $SnCl_4$. Thus, many of the most readily assessable potential Sn precursors have been already tested. It is important that any precursors for Ge and Sn are relatively cheap, easy to acquire and easy to store for moderate amounts of time both for research and for commercial scale production purposes.

7.2.2 Strained and Relaxed GeSn Layers

Increasing crystal lattice strain relaxation in $Ge_{1-x}Sn_x$ epilayers is an on-going effort, with all available avenues of research meeting significant challenges. The growth of thick $Ge_{1-x}Sn_x$ alloy layers in order to induce strain relaxation increases growth times and production costs, due to the small growth rate at the low growth temperatures. If a method which significantly increases the growth rate without significantly increasing the cost is identified, this would facilitate the production of thicker more strain relaxed layers. However, without any significant advances, using thick layers for strain relaxation remains an uneconomical option. In addition to this, very thick $Ge_{1-x}Sn_x$ layers have been grown which possess high Sn fraction and these layers still possess significant residual compressive strain [131]. This implies that layers significantly thicker than necessary for Ge relaxation on Si will be needed for complete strain relaxation of $Ge_{1-x}Sn_x$ epilayers. This can be attributed to the low growth temperature inhibiting atomic movement and the production of strain relieving lattice dislocations.

The high thermal sensitivity of the $Ge_{1-x}Sn_x$ layers makes thermal annealing or thermal cycling an unattractive option due to the degradation of crystal quality, particularly of high Sn fraction alloy layers.

Further development of $Ge_{1-x}Sn_x$ CVD growth methods, analogous to those developed for Ge in order to reduce crystal defects, with a low temperature seed layer proceeding a higher growth temperature layer [141], may be a possible route for increasing the degree of strain relaxation achieved in $Ge_{1-x}Sn_x$ layers. Potentially, inducing strain relaxation may be achievable by using graded structures, as is used for strain engineering and defect reduction with Si_yGe_{1-y} alloy layers [142]. For example using a partially relaxed higher Sn fraction alloy to act as a growth platform for a lower Sn fraction layer. These development routes do complicate growth, introduce limits to the thermal budget of the structure to that of the higher Sn fraction layer and also mean that the highest Sn fraction layers cannot be relaxed. However, it may be a more effective route than other strain relaxation methods.

7.2.3 Thermal Stability of GeSn

This work confirms the existence of a critical temperature for moderate and high Sn fraction $Ge_{1-x}Sn_x$. Further work is required in order to identify and investigate which properties influence whether a critical temperature exists for a particular alloy and at what temperature the material will degrade. This work has examined Sn alloy fraction, epilayer thickness, strain relaxation state and sample environment, but additional data is necessary to properly understand the relationship between these properties and the critical temperature.

To expand upon the progress made in this work, *in-situ* imaging of $Ge_{1-x}Sn_x$ layers during thermal treatments should be conducted; a study comparable to investigations

with *in-situ* XRD conducting in this work could be carried out. The hints of Sn segregation and change of surface features seen in this work are also seen in other works [66], but a comprehensive understanding of their evolution is desirable. These investigations should investigate the threshold parameters for lower Sn fraction alloys which display characteristically different behaviour, with no critical temperature. For example, investigations of very thick, low Sn fraction alloy layers to examine whether sufficient layer thickness causes a change in behaviour.

7.2.4 Electrical Contacts

Forming Ohmic contacts to high Sn fraction alloys is challenging due to the thermal instability of the alloy. However, it is frequently these high Sn fraction alloys which are desirable for devices. The identification of the critical temperatures of high Sn fraction alloys further cements the need for low temperature processing.

Therefore, future research should investigate and optimise the contact metals, annealing temperatures and annealing duration. In this work a single annealing time of 1 hour was used. The choice of annealing time will be required to balance being sufficiently low to be economical, but also produce a quality electrical contact.

7.2.5 SiGeSn

In the research field the ternary $Si_yGe_{1-x-y}Sn_x$ alloy has been investigated in tandem with the binary alloy, though progress has been slower due to the increased complexity of materials characterization and in some areas the need for foundational knowledge the binary alloy. The ternary alloy remains a promising area for future research. $Si_yGe_{1-x-y}Sn_x$ alloys are particularly of interest for device applications due to the lattice parameter and bandgap decoupling being of great potential for strain and bandgap engineering. However, this very characteristic complicates materials

characterization. The appropriately modified Vegard's law can be used to determine a unique lattice parameter and bandgap from a known ternary alloy composition [8]. However, it is not possible to use the same method to use a known lattice parameter to determine a unique composition and bandgap for an alloy.

7.2.5.1 Growth

The CVD growth of $Si_yGe_{1-x-y}Sn_x$ alloy epitaxial layers requires similar conditions to that of $Ge_{1-x}Sn_x$ binary alloy growth [69,79]. Specifically, low growth temperatures are still necessary for Sn incorporation. Due to the low growth temperatures disilane, Si_2H_6, is used as Si precursor source as the growth rate when using monosilane, SiH_4, is too low for effective Si incorporation into the alloy at an acceptable growth rate. As with binary $Ge_{1-x}Sn_x$ growth digermaine, Ge_2H_6, and tin-tetrachloride, $SnCl_4$, were used as the Ge and Sn sources, respectively, for $Si_yGe_{1-x-y}Sn_x$ alloy growth.

7.2.5.2 Characterization

Materials characterization of $Si_yGe_{1-x-y}Sn_x$ epilayers is challenging. Very low growth temperatures are used to achieve Si and Sn incorporation, leading to very thin layers. As with characterization of the binary alloy epilayers, the material characteristics were determined by a range of methods. AFM was used to determine the surface morphology and roughness. TEM was used to determine the epilayer thickness, presence and nature of any lattice defects and get qualitative data on the degree of crystallinity including lattice defects and precipitation. XRD RSMs were used to determine the degree of epilayer strain relaxation and to determine the degree of crystal quality from the Bragg peak FWHM, by assuming a binary $Ge_{1-x}Sn_x$ alloy growth the lower bound for alloy Sn fraction could be determined, but the actual

ternary alloy epilayer composition could not. SIMS was used to determine the alloy

composition and the thickness of the ternary alloy epilayer. Raman spectroscopy was

also used as a rapid method to confirm that all the elements are incorporated into the

lattice.

7.2.5.2.1 TEM

TEM images of the $Si_yGe_{1-x-y}Sn_x$/Ge/Si structure is shown in Figure 7-1, show the

ternary alloy epilayers are very thin. The observed layers are of a high crystalline

quality, but with a fairly high concentration of lattice defects.

A HR-TEM image, obtained using a JOEL 2100 fx, is shown in Figure 7-2 which

show that the $Si_yGe_{1-x-y}Sn_x$ epilayer is of high crystalline quality, without indication

of a high density of lattice defects. The epilayer-buffer interface is well-defined and

the interface between the two epitaxial layers clearly visible. Additionally, point

misfit dislocations are visible at the $Si_yGe_{1-x-y}Sn_x$ /Ge interface.
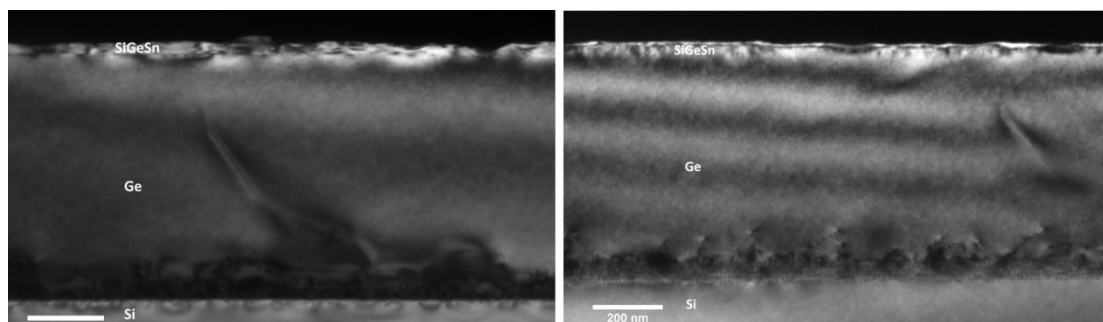
Figure 7-1 (left) A TEM (004) diffraction condition image of the SiGeSn/Ge/Si structure. The epilayer appears to be defective and uneven. (right) (224) diffraction condition image of the SiGeSn/Ge/Si strucutre. The dislocations appear to penetrate through the thin epilayer. This is different to what is observed with binary alloy epilayers, possibly indicating a different relaxation mechanism or possibly a different growth mechanism.
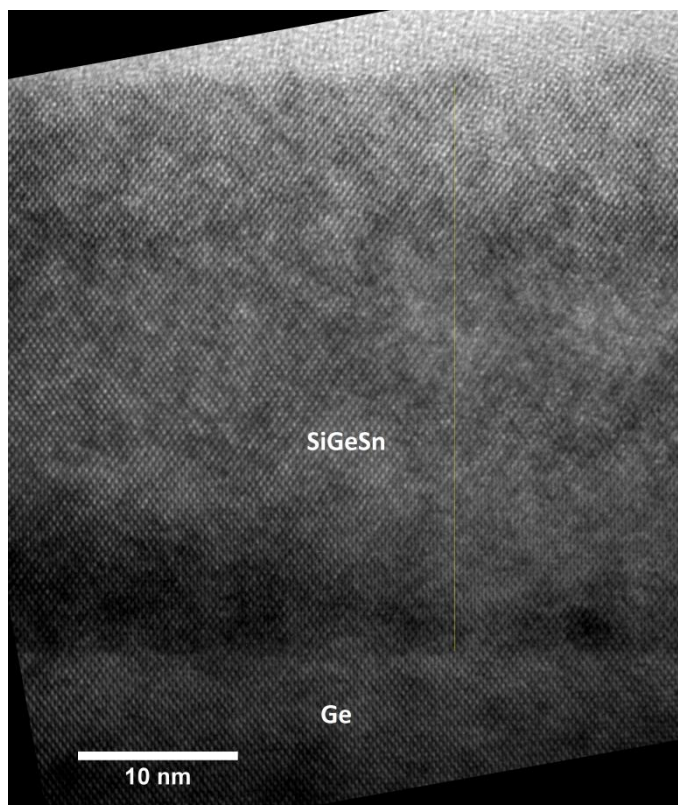
Figure 7-2 A high magnification HR-TEM image of the SiGeSn epilayer and the top of the Ge buffer. The crystalline structure of the $Si_yGe_{1-x-y}Sn_x$ epilayer is 35 nm thick.

The low magnification images of the $Si_yGe_{1-x-y}Sn_x$ epilayer indicate the presence of lattice defects in the layer, which are not observed at higher magnification where the epilayer appears to have high crystal quality and be relatively defect free. This discrepancy can be attributed to the defect density being sufficiently low for them not to appear in the low sample volume observed at high magnifications. In the high magnification image some epilayer surface roughening is observable.

7.2.5.2.2 XRD

In the symmetric and asymmetric RSMs, shown in Figure 7-4 the XRD Bragg peak of the $Si_yGe_{1-x-y}Sn_x$ epilayer has a very low intensity, which may be due to the layer being very thin. The low intensity makes determining the degree of strain relaxation of epilayer challenging, but it appears to have undergone some strain relaxation with
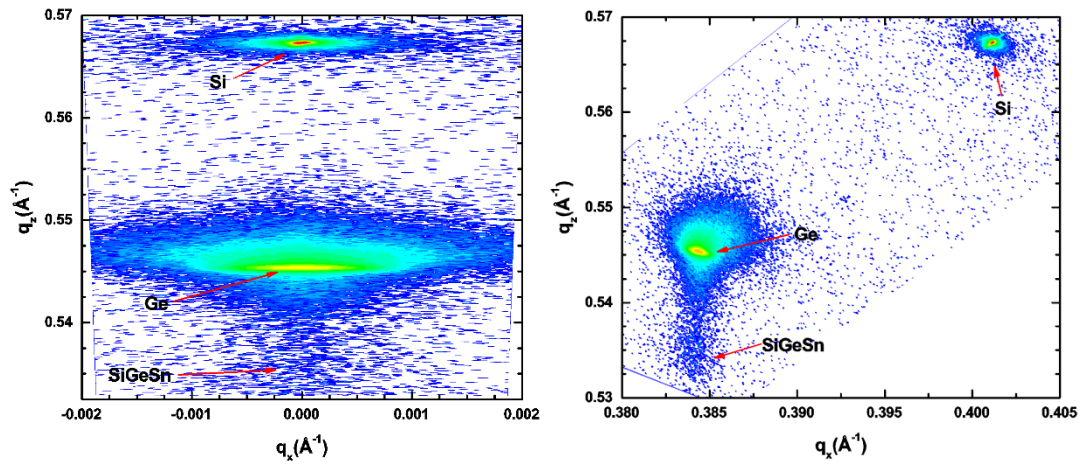
Figure 7-4 A XRD RMSs of an SiGeSn/Ge/Si sample (left) symmetric (004) and (right) asymmetric (224). The SiGeSn Bragg peaks are very weak, though it appears to be slightly strain relaxed relative to the Ge buffer.

the $Si_yGe_{1-x-y}Sn_x$ Bragg peak q_x value differing only slightly from that of the underlying Ge buffer. Without determining the epilayer composition it is not possible to determining the degree of layer relaxation.

While the $Si_yGe_{1-x-y}Sn_x$ RSM Bragg peak are very weak, the epilayers peak is clear in the XRD (004) rocking curve (Figure 7-3), due to a longer count time. If the $Si_yGe_{1-x-y}Sn_x$ peak was analysed as a binary $Ge_{1-x}Sn_x$ alloy the Sn fraction would be 3 at. %.
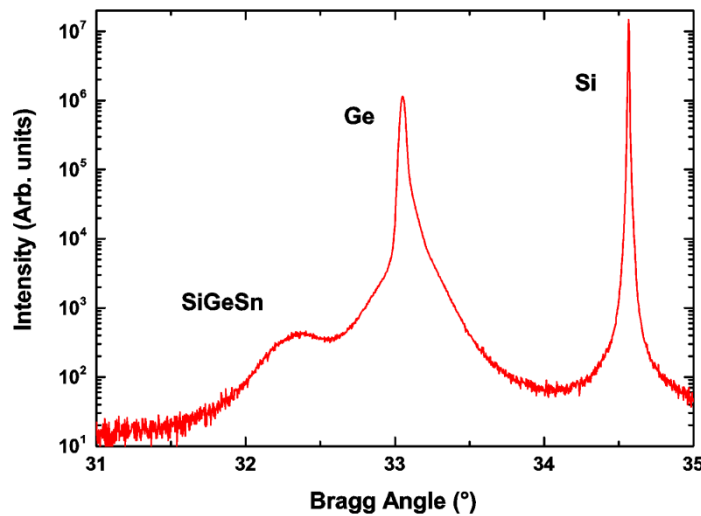
Figure 7-3 A representative XRD (004) rocking curve of a SiGeSn/Ge/Si sample. The $Si_yGe_{1-x-y}Sn_x$ Bragg peak is clearly discernible, but is very weak and broad.

186

This places a lower limit on the Sn fraction of the ternary alloy, as adding Si reduces the lattice parameter for a given Sn concentration.

The $Si_yGe_{1-x-y}Sn_x$ epilayer Bragg peak is broad, which is consistent with a thin layer having some lattice defects as observed in the low magnification TEM images discussed previously. This indicates that the crystal quality of the ternary alloys investigated is not as high as binary alloys grown under similar conditions.

7.2.5.2.3 Raman
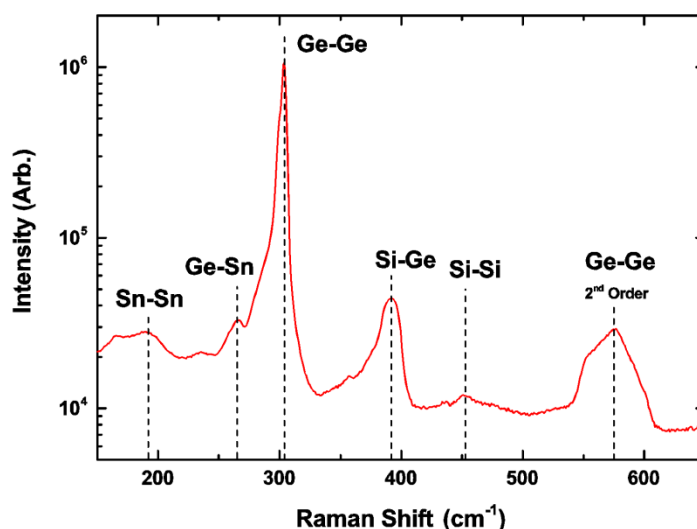
Figure 7-5 Raman spectroscopy scan of $Si_yGe_{1-x-y}Sn_x$/Ge/Si with a sample temperature of 150 K. The SiGeSn epilayer was 35 nm thick, therefore some of the detected signal will be from the Ge buffer. However, the signal from non-Ge elements are clear.

Raman spectroscopy is useful for determining the elements contained in an epilayer and confirming the distribution of bonding. Room temperature and low temperature Raman scans of the ternary alloy samples were obtained; a spectra obtained at 150 K is shown in Figure 7-5. The incorporation of Si in the $Ge_{1-x}Sn_x$ matrix leads to additional peaks from the Si-Ge and Si-Si bond, the values of these Raman shifts and

the others observed are established in the literature from Si_yGe_{1-y} and Ge1-xSnx research [49,121,122].

Weaker first-order Raman scattering peaks can be assigned to phonon modes from the alloy. A particularly intense Sn-Sn bond, relative to the low concentration of Sn in the alloy, may indicative some Sn clustering and the onset of segregation. An intense Si-Sn peak would be indicative of Si favouring sites near Sn atoms, which would minimise localised strain in the Ge dominated lattice. Other work has suggested this Si-Sn peak contributes the broadening of the Si Ge peak at ~400 cm^{-1}, but even at low temperatures is not observed here [113].

These Raman spectra confirm the incorporation of Si and Sn into the alloy crystal lattice. The shoulder to left of the Ge-Ge peak is attributed to a strained Ge-Ge peak, which is indicative of a Ge-Ge bonding close to a comparatively heavy Sn atom.

The ~30 nm $Si_yGe_{1-x-y}Sn_x$ epilayer thickness means that the laser penetration depth permeates the underlying Ge buffer, consequently from Raman data alone the epilayer composition cannot determined accurately. Despite measuring using low sample temperatures, the Raman peak signal intensity for the Si- and Sn- bond is relatively weak, which is attributed to the low concentration of these elements and from the detected spectra including signal contributions from the Ge buffer.

7.2.5.2.4 SIMS

In this work SIMS measurements were used to measure the composition of $Si_yGe_{1-y-x}Sn_x$ alloy epitaxial layers, as XRD cannot give a unique composition. As previously discussed SIMS gives the material composition as a function of sample depth.

The SIMS profiles for two $Si_yGe_{1-x-y}Sn_x$ /Ge/Si samples are shown in Figure 7-5. These plots show that for both samples there is a thin surface oxide layer, with

oxygen composing ~50% of the material at a 2-3 nm depth, at greater sample depth the oxygen fraction decreases to <1% at a depth of 10 nm from the surface. Below the surface oxide, there is a constant composition $Si_yGe_{1-x-y}Sn_x$ ternary layer. Both $Si_yGe_{1-x-y}Sn_x$ epilayer samples have a Sn fraction of 5 at. %., with a Si fraction of 6 and 8 at. %, for the left and right plot respectively. Below the constant composition layer, the Si and Sn concentrations decrease smoothly with depth, potentially indicating some limited Si and Sn diffusion into the Ge-buffer during epilayer growth.
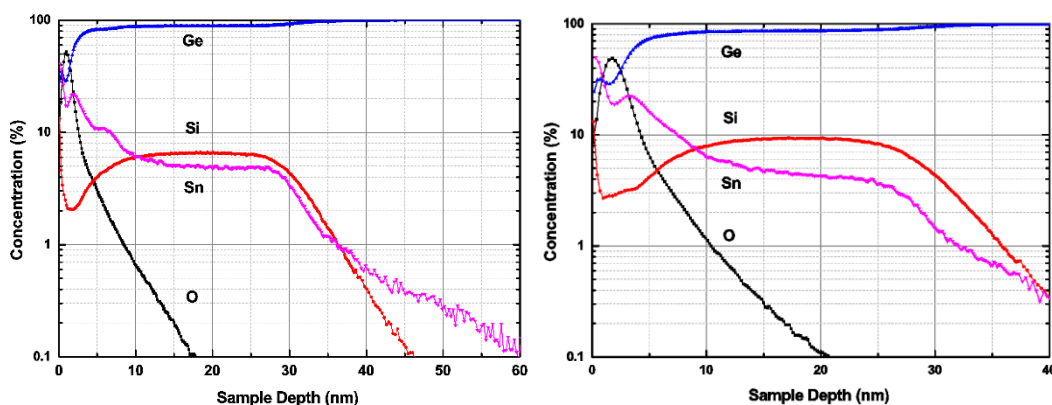
Figure 7-6 SIMS profiles from two $Si_yGe_{1-x-y}Sn_x$ epilayer samples. Both samples show high oxygen incorporation in the first 5 nm of the surface, with O fractions declining to ~1% below 10 nm. Both samples show lower Si fractions in the oxide and higher Sn fractions in the top 10 nm of the surface compared to the layer below. One sample (left) shows 20 nm of constant composition $Si_{0.06}Ge_{0.89}Sn_{0.05}$ while the other sample (right) has a 15 nm layer of $Si_{0.08}Ge_{0.87}Sn_{0.05}$. Below the epilayer, Si and Sn concentrations gradually decrease

The epilayer thickness and composition determined by SIMS are in agreement with other characterization observations, TEM and XRD respectively. The ~35 nm epilayer thickness observed in TEM is approximately in agreement with the SIMS profile of the oxide and the constant composition layer, with the Si and Sn fractions dropping below 1 at. % at this depth for both samples. The compositions from SIMS give predicted lattice parameters in agreement with the XRD results.

7.2.5.3 SiGeSn Summary

Ternary $Si_yGe_{1-x-y}Sn_x$ layers have been grown by CVD, but determining the alloy composition is reliant on SIMS – which is less routine than XRD, and therefore more costly. The ternary alloy layers produced in this work have a greater density of defects than binary alloys grown by the same method. Epilayer strain relaxation appears to initiate at comparatively non-Ge low composition for low epilayer thickness. The surface roughness of these samples may mean using these layers as platforms for subsequent growth will require further development.

During $Si_yGe_{1-x-y}Sn_x$ growth, the Sn and Ge precursor gas concentrations were set to be equivalent to those used this growth temperature produced a binary $Ge_{1-x}Sn_x$ alloy with approximately 10 at. % Sn. The lower Sn fractions determined for the ternary alloy layers, half of the target, shows a significant decrease in Sn incorporation. The total of the Sn and Si concentrations, however, is much closer to the expected Sn fraction, it is believed therefore that there is competition between the Sn and Si precursors at the growth surface for active sites during CVD growth.

The ternary alloy is a potential route for advancing the available material properties attainable with Sn-rich alloys. As with the binary alloy further work will be needed to develop the growth method to produce the desired structures, but progress is being made.

The research on germanium-tin alloys to date has revealed many exciting properties, with potential applications which will enrich the capabilities of currently available devices. But much work remains to be done, both to realise these applications and to fully explore the properties of germanium-tin alloys which expand our current knowledge of condensed matter.

8 References

[1] M.M. Waldrop, More than Moore, Nature. 530 (2016) 145. doi:10.1038/530144a.

[2] R. a. Soref, L. Friedman, Direct-gap Ge/GeSn/Si and GeSn/Ge/Si heterostructures, Superlattices Microstruct. 14 (1993) 189–193. doi:10.1006/spmi.1993.1122.

[3] R. a. Soref, Silicon-based optoelectronics, Proc. IEEE. 81 (1993) 1687–1706. doi:10.1109/5.248958.

[4] S. Oguz, W. Paul, T.F. Deutsch, B.Y. Tsaur, D. V. Murphy, Synthesis of metastable, semiconducting Ge-Sn alloys by pulsed UV laser crystallization, Appl. Phys. Lett. 43 (1983) 848. doi:10.1063/1.94524.

[5] J. Kouvetakis, J. Menendez, A.V.G. Chizmeshya, TIN-BASED GROUP IV SEMICONDUCTORS: New Platforms for Opto- and Microelectronics on Silicon, Annu. Rev. Mater. Res. 36 (2006) 497–554. doi:10.1146/annurev.matsci.36.090804.095159.

[6] E. Kasper, J. Werner, M. Oehme, S. Escoubas, N. Burle, J. Schulze, Growth of silicon based germanium tin alloys, Thin Solid Films. 520 (2012) 3195–3200. doi:10.1016/j.tsf.2011.10.114.

[7] R. Soref, J. Kouvetakis, J. Menendez, Advances in SiGeSn/Ge Technology, Mater. Res. Soc. Symp. 958 (2007).

[8] P. Aella, C. Cook, J. Tolle, S. Zollner, a. V.G. Chizmeshya, J. Kouvetakis, Optical and structural properties of $Si_x Sn_y Ge_{1-x-y}$ alloys, Appl. Phys. Lett. 84 (2004) 888. doi:10.1063/1.1645324.

[9] R. Roucka, J. Tolle, C. Cook, a. V.G. Chizmeshya, J. Kouvetakis, V. D'Costa, et al., Versatile buffer layer architectures based on $Ge_{1-x}Sn_x$ alloys, Appl. Phys. Lett. 86 (2005) 191912. doi:10.1063/1.1922078.

[10] R. Roucka, J. Tolle, B. Forrest, J. Kouvetakis, V.R. D'Costa, J. Menéndez, $Ge_{1-y}Sn_y/Si(100)$ composite substrates for growth of $In_x Ga_{1-x}As$ and $GaAs_{1-x}Sb_x$ alloys, J. Appl. Phys. 101 (2007) 13518. doi:10.1063/1.2407274.

[11] R.T. Beeler, G.J. Grzybowski, R. Roucka, L. Jiang, J. Mathews, D.J. Smith, et al., Synthesis and Materials Properties of Sn / P-Doped Ge on Si (100): Photoluminescence and Prototype Devices, Chem. Mater. 23 (2011) 4480–4486. doi:dx.doi.org/10.1021/cm201648x.

[12] A.V.G. Chizmeshya, M.R. Bauer, J. Kouvetakis, Experimental and Theoretical Study of Deviations from Vegard ' s Law in the $Sn_x Ge_{1-x}$ System, Chem. Mater. 15 (2003) 2511–2519.

[13] Y. Shimura, T. Asano, O. Nakatsuka, S. Zaima, Crystallinity Improvement of Epitaxial Ge Grown on a Ge(110) Substrate by Incorporation of Sn, Appl. Phys. Express. 5 (2012) 15501. doi:10.1143/APEX.5.015501.

[14] M.R. Bauer, J. Tolle, C. Bungay, A.V.G. Chizmeshya, D.J. Smith, J. Menéndez, et al., Tunable band structure in diamond–cubic tin–germanium alloys grown on silicon substrates, Solid State Commun. 127 (2003) 355–359. doi:10.1016/S0038-1098(03)00446-0.

[15] V.R. D'Costa, W. Wang, Q. Zhou, T.K. Chan, T. Osipowicz, E.S. Tok, et al., Compositional dependence of optical critical point parameters in pseudomorphic GeSn alloys, J. Appl. Phys. 116 (2014) 53520.

doi:10.1063/1.4892105.

[16] X. Zhang, C. Ying, Z. Li, G. Shi, First-principles calculations of structural stability, elastic, dynamical and thermodynamic properties of SiGe, SiSn, GeSn, Superlattices Microstruct. 52 (2012) 459–469. doi:10.1016/j.spmi.2012.06.001.

[17] Y. Shimura, N. Tsutsui, O. Nakatsuka, A. Sakai, S. Zaima, Low temperature growth of Ge1−xSnx buffer layers for tensile–strained Ge layers, Thin Solid Films. 518 (2010) S2–S5. doi:10.1016/j.tsf.2009.10.044.

[18] S. Wirths, a. T. Tiedemann, Z. Ikonic, P. Harrison, B. Holländer, T. Stoica, et al., Band engineering and growth of tensile strained Ge/(Si)GeSn heterostructures for tunnel field effect transistors, Appl. Phys. Lett. 102 (2013) 192103. doi:10.1063/1.4805034.

[19] S. Takeuchi, Y. Shimura, T. Nishimura, B. Vincent, G. Eneman, T. Clarysse, et al., Ge1−xSnx stressors for strained-Ge CMOS, Solid. State. Electron. 60 (2011) 53–57. doi:10.1016/j.sse.2011.01.022.

[20] Y. Dong, W. Wang, X. Xu, X. Gong, D. Lei, Q. Zhou, et al., Germanium-Tin on Si Avalanche Photodiode: Device Design and Technology Demonstration, IEEE Trans. Electron Devices. 62 (2015) 128–135. doi:10.1109/TED.2014.2366205.

[21] K. Majumder, N.R. Das, Effects of alloy composition on gain and bandwidth of Si/SiGe and Si/GeSn avalanche photodiodes, Opt. - Int. J. Light Electron Opt. 127 (2016) 3059–3064. doi:10.1016/j.ijleo.2015.11.174.

[22] J. Liu, D.D. Cannon, K. Wada, Y. Ishikawa, S. Jongthammanurak, D.T. Danielson, et al., Tensile strained Ge p-i-n photodetectors on Si platform for C and L band telecommunications, Appl. Phys. Lett. 87 (2005) 1–4. doi:10.1063/1.1993749.

[23] R. Roucka, J. Xie, J. Kouvetakis, J. Mathews, V. D'Costa, E. Al., GeSn photoconductor structures at 1.55μm From advanced materials_2008.pdf, J. Vac. Sci. Technol. B. 26 (2008) 1952–1959.

[24] J. Mathews, R. Roucka, J. Xie, S.Q. Yu, J. Me??ndez, J. Kouvetakis, Extended performance GeSn/Si(100) p-i-n photodetectors for full spectral range telecommunication applications, Appl. Phys. Lett. 95 (2009) 10–13. doi:10.1063/1.3238327.

[25] V.R. D'Costa, Y. Fang, J. Mathews, R. Roucka, J. Tolle, J. Menéndez, et al., Sn-alloying as a means of increasing the optical absorption of Ge at the C - and L -telecommunication bands, Semicond. Sci. Technol. 24 (2009) 115006. doi:10.1088/0268-1242/24/11/115006.

[26] A. Gassenq, F. Gencarelli, J. Van Campenhout, Y. Shimura, R. Loo, G. Narcy, et al., GeSn / Ge heterostructure short-wave infrared photodetectors on silicon, Opt. Express. 20 (2012) 27–31.

[27] Y.-Y. Fang, J. Xie, J. Tolle, R. Roucka, V.R. D'Costa, A.V.G. Chizmeshya, et al., Molecular-Based Synthetic Approach to New Group IV Materials for High-Efficiency, Low-Cost Solar Cells and Si-Based Optoelectronics, J. Am. Chem. Soc. 130 (2008) 16095–16102. doi:10.1021/ja806636c.

[28] B.R. Conley, A. Mosleh, S.A. Ghetmiri, H. a Naseem, J. Tolle, S. Yu, CVD growth of Ge$_{1−x}$Sn$_x$ using large scale Si process for higher efficient multi-junction solar cells, in: 2013 IEEE 39th Photovolt. Spec. Conf., IEEE, 2013: pp. 1346–1349. doi:10.1109/PVSC.2013.6744392.

[29]   J. Xie, A.V.G. Chizmeshya, J. Tolle, V.R. Dcosta, J. Menendez, J. Kouvetakis, Synthesis, stability range, and fundamental properties of Si-Ge-Sn semiconductors grown directly on Si(100) and Ge(100) platforms, Chem. Mater. 22 (2010) 3779–3789. doi:10.1021/cm100915q.

[30]   H.-J. Jo, G.H. Kim, J.S. Kim, M.-Y. Ryu, Y.K. Yeo, T.R. Harris, et al., Observation of temperature-dependent heavy- and light-hole split direct bandgap and tensile strain from Ge0.985Sn0.015 using photoreflectance spectroscopy, Curr. Appl. Phys. 16 (2016) 83–87. doi:10.1016/j.cap.2015.10.014.

[31]   K. Ye, W. Zhang, M. Oehme, M. Schmid, M. Gollhofer, K. Kostecki, et al., Absorption coefficients of GeSn extracted from PIN photodetector response, Solid. State. Electron. 110 (2015) 71–75. doi:10.1016/j.sse.2015.01.017.

[32]   J. Liu, R. Camacho-Aguilera, J.T. Bessette, X. Sun, X. Wang, Y. Cai, et al., Ge-on-Si optoelectronics, Thin Solid Films. 520 (2012) 3354–3360. doi:10.1016/j.tsf.2011.10.121.

[33]   S. Gupta, B. Magyari-Köpe, Y. Nishi, K.C. Saraswat, Achieving direct band gap in germanium through integration of Sn alloying and external strain, J. Appl. Phys. 113 (2013) 073707_1-073707_7. doi:10.1063/1.4792649.

[34]   M. Bauer, J. Taraci, J. Tolle, a. V.G. Chizmeshya, S. Zollner, D.J. Smith, et al., Ge–Sn semiconductors for band-gap and lattice engineering, Appl. Phys. Lett. 81 (2002) 2992. doi:10.1063/1.1515133.

[35]   B. Vincent, F. Gencarelli, H. Bender, C. Merckling, B. Douhard, D.H. Petersen, et al., Undoped and in-situ B doped GeSn epitaxial growth on Ge by atmospheric pressure-chemical vapor deposition, Appl. Phys. Lett. 99 (2011) 152103. doi:10.1063/1.3645620.

[36]   M. Myronov, C. Morrison, J. Halpin, S. Rhead, J. Foronda, D. Leadley, Revealing the high room and low temperature mobilities of 2D holes in a strained Ge quantum well heterostructures grown on a standard Si(001) substrate, 2014 7th Int. Silicon-Germanium Technol. Device Meet. ISTDM 2014. 110 (2014) 11–12. doi:10.1109/ISTDM.2014.6874628.

[37]   J. Mathews, R.T. Beeler, J. Tolle, C. Xu, R. Roucka, J. Kouvetakis, et al., Direct-gap photoluminescence with tunable emission wavelength in Ge[sub 1−y]Sn[sub y] alloys on silicon, Appl. Phys. Lett. 97 (2010) 221912. doi:10.1063/1.3521391.

[38]   S. Wirths, D. Stange, M.-A. Pampillón, A.T. Tiedemann, G. Mussler, A. Fox, et al., High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors, ACS Appl. Mater. Interfaces. 7 (2015) 62–67. doi:10.1021/am5075248.

[39]   L. Wang, S. Su, W. Wang, X. Gong, Y. Yang, P. Guo, et al., Strained germanium–tin (GeSn) p-channel metal-oxide-semiconductor field-effect-transistors (p-MOSFETs) with ammonium sulfide passivation, Solid. State. Electron. 83 (2013) 66–70. doi:10.1016/j.sse.2013.01.031.

[40]   D. Stange, S. Wirths, N. Von Den Driesch, G. Mussler, T. Stoica, Z. Ikonic, et al., Optical Transitions in Direct-Bandgap Ge1-xSnx Alloys, ACS Photonics. 2 (2015) 1539–1545. doi:10.1021/acsphotonics.5b00372.

[41]   K.H. Lee, Y.H. Tan, A. Jandl, E.A. Fitzgerald, C.S. Tan, Comparative studies of the growth and characterization of germanium epitaxial film on silicon (001) with 0° and 6° offcut, J. Electron. Mater. 42 (2013) 1133–1139. doi:10.1007/s11664-013-2538-7.

[42] J.M. Hartmann, A. Abbadie, N. Cherkashin, H. Grampeix, L. Clavelier, Epitaxial growth of Ge thick layers on nominal and 6° off Si(0 0 1); Ge surface passivation by Si, Semicond. Sci. Technol. 24 (2009) 55002. doi:10.1088/0268-1242/24/5/055002.

[43] S. Wirths, D. Buca, A.T. Tiedemann, B. Hollander, P. Bernardy, T. Stoica, et al., Epitaxial Growth of Ge1-xSnx by Reduced Pressure CVD Using SnCl4 and Ge2H6, ECS Trans. 50 (2012) 885–893.

[44] D.J. Paul, Si/SiGe heterostructures: from material and physics to devices and circuits, Semicond. Sci. Technol. 19 (2004) R75–R108. doi:10.1088/0268-1242/19/10/R02.

[45] M. Oehme, M. Schmid, M. Kaschel, M. Gollhofer, D. Widmann, E. Kasper, et al., GeSn p-i-n detectors integrated on Si with up to 4% Sn, Appl. Phys. Lett. 101 (2012) 141110. doi:10.1063/1.4757124.

[46] M. Oehme, K. Kostecki, T. Arguirov, G. Mussler, K. Ye, M. Gollhofer, et al., GeSn heterojunction LEDs on Si substrates, IEEE Photonics Technol. Lett. 26 (2014) 187–189. doi:10.1109/LPT.2013.2291571.

[47] G. Roelkens, U.D. Dave, A. Gassenq, N. Hattasan, C. Hu, B. Kuyken, et al., Silicon-Based Photonic Integration Beyond the Telecommunication Wavelength Range, IEEE J. Sel. Top. QUANTUM Electron. 20 (2014).

[48] T. Pham, W. Du, H. Tran, J. Margetis, J. Tolle, G. Sun, et al., Systematic study of Si-based GeSn photodiodes with 26 μm detector cutoff for short-wave infrared detection, Opt. Express. 24 (2016) 4519. doi:10.1364/OE.24.004519.

[49] H. Chen, Y. Li, C. Peng, H. Liu, Y. Liu, Q. Huang, et al., Crosshatching on a SiGe film grown on a Si(001) substrate studied by Raman mapping and atomic force microscopy, Phys. Rev. B. 65 (2002) 1–4. doi:10.1103/PhysRevB.65.233303.

[50] G. SH;, P.C. R;, A.W.. Ewald, R.J.. Wagner, Interband magnetoreflection of alpha tin, J. Phys. Chem. Solids. 31 (1970) 2031–2049.

[51] V. D'Costa, C. Cook, A. Birdwell, C. Littler, M. Canonico, S. Zollner, et al., Optical critical points of thin-film Ge1−ySny alloys: A comparative Ge1−ySny∕Ge1−xSix study, Phys. Rev. B. 73 (2006) 125207. doi:10.1103/PhysRevB.73.125207.

[52] R. Chen, H. Lin, Y. Huo, C. Hitzman, T.I. Kamins, J.S. Harris, Increased photoluminescence of strain-reduced, high-Sn composition Ge1−xSnx alloys grown by molecular beam epitaxy, Appl. Phys. Lett. 99 (2011) 181125. doi:10.1063/1.3658632.

[53] G. Grzybowski, R.T. Beeler, L. Jiang, D.J. Smith, J. Kouvetakis, J. Menéndez, Next generation of Ge1−ySny (y = 0.01-0.09) alloys grown on Si(100) via Ge3H8 and SnD4: Reaction kinetics and tunable emission, Appl. Phys. Lett. 101 (2012) 72105. doi:10.1063/1.4745770.

[54] G. Sun, R. a. Soref, H.H. Cheng, Design of an electrically pumped SiGeSn/GeSn/SiGeSn double-heterostructure midinfrared laser, J. Appl. Phys. 108 (2010) 33107. doi:10.1063/1.3467766.

[55] Y. Chibane, M. Ferhat, Electronic structure of Snx Ge1-x alloys for small Sn compositions: Unusual structural and electronic properties, J. Appl. Phys. 107 (2010) 1–8. doi:10.1063/1.3326162.

[56] J.C. Slater, Atomic Radii in Crystals, J. Chem. Phys. 41 (1964) 3199. doi:10.1063/1.1725697.

[57] J.A. Van Vechten, J.C. Phillips, New set of tetrahedral covalent radii, Phys. Rev. B. 2 (1970) 2160–2167. doi:10.1103/PhysRevB.2.2160.

[58] E. Kasper, A. Schuh, G. Bauer, B. Holländer, H. Kibbel, Test of Vegard's law in thin epitaxial SiGe layers, J. Cryst. Growth. 157 (1995) 68–72. doi:10.1016/0022-0248(95)00373-8.

[59] F. Gencarelli, B. Vincent, J. Demeulemeester, A. Vantomme, A. Moussa, A. Franquet, et al., Crystalline Properties and Strain Relaxation Mechanism of CVD Grown GeSn, ECS J. Solid State Sci. Technol. 2 (2013) P134–P137. doi:10.1149/2.011304jss.

[60] N. Bhargava, M. Coppinger, J. Prakash Gupta, L. Wielunski, J. Kolodzey, Lattice constant and substitutional composition of GeSn alloys grown by molecular beam epitaxy, Appl. Phys. Lett. 103 (2013) 41908. doi:10.1063/1.4816660.

[61] S. Wirths, D. Buca, S. Mantl, Si–Ge–Sn alloys: From growth to applications, Prog. Cryst. Growth Charact. Mater. 62 (2016) 1–39. doi:10.1016/j.pcrysgrow.2015.11.001.

[62] J.P. Dismukes, L. Ekstrom, R.J. Paff, Lattice Parameter and Density in Germanium-Silicon Alloys, J. Phys. Chem. 68 (1964) 3021–3027. doi:10.1021/j100792a049.

[63] D. Hull, D.J. Bacon, Introduction to Dislocations, 3rd ed., Pergamon Press plc, 1984.

[64] R.F.C. Farrow, D.S. Robertson, G.M. Williams, A.G. Cullis, G.R. Jones, I.M. Young, et al., The growth of metastable, heteroepitaxial films of α-Sn by metal beam epitaxy, J. Cryst. Growth. 54 (1981) 507–518. doi:10.1016/0022-0248(81)90506-6.

[65] W. Wang, Y. Dong, Q. Zhou, E.S. Tok, Y.-C. Yeo, Germanium–tin interdiffusion in strained Ge/GeSn multiple-quantum-well structure, J. Phys. D. Appl. Phys. 49 (2016) 225102. doi:10.1088/0022-3727/49/22/225102.

[66] L. Wang, W. Wang, Q. Zhou, J. Pan, Z. Zhang, E.S. Tok, et al., Post-growth annealing of germanium-tin alloys using pulsed excimer laser, J. Appl. Phys. 118 (2015) 25701. doi:10.1063/1.4926484.

[67] H. Li, Y.X. Cui, K.Y. Wu, W.K. Tseng, H.H. Cheng, H. Chen, Strain relaxation and Sn segregation in GeSn epilayers under thermal treatment, Appl. Phys. Lett. 102 (2013) 251907. doi:10.1063/1.4812490.

[68] J.M. Hartmann, J.F. Damlencourt, Y. Bogumilowicz, P. Holliger, G. Rolland, T. Billon, Reduced pressure-chemical vapor deposition of intrinsic and doped Ge layers on Si(0 0 1) for microelectronics and optoelectronics purposes, J. Cryst. Growth. 274 (2005) 90–99. doi:10.1016/j.jcrysgro.2004.10.042.

[69] R. Chen, Y.-C. Huang, S. Gupta, A.C. Lin, E. Sanchez, Y. Kim, et al., Material characterization of high Sn-content, compressively-strained GeSn epitaxial films after rapid thermal processing, J. Cryst. Growth. 365 (2013) 29–34. doi:10.1016/j.jcrysgro.2012.12.014.

[70] H. Li, H.H. Cheng, L.C. Lee, C.P. Lee, L.H. Su, Y.W. Suen, Electrical characteristics of Ni Ohmic contact on n-type GeSn, Appl. Phys. Lett. 104 (2014) 241904. doi:10.1063/1.4883748.

[71] W. Assmus, S. Brühne, F. Charra, G. Chiarotti, C. Fischer, G. Fuchs, et al., Springer Handbook of Condensed Matter and Materials Data, 1st ed., Springer Berlin Heidelberg, Wuzburg, 2005. doi:10.1007/3-540-30437-1.

[72] S. Wirths, R. Geiger, N.V. Den Driesch, G. Mussler, T. Stoica, S. Mantl, et al.,

Lasing in direct-bandgap GeSn alloy grown on Si, (2015) 1–14. doi:10.1038/nphoton.2014.321.

[73] a. Jamshidi, M. Noroozi, M. Moeen, A. Hallén, B. Hamawandi, J. Lu, et al., Growth of GeSnSiC layers for photonic applications, Surf. Coatings Technol. 230 (2013) 106–110. doi:10.1016/j.surfcoat.2013.06.074.

[74] J.W. Wagner, Preparation and Properties of Bulk In[sub 1−x]Ga[sub x]As Alloys, J. Electrochem. Soc. 117 (1970) 1193. doi:10.1149/1.2407767.

[75] Y. Yamazoe, T. Nishino, Y. Hamakawa, T. Kariya, Bandgap Energy of InGaAsP Quaternary Alloy, Jpn. J. Appl. Phys. 19 (1980) 1473–1479. doi:10.1143/JJAP.19.1473.

[76] V. D'Costa, Y.-Y. Fang, J. Tolle, J. Kouvetakis, J. Menéndez, Tunable Optical Gap at a Fixed Lattice Constant in Group-IV Semiconductor Alloys, Phys. Rev. Lett. 102 (2009) 1–4. doi:10.1103/PhysRevLett.102.107403.

[77] J. Xie, J. Tolle, V.R. D'Costa, a. V.G. Chizmeshya, J. Menéndez, J. Kouvetakis, Direct integration of active Ge[sub 1−x](Si[sub 4]Sn)[sub x] semiconductors on Si(100), Appl. Phys. Lett. 95 (2009) 181909. doi:10.1063/1.3242002.

[78] P. Moontragoon, R. a. Soref, Z. Ikonic, The direct and indirect bandgaps of unstrained SixGe1−x−ySny and their photonic device applications, J. Appl. Phys. 112 (2012) 73106. doi:10.1063/1.4757414.

[79] N. Amrane, S. Ait Abderrahmane, H. Aourag, Band structure calculation of GeSn and SiSn, Infrared Phys. Technol. 36 (1995) 843–848. doi:10.1016/1350-4495(95)00019-U.

[80] V.R. D'Costa, Y.-Y. Fang, J. Tolle, J. Kouvetakis, J. Menéndez, Ternary GeSiSn alloys: New opportunities for strain and band gap engineering using group-IV semiconductors, Thin Solid Films. 518 (2010) 2531–2537. doi:10.1016/j.tsf.2009.09.149.

[81] S.D. Rhead, J.E. Halpin, V. a. Shah, M. Myronov, D.H. Patchett, P.S. Allred, et al., Tensile strain mapping in flat germanium membranes, Appl. Phys. Lett. 104 (2014) 172107. doi:10.1063/1.4874836.

[82] A.Y. Cho, J.R. Arthur, Molecular beam epitaxy, Prog. Solid State Chem. 10 (1975) 157–191. doi:10.1016/0079-6786(75)90005-9.

[83] O. Gurdal, M.A. Hasan, M.R. Sardela, J.E. Greene, H.H. Radamson, J.E. Sundgren, et al., Growth of metastable Ge1-xSnx/Ge strained layer superlattices on Ge(001)2??1 by temperature-modulated molecular beam epitaxy, Appl. Phys. Lett. 67 (1995) 956. doi:10.1063/1.114707.

[84] M. Oehme, D. Buca, K. Kostecki, S. Wirths, B. Holländer, E. Kasper, et al., Epitaxial growth of highly compressively strained GeSn alloys up to 12.5% Sn, J. Cryst. Growth. 384 (2013) 71–76. doi:10.1016/j.jcrysgro.2013.09.018.

[85] M. Nakamura, Y. Shimura, S. Takeuchi, O. Nakatsuka, S. Zaima, Growth of Ge1−xSnx heteroepitaxial layers with very high Sn contents on InP(001) substrates, Thin Solid Films. 520 (2012) 3201–3205. doi:10.1016/j.tsf.2011.10.153.

[86] W. Wang, W.K. Loke, T. Yin, Z. Zhang, V.R. D'Costa, Y. Dong, et al., Growth and characterization of highly tensile strained Ge1−xSnx formed on relaxed InyGa1−yP buffer layers, J. Appl. Phys. 119 (2016) 125303. doi:10.1063/1.4944718.

[87] Y. Shimura, S. Takeuchi, O. Nakatsuka, B. Vincent, F. Gencarelli, T. Clarysse, et al., In-situ Ga doping of fully strained Ge1-xSnx heteroepitaxial

layers grown on Ge(001) substrates, Thin Solid Films. 520 (2012) 3206–3210. doi:10.1016/j.tsf.2011.10.084.

[88] M.R. Bauer, C.S. Cook, P. Aella, J. Tolle, J. Kouvetakis, P.A. Crozier, et al., SnGe superstructure materials for Si-based infrared optoelectronics, Appl. Phys. Lett. 83 (2003) 3489–3491. doi:10.1063/1.1622435.

[89] M. Bauer, C. Ritter, P. a. Crozier, J. Ren, J. Menendez, G. Wolf, et al., Synthesis of ternary SiGeSn semiconductors on Si(100) via Sn[sub x]Ge[sub 1−x] buffer layers, Appl. Phys. Lett. 83 (2003) 2163. doi:10.1063/1.1606104.

[90] A. Mosleh, S.A. Ghetmiri, B.R. Conley, M. Hawkridge, M. Benamara, A. Nazzal, et al., Material Characterization of Ge1−x Sn x Alloys Grown by a Commercial CVD System for Optoelectronic Device Applications, J. Electron. Mater. 43 (2014) 938–946. doi:10.1007/s11664-014-3089-2.

[91] Y. Inuzuka, S. Ike, T. Asano, W. Takeuchi, O. Nakatsuka, S. Zaima, Characterization of crystallinity of Ge1−xSnx epitaxial layers grown using metal-organic chemical vapor deposition, Thin Solid Films. 602 (2016) 7–12. doi:10.1016/j.tsf.2015.10.043.

[92] K. Suda, S. Ishihara, N. Sawamoto, H. Machida, M. Ishikawa, H. Sudoh, et al., Ge1-xSnx Epitaxial Growth on Ge Substrate by MOCVD, ECS Trans. 64 (2014) 697–701. doi:10.1149/06406.0697ecst.

[93] V. a. Shah, a. Dobbie, M. Myronov, D.R. Leadley, High quality relaxed Ge layers grown directly on a Si(0 0 1) substrate, Solid. State. Electron. 62 (2011) 189–194. doi:10.1016/j.sse.2011.03.005.

[94] A. Mosleh, M. Alher, L.C. Cousar, W. Du, S.A. Ghetmiri, S. Al-Kabi, et al., Buffer-Free GeSn and SiGeSn Growth on Si Substrate Using In Situ SnD4 Gas Mixing, J. Electron. Mater. 45 (2016) 2051–2058. doi:10.1007/s11664-016-4402-z.

[95] J. Kouvetakis, J. Tolle, R. Roucka, V.R. D'Costa, Y.-Y. Fang, A.V.G. Chizmeshya, et al., Nanosynthesis of SiGeSn SCs and devices via purpose built hydride compounds, ECS Trans. 16 (2008) 807–821.

[96] M. Kurosawa, Y. Tojo, R. Matsumura, T. Sadoh, M. Miyao, Single-crystalline laterally graded GeSn on insulator structures by segregation controlled rapid-melting growth, Appl. Phys. Lett. 101 (2012) 91905. doi:10.1063/1.4748328.

[97] K. Toko, N. Oya, N. Saitoh, N. Yoshizawa, T. Suemasu, 70 °C synthesis of high-Sn content (25%) GeSn on insulator by Sn-induced crystallization of amorphous Ge, Appl. Phys. Lett. 106 (2015) 82109. doi:10.1063/1.4913744.

[98] R.R. Lieten, T. Maeda, W. Jevasuwan, H. Hattori, N. Uchida, S. Miura, et al., Tensile-Strained GeSn Metal–Oxide–Semiconductor Field-Effect Transistor Devices on Si(111) Using Solid Phase Epitaxy, Appl. Phys. Express. 6 (2013) 101301. doi:10.7567/APEX.6.101301.

[99] T. Sadoh, A. Ooato, J.-H. Park, M. Miyao, High Sn-concentration (~8%) GeSn by low-temperature (~150°C) solid-phase epitaxy of a-GeSn/c-Ge, Thin Solid Films. 602 (2016) 20–23. doi:10.1016/j.tsf.2015.09.069.

[100] a. S. Saidov, S.N. Usmonov, U.P. Asatova, Growth of Ge1−xSnx solid solution films and study of their structural properties and some of their photoelectric properties, Semiconductors. 46 (2012) 1088–1095. doi:10.1134/S1063782612080180.

[101] O. Nakatsuka, K. Mochizuki, Y. Shimura, T. Yamaha, S. Zaima, Low temperature formation of Si1−x−yGexSny-on-insulator structures by using solid-phase mixing of Ge1−zSnz/Si-on-insulator substrates, Thin Solid Films.

520 (2012) 3288–3292. doi:10.1016/j.tsf.2011.10.120.

[102] G. He, H.A. Atwater, Interband Transitions in SnxGe1-x Alloys, Phys. Rev. Lett. 79 (1997) 1937–1940.

[103] F. Gencarelli, B. Vincent, L. Souriau, O. Richard, W. Vandervorst, R. Loo, et al., Low-temperature Ge and GeSn Chemical Vapor Deposition using Ge2H6, Thin Solid Films. 520 (2012) 3211–3215. doi:10.1016/j.tsf.2011.10.119.

[104] Y. Bogumilowicz, J.M. Hartmann, N. Cherkashin, A. Claverie, G. Rolland, T. Billon, SiGe virtual substrates growth up to 50% Ge concentration for Si/Ge dual channel epitaxy, Mater. Sci. Eng. B Solid-State Mater. Adv. Technol. 124–125 (2005) 113–117. doi:10.1016/j.mseb.2005.08.052.

[105] G. Grzybowski, L. Jiang, R.T. Beeler, T. Watkins, A.V.G. Chizmeshya, C. Xu, et al., Ultra-Low-Temperature Epitaxy of Ge-based Semiconductors and Optoelectronic Structures on Si (100): Introducing Higher Order Germanes (Ge3H8, Ge4H10), Chem. Mater. 24 (2012) 1619–1628.

[106] J.C. Lou, M.S. Lin, J.I. Chyi, J.H. Shieh, Process study of chemically vapour-deposited SnOx (x≈2) films, Thin Solid Films. 106 (1983) 163–173. doi:10.1016/0040-6090(83)90478-9.

[107] N.D. Boscher, C.J. Carmalt, R.G. Palgrave, I.P. Parkin, Atmospheric pressure chemical vapour deposition of SnSe and SnSe2 thin films on glass, Thin Solid Films. 516 (2008) 4750–4757. doi:10.1016/j.tsf.2007.08.100.

[108] Y.J. Cho, C.H. Kim, H.S. Im, Y. Myung, H.S. Kim, S.H. Back, et al., Germanium–tin alloy nanocrystals for high-performance lithium ion batteries, Phys. Chem. Chem. Phys. 15 (2013) 11691. doi:10.1039/c3cp51366a.

[109] M.S. Skilbeck, a J. Marsden, G. Cao, I. a Kinloch, R.J. Young, R.S. Edwards, et al., Multimodal microscopy using "half and half" contact mode and ultrasonic force microscopy., Nanotechnology. 25 (2014) 335708. doi:10.1088/0957-4484/25/33/335708.

[110] Critical Dimension AFM Probes, (n.d.) 541. http://store.nanoscience.com/store/pc/viewcategories.asp?idCategory=10 (accessed August 20, 2016).

[111] R.E. Honig, Sputtering of surfaces by positive ion beams of low energy, J. Appl. Phys. 29 (1958) 549–555. doi:10.1063/1.1723219.

[112] E. Laboratories, SIMS - EAG Laboratories, (n.d.). http://www.eag.com/secondary-ion-mass-spectrometry-sims/ (accessed August 24, 2016).

[113] A. Thompson, D. Attwood, E. Gullikson, M. Howells, K.-J. Kim, K. Kirz, et al., X-ray data booklet, 3rd ed., Berkeley, 2009. doi:10.1107/S090904950100807X.

[114] P. Van der Sluis, Determination of strain in epitaxial semiconductor layers by high-resolution X-ray diffraction, J. Phys. D. Appl. Phys. 188 (1999) A188–A191. http://iopscience.iop.org/0022-3727/26/4A/039 (accessed October 8, 2012).

[115] P.F. Fewster, X-ray diffraction from low-dimensional structures, Semicond. Sci. Technol. 1915 (1993) 1915–1934.

[116] E.L. Saldin, E.A. Schneidmiller, M. V. Yurkov, Femtosecond resolution experiments at third-generation light sources: A concept based on the statistical properties of synchrotron radiation, Opt. Commun. 221 (2003) 403–410. doi:10.1016/S0030-4018(03)01502-5.

[117] P.L. Bonanno, S. Gautier, A.A. Sirenko, A. Kazimirov, Z.H. Cai, W.H. Goh,

et al., Submicron beam X-ray diffraction of nanoheteroepitaxily grown GaN: Experimental challenges and calibration procedures, Nucl. Instruments Methods Phys. Res. Sect. B Beam Interact. with Mater. Atoms. 268 (2010) 320–324. doi:10.1016/j.nimb.2009.09.016.

[118] D.E. Sayers, E.A. Stern, New Technique for Investigating Noncrystalline Structures: Fourier Analysis of the Extended X-Ray — Absorption Fine Structure, Phys. Rev. Lett. 27 (1971) 1204–1207.

[119] B. Lee, P.A. (Laboratories, P.H. Citrin, P. Eisenberger, B.M. Kincaid, Extended x-ray absorption fine structure - its strengths and limitations as a structural tool, Rev. Mod. Phys. 53 (1981).

[120] D.B.. Williams, C.B. Carter, Transmission Electron Microscopy, 2nd ed., Springer US, Boston, MA, 2009. doi:10.1007/978-0-387-76501-3.

[121] J.-H. Fournier-Lupien, S. Mukherjee, S. Wirths, E. Pippel, N. Hayazawa, G. Mussler, et al., Strain and composition effects on Raman vibrational modes of silicon-germanium-tin ternary alloys, Appl. Phys. Lett. 103 (2013) 263103. doi:10.1063/1.4855436.

[122] C. Chang, H. Li, T.-P. Chen, W.-K. Tseng, H. Cheng, C.-T. Ko, et al., The strain dependence of Ge1−xsnx (x=0.083) Raman shift, Thin Solid Films. 593 (2015) 40–43. doi:10.1016/j.tsf.2015.09.040.

[123] R. Cheng, W. Wang, X. Gong, L. Sun, P. Guo, H. Hu, et al., Relaxed and Strained Patterned Germanium-Tin Structures: A Raman Scattering Study, ECS J. Solid State Sci. Technol. 2 (2013) P138–P145. doi:10.1149/2.013304jss.

[124] C. Meng, J. Chen, S. Lee, The Growth and Raman Spectra of boron-doped Silicon Nanowires, (2005) 0–3.

[125] X. Zhang, D. Zhang, J. Zheng, Z. Liu, C. He, C. Xue, et al., Formation and characterization of Ni/Al Ohmic contact on n+-type GeSn, Solid. State. Electron. 114 (2015) 178–181. doi:10.1016/j.sse.2015.09.010.

[126] D.K. Schroder, MATERIAL AND DEVICE SEMICONDUCTOR MATERIAL AND DEVICE Third Edition, 3rd ed., Wiley, 2006. doi:10.1063/1.2810086.

[127] E. Kasper, M. Kittler, M. Oehme, T. Arguirov, Germanium tin: silicon photonics toward the mid-infrared [Invited], Photonics Res. 1 (2013) 69. doi:10.1364/PRJ.1.000069.

[128] J. Sau, M. Cohen, Possibility of increased mobility in Ge-Sn alloy system, Phys. Rev. B. 75 (2007) 45208. doi:10.1103/PhysRevB.75.045208.

[129] J. Lu, J. Sundqvist, M. Ottosson, A. Tarre, A. Rosental, J. Aarik, et al., Microstructure characterisation of ALD-grown epitaxial SnO2 thin films, J. Cryst. Growth. 260 (2004) 191–200. doi:10.1016/j.jcrysgro.2003.08.042.

[130] N. Von Den Driesch, D. Stange, S. Wirths, G. Mussler, B. Holla¨nder, Z. Ikonic, et al., Direct Bandgap Group IV Epitaxy on Si for Laser Applications, Chem. Mater. 27 (2015) 4693–4702. doi:10.1021/acs.chemmater.5b01327.

[131] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, et al., Lasing in direct-bandgap GeSn alloy grown on Si, Nat. Photonics. (2015) 1–5. doi:10.1038/nphoton.2014.321.

[132] T. Asano, S. Kidowaki, M. Kurosawa, N. Taoka, O. Nakatsuka, S. Zaima, Influence of Ge substrate orientation on crystalline structures of Ge1−xSnx epitaxial layers, Thin Solid Films. 557 (2014) 159–163. doi:10.1016/j.tsf.2013.10.087.

[133] K.O. Hara, Y. Hoshi, N. Usami, Y. Shiraki, K. Nakamura, T. Suemasu, N-Type Doping of BaSi 2 Epitaxial Films by Phosphorus Ion Implantation and Thermal Annealing, (2013) 3–4.

[134] T. Paskova, E.B. Svedberg, A. Henry, A.Y. Kuznetsov, H.H. Radamson, B.G. Svensson, et al., Comparison of Strain Relaxation in Si/SiGe/Si Heterostructures after Annealing in Oxidizing and Inert Atmospheres, Phys. Scr. T79 (1999) 202–205.

[135] K. Chen, C. Su, C. Chou, Y. Wu, Formation of Ohmic Contact With Low Contact Resistance on n-GeSn by Fermi Level Depinning Using Plasma Treatment, IEEE Electron Device Lett. 37 (2016) 827–830. doi:10.1109/LED.2016.2566809.

[136] S. Gupta, E. Simoen, R. Loo, O. Madia, D. Lin, C. Merckling, et al., Density and Capture Cross-Section of Interface Traps in GeSnO 2 and GeO 2 Grown on Heteroepitaxial GeSn, ACS Appl. Mater. Interfaces. 8 (2016) 13181–13186. doi:10.1021/acsami.6b01582.

[137] F. Bellenger, B. De Jaeger, C. Merckling, M. Houssa, J. Penaud, L. Nyns, et al., High FET performance for a future CMOS GeO2-based technology, IEEE Electron Device Lett. 31 (2010) 402–404. doi:10.1109/LED.2010.2044011.

[138] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, et al., Effective electrical passivation of Ge(100) for high- k gate dielectric layers using germanium oxide, Appl. Phys. Lett. 91 (2007) 6–9. doi:10.1063/1.2773759.

[139] N.D. Papadopoulos, P.E. Tsakiridis, E. Hristoforou, STRUCTURAL AND ELECTRICAL PROPERTIES OF UNDOPED SnO 2 FILMS DEVELOPED BY A LOW COST CVD TECHNIQUE WITH TWO DIFFERENT METHODS: COMPARATIVE STUDY, J. Optoelectron. Adv. Mater. 7 (2005) 2693–2706.

[140] K. Gallacher, P. Velha, D.J. Paul, I. MacLaren, M. Myronov, D.R. Leadley, Ohmic contacts to n-type germanium with low specific contact resistivity, Appl. Phys. Lett. 100 (2012) 22113. doi:10.1063/1.3676667.

[141] Y. Yamamoto, P. Zaumseil, T. Arguirov, M. Kittler, B. Tillack, Low threading dislocation density Ge deposited on Si (100) using RPCVD, Solid. State. Electron. 60 (2011) 2–6. doi:10.1016/j.sse.2011.01.032.

[142] M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, E.A. Fitzgerald, Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing, Appl. Phys. Lett. 72 (1998) 1718. doi:10.1063/1.121162.

[143] G. Sun, S.-Q. Yu, The SiGeSn approach towards Si-based lasers, Solid. State. Electron. 83 (2013) 76–81. doi:10.1016/j.sse.2013.01.037.