



Queensland University of Technology
Brisbane Australia

This is the author's version of a work that was submitted/accepted for publication in the following source:

Cabanes Aracil, Jaime, Lopez-Roldan, Jose, Coetzee, Jacob, Darmann, Frank, & Tang, Tee (2012) Saturated core high-temperature superconducting fault current limiters as an alternative to conventional series reactors in a distribution grid. In *Proceedings of the 10th International Conference on AC and DC Power Transmission*, The Institution of Engineering and Technology (IET), Holiday Inn, Birmingham.

This file was downloaded from: <http://eprints.qut.edu.au/58279/>

© Copyright 2012 The Institution of Engineering and Technology

All rights reserved. Apart from any copying under the U.K. Copyright, Designs and Patents Act 1988, Part 1, Section 38, whereby a single copy of an article may be supplied, under certain conditions, for the purposes of research or private study, by a library of a class prescribed by The Copyright (Librarians and Archivists) (Copying of Copyright Material) regulations 1989: SI 1989/1212, no part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means without the prior permission of the copyright owners. Permission is, however, not required to copy abstracts of papers or articles on condition that a full reference to the source is shown.

Notice: *Changes introduced as a result of publishing processes such as copy-editing and formatting may not be reflected in this document. For a definitive version of this work, please refer to the published source:*

Saturated Core High-Temperature Superconducting Fault Current Limiters as an Alternative to Conventional Series Reactors in a Distribution Grid

Jaime Cabanes Aracil, Jose Lopez-Roldan, Jacob Carl Coetzee, Frank Darmann and Tee Tang

Abstract-- Series reactors are used in distribution grids to reduce the short-circuit fault level. Some of the disadvantages of the application of these devices are the voltage drop produced across the reactor and the steep front rise of the transient recovery voltage (TRV), which generally exceeds the rating of the associated circuit breaker.

Simulations were performed to compare the characteristics of a saturated core High-Temperature Superconducting Fault Current Limiter (HTS FCL) and a series reactor. The design of the HTS FCL was optimized using the evolutionary algorithm. The resulting Pareto frontier curve of optimum solution is presented in this paper. The results show that the steady-state impedance of an HTS FCL is significantly lower than that of a series reactor for the same level of fault current limiting. Tests performed on a prototype 11 kV HTS FCL confirm the theoretical results.

The respective transient recovery voltages (TRV) of the HTS FCL and an air core reactor of comparable fault current limiting capability are also determined. The results show that the saturated core HTS FCL has a significantly lower effect on the rate of rise of the circuit breaker TRV as compared to the air core reactor. The simulation results are validated with short-circuit test results.

Index Terms-- fault current limiters (FCLs), finite element method, magnetic flux, saturable cores, short circuit currents.

I. INTRODUCTION

There is an increasing worldwide demand for electrical power, which drives distribution system expansion and gives rise to higher fault current levels. The sudden reduction in the power grid impedance under fault conditions causes a surge in current. When this occurs, the protection system mitigates the surge current by commanding the circuit breakers to open, either until the mishap clear itself or until someone repairs the fault. This process can be costly and can result in significant downtime in grid power. These problems can be overcome by limiting the fault current to an acceptable level. A conventional method of protecting the power grid involves the use of air core reactors. This system has been proven to be reliable at a reduced cost. However, such a system has a number of drawbacks such as large voltage drops and substantial power loss during normal operation. These factors make them unattractive under certain conditions [1, 2].

J. Cabanes Aracil, J. Lopez-Roldan, J.C. Coetzee and T. Tang are with the School of Electrical Engineering and Computer Science, Queensland University of Technology, P.O. Box 2434, Brisbane, Queensland, 4001, Australia, (phone:+61(0)7-31382865; e-mail: jaime.cabanes@qut.edu.au).

F. Darmann are with Zenergy Power Pty Ltd., Suite 7, 1 Lowden Square, Wollongong, NSW 2500, Australia.

High temperature superconducting (HTS) fault current limiters (FCLs) are more modern protection systems. These devices present negligible impedance under normal operating conditions, but have the ability to switch to a high impedance state when a fault occurs. HTS FCLs can thus act as high-voltage protectors for power grids under short circuit conditions, while increasing system reliability and efficiency and enabling cost-efficient grid expansion including the integration of distributed generation sources.

Figure 1 shows the basic arrangement of the air core series reactor system. The air core series reactor consists of a coil or a battery of coils in series with the circuit that needs to be protected.

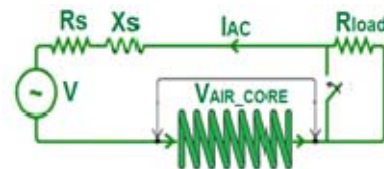


Figure 1 Basic circuit diagram of the air core series reactor

The HTS FCL system consists of two iron cores with conventional copper AC coils wound on the cores. The circuit that needs to be protected is connected in series with the AC coils of the FCL, as shown in Figure 2. A DC coil enclosing both cores is used to bias the cores into saturation under normal operating conditions, thereby providing a low value of steady-state inductance. Under a fault condition, the biasing by the HTS DC coil is reduced in response to the increased current in the load, thus causing the cores to become unsaturated. The impedance of the HTS FCL then changes instantly to a high value, thereby limiting the fault current to a prescribed maximum. In order to maintain a better distribution of the magnetic flux, the DC coil is often split in two separate coils in parallel, as depicted in Figure 2.

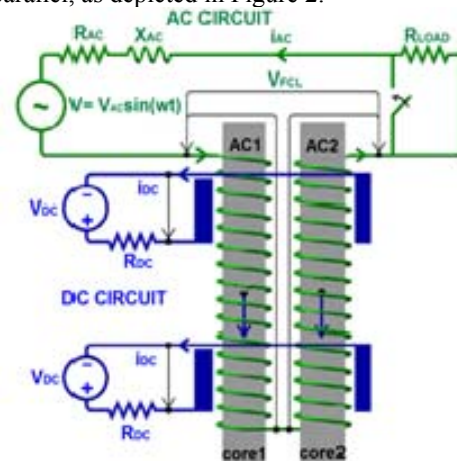


Figure 2 Basic circuit diagram of the HTS FCL

A two coil-core structure per phase is needed to limit the AC current. AC Coil 1 (AC1) is wound in the opposite direction to the DC coil whereas AC Coil 2 (AC2) coil is wound in the same direction as the DC coil (see Fig. 2). When the AC fault current is positive, the first coil-core structure limits the fault current, while the fault current is restricted by the second coil-core when the AC current is negative.

In this paper, test results made recorded for full scale HTS-FCL are shown. This HTS FCL was successfully tested and implemented in the UK power-grid for 11kV application. Additional specifications of the HTS FCL can be found in [3]



Figure 3 HTS FCL Full scale prototype for 11kV application

II. OPTIMIZATION OF THE HTS FCL

Utilization of mathematical optimization techniques enable the optimization of FCL designs against specific sets of criteria in the electromagnetic paradigm. The optimization strategy used in this paper is the evolutionary algorithm. This multi-objective strategy is based on the Pareto concept. The Pareto concept defines an optimum set of values while improving objective criteria without deterioration in any of the other objective criteria. When this improvement is no longer possible, the Pareto frontier curved is defined and the optimum set of values are achieved [4-6].

In this paper, the two optimization criteria for the HTS FCL are the voltage drop in the distribution grid and the cost of the apparatus. Both criteria are to be minimized and are assigned equal weights in the algorithm. The variables that can be optimized are related to the inductance of an air core coil

$$L_{\text{air core}} = \frac{N_{AC} \cdot A_{\text{core}}}{h_{AC}} \cdot \mu,$$

where N_{AC} is the number of turns, A_{core} is the cross sectional area of the core and the h_{AC} is the height of the AC coil. All these parameters together with the number of ampere turns of

the HTS DC coils make up the set of input variables to our optimization system.

Figure 4 shows the different optimum solutions of the HTS FCL design.

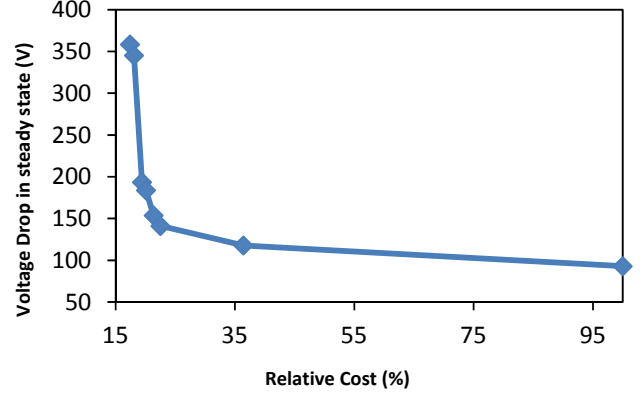


Figure 4 Pareto frontier optimization curve of the HTS FCL

The design with the lowest cost has a high voltage drop penalty, whereas the solution with the minimum voltage drop has high cost. The final design was chosen in the elbow of the curve, where the trade-off between voltage drop and cost was best suited relative to the required specifications.

III. PERFORMANCE AND MODEL VALIDATION

The overall performance of the HTS FCL was assessed by measuring the transient currents obtained with the FCL under short-circuit conditions. The HTS FCL and the series reactor were modeled using Finite element method (FEM) software. Table 1 shows the main parameters of the system.

Table 1
Circuit Design Parameters

Parameter	Value
Rated Voltage	11.3 kV
Nominal Current	1170 A rms
Line Frequency	50 Hz
R_{load}^*	10 k Ω / 5 Ω
R_{AC}	0.017 Ω
X_{AC}	1.03 Ω
I_{DC}	100 A
Prospective unlimited peak fault current (without FCL)	17.3 kA peak
Peak limited current (with the FCL in the Grid)	13.8 kA peak
X_{CLR}	0.3 Ω

The test for the HTS FCL was conducted in a high voltage laboratory. The test involved the implementation of the HTS FCL in a circuit as represented in Figure 2 and then applying a short-circuit fault. The standard test procedure does not apply any pre-fault current. Therefore a load of $R_{\text{load}} = 10$ k Ω was included in our model to simulate the test conditions of minimal pre-fault current. Figure 5 shows the excellent agreement between measurements on the prototype and the FEM model. This test did not provide comparative data for the air-core series reactor, but confirmed the validity of the simulation model. Theoretical data for the series reactor was also generated.

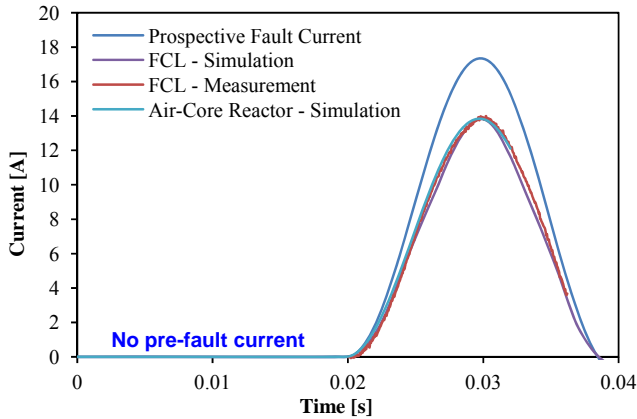


Figure 5 Short-circuit fault without pre-fault current

The prospective current maximum peak was 17.3 kA, whereas the limited current peak was measured as 13.8 kA. A reduction of 20 % was thus achieved.

Figure 6 and Figure 7 show the FEM simulations in order to compare the performance between air core series reactors and HTS FCL. For this simulation, a load of $R_{load} = 5 \Omega$ was used. Figure 6 shows the current before and during the fault, whereas Figure 7 shows the voltage across the two limiting systems under steady state conditions.

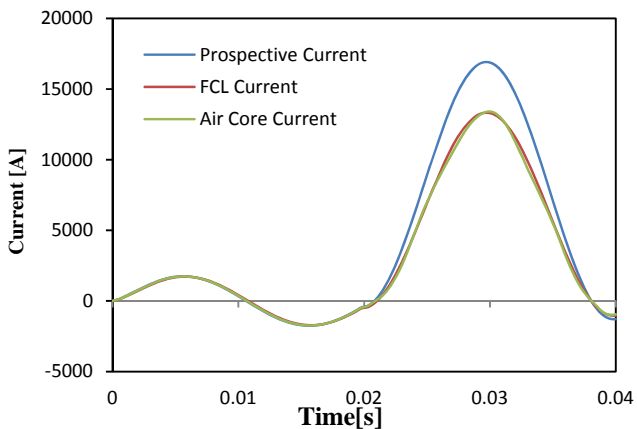


Figure 6 Short-circuit fault with pre-fault current

Under the new conditions, the current peak is 16.8 kA for the prospective fault current and 13 kA for the limited current. Both the FCL and the air-core reactor therefore achieve a fault current reduction of 22% .

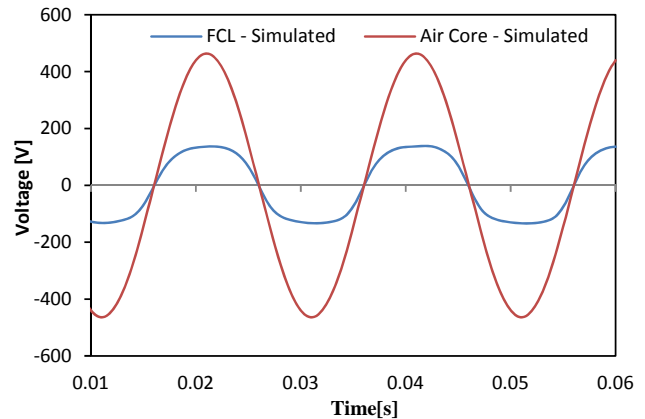


Figure 7 Voltage across the limiting systems

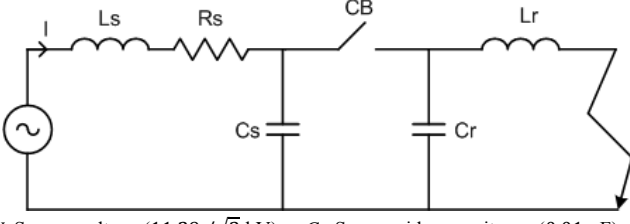
The voltage drop across the HTS FCL during the steady state is 114 Vrms, whereas the corresponding voltage drop across the air core series reactor was found to be 325 Vrms. By using the HTS FCL instead of the series reactor, the voltage drop in the distribution grid under normal operating conditions can therefore be reduced by 65%.

IV. STRESS ON THE CIRCUIT BREAKER DUTY DUE TO SERIES REACTORS

The use of series reactors could stress the interruption duty of the circuit breaker by introducing a fast transient oscillation in the TRV [7, 8]. This is due to the combination of both low capacitance and high inductance of the device.

The burden on a circuit breaker is a function of the magnitude of the interrupted current and the transient recovery voltage (TRV) [9]. Conventional series reactors reduce the current interruption rating of a circuit breaker. However, they can increase the rate of rise of recovery voltage (RRRV) and the peak TRV value to above that when the FCL is absent [9, 10]. A larger RRRV has a negative impact on the interrupting capability of the circuit breaker.

The transient recovery voltage response of the circuit depicted in Figure 8 is that of a double frequency transient [11]. The transient recovery voltage across the breaker represents the different voltage responses between the source side and reactor side of the breaker. Post interruption, the voltage across the source capacitance has a similar waveform profile as the source voltage. The voltage across the reactor capacitance is a decaying oscillatory signal representing the capacitor discharging through the reactor inductance. When there is no reactor present (i.e. fault at the breaker terminal), the capacitor is unable to discharge and hence the transient recovery voltage is equivalent to the voltage across the source capacitance.



V: Source voltage (11.29 / $\sqrt{3}$ kV) C_s : Source side capacitance (0.01 μ F)
 L_s : Source inductance (3.29 mH) C_r : Reactor side capacitance (500 pF)
 R_s : Source resistance (17.27 m Ω) L_r : Reactor inductance (1.14 mH)

Figure 8 Single-phase equivalent circuit diagram of a three-phase-to-ground symmetrical short circuit

The fault current of a network with a series reactor installed is given by

$$I_{FC} = \frac{U_n}{R_S + j\omega(L_S + L_R)}, \quad (1)$$

where U_n is the line-to-ground voltage of the source, R_S is the resistance of the source, L_S is the inductance of the source, L_R is the reactance of the reactor and ω is the network angular frequency. The network is assumed to be in a steady state condition prior to the fault, hence all capacitances are neglected [11]. Given the reduced fault current of a fault current limiter, the inductance of a series reactor designed to produce the same fault current reduction can be calculated using

$$L_r = \frac{U_n}{\omega I_{FC,fc1}} - L_s, \quad (2)$$

where $I_{FC,fc1}$ is the fault current of the network when a fault current limiter is installed. The source resistance is neglected in the calculation, since $X_s \gg R_s$.

In order to plot the transient recovery voltage profile of the circuit, the voltage across the source and reactor capacitance need to be calculated. The following formulas are valid for the first hundreds of microseconds after current zero and neglecting the damping of the system.

The voltage across the reactor side capacitor is given by

$$V_r = \frac{\sqrt{2}U_n}{\sqrt{3}} \frac{L_r}{(L_s + L_r)} \cos(2\pi f_{n,r}t), \quad (3)$$

where $f_{n,r}$ is the natural frequency of the reactor side of the circuit, given by

$$f_{n,r} = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (4)$$

The voltage across the source capacitor is calculated by subtracting the voltage drop across the source inductance from the source voltage:

$$V_s = \frac{\sqrt{2}U_n}{\sqrt{3}} \cos(2\pi ft) - \frac{\sqrt{2}U_n}{\sqrt{3}} \frac{L_s}{L_s + L_r} \cos(2\pi f_{n,s}t) \quad (5)$$

where f is the nominal system frequency and $f_{n,s}$ is the natural frequency of the source side circuit, given by

$$f_{n,s} = \frac{1}{2\pi\sqrt{L_s C_s}}. \quad (6)$$

The transient recovery voltage is the difference of the source and reactor voltages:

$$V_{TRV}(t) = V_s(t) - V_r(t). \quad (7)$$

Figure 9 shows the analytical result of the circuit in Figure 8. It is important to note that the oscillation damping due to the resistance of the circuit is not considered.

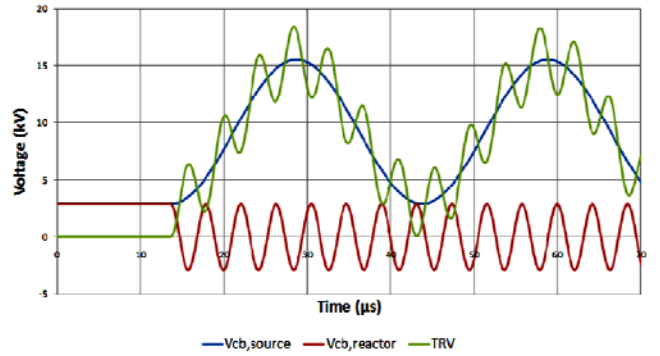


Figure 9 Analytically calculated transient recovery voltage profile for the circuit of figure

V. COMPARISON OF THE TRV OF SERIES REACTOR AND EQUIVALENT SATURATED CORE HTS FCL

The influence of the HTS FCL of Table 1 on the circuit breaker RRRV is compared to the results obtained for a series reactor which achieves the same fault current limiting. The TRV simulations for the FCL were conducted in PSCAD®. A specific model of the HTS FCL had to be built for these simulations.

The induced emf across each phase of the HTS FCL is a function of DC bias and AC load currents [12]. It can be represented by the following function:

$$emf(i_{ac}) = -n_{ac} A_{core} \frac{\partial B}{\partial i_{ac}} \frac{\partial i}{\partial t} = -n_{ac} A_{core} \mathfrak{Z}(i_{ac}, B_{sat}, I_{max}, K) \frac{\partial i}{\partial t} \quad (8)$$

$$-I_{max} \leq i_{ac} \leq I_{max}$$

$$emf(i_{ac}) = -L_{air} \frac{\partial i}{\partial t} \quad (9)$$

$$|i_{ac}| \geq I_{max}$$

where:

N_{AC} is the number of AC turns per coil,

A_{core} is the core cross section contained by the AC coil,

i_{AC} is the instantaneous line current,

B_{sat} is the magnetic flux density in the core material at saturation.

I_{max} is the maximum AC peak current needed to fully de-saturate the cores,

K accounts for the level of DC bias current,

L_{air} is the equivalent air-core inductance of a single AC coil,

\mathfrak{S} is the FCL function [10, 12].

Figure 10 shows the PSCAD® network model used in the simulations of the saturable-core HTS FCL. The capacitance on the HTS FCL side of the breaker is an order of magnitude higher than that of the series reactor due to the iron-core construction of the HTS FCL as opposed to the air-core series reactor.

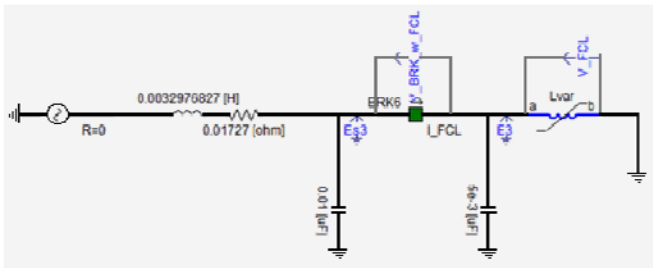


Figure 10 Saturable-core HTS FCL PSCAD® model

Figure 11 illustrate the TRV profiles for the series reactor and the saturable-core HTS FCL. A symmetrical fault current was used to produce these figures.

It is known that increasing the asymmetry of the fault current reduces the amplitude of the circuit breaker TRV.

Comparing Figure 11 and Figure 12, the HTS FCL and series reactor have the same TRV amplitude (18 kV). It is important to highlight that the amplitude of the voltage oscillation on the load side in the case of the series reactor ($V_{reactor}$) is significantly larger than the load side of the HTS FCL (V_{FCL}). The first peak of the series reactor load side voltage is approximately four times the amplitude of the load side voltage of the HTS FCL. The higher amplitude of the first TRV peak for the series reactor results in a larger initial RRRV, which affects the interruption capability of the breaker.

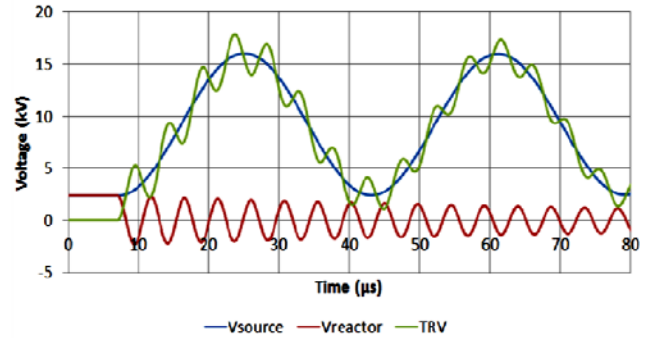


Figure 11 Series reactor transient recovery voltage profile, symmetrical fault current.

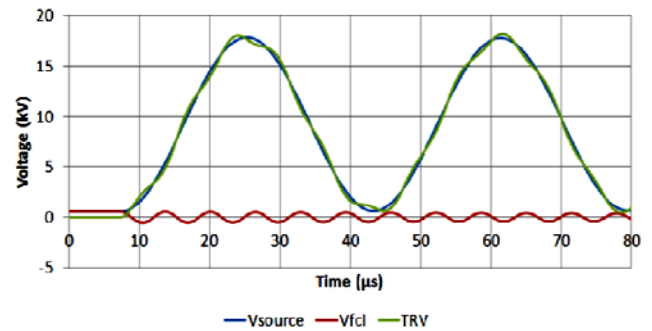


Figure 12 Equivalent saturable-core HTS FCL transient recovery voltage profile, symmetrical fault current.

VI. TEST VALIDATION

TRV Simulation results were validated by short-circuit tests on the HTS FCL and an equivalent series reactor performed in a power laboratory.

Figure 13 shows the TRV during a fault interruption. The TRV for the current limiting reactor (CLR) shows the double oscillation simulated in Figure 11. The high frequency oscillation is damped very rapidly. However it has a significant higher initial RRRV than the TRV oscillation produced during the same fault in the HTS FCL.

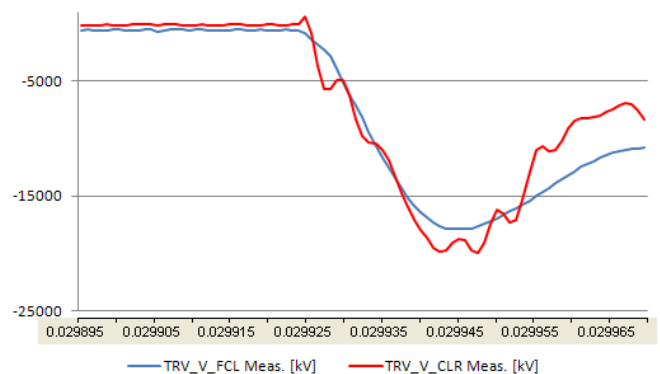


Figure 13 TRV measured during short circuit tests for a current limiter reactor (CLR) and a HTS FCL

VII. CONCLUSION

This paper shows the two main advantages of an HTS FCL compared to a series current limiting reactor. The series current limiting reactor suffers from high voltage drop during the steady state, whereas the HTS FCL maintains significantly lower levels. In addition, the high RRRV of the series reactor limits the interruption capabilities of the circuit breaker. The HTS FCL therefore offers a very attractive solution to the limitations of the series reactor.

REFERENCES

- [1] E. Leung, "Surge protection for power grids," *Spectrum, IEEE*, vol. 34, pp. 26-30, 1997.
- [2] J. R. S. S. Kumara, A. Atputharajah, J. B. Ekanayake, and F. J. Mumford, "Over current protection coordination of distribution networks with fault current limiters," in *Power Engineering Society General Meeting, 2006. IEEE*, 2006, p. 8 pp.
- [3] J. Cabanes Aracil, J. Lopez-Roldan, J. C. Coetzee, F. Darmann, and T. Tang, "Analysis of electromagnetic forces in high voltage superconducting fault current limiters with saturated core," *International Journal of Electrical Power & Energy Systems*, vol. 43, pp. 1087-1093, 2012.
- [4] E. Zitzler and L. Thiele, "Multiobjective evolutionary algorithms: a comparative case study and the strength Pareto approach," *Evolutionary Computation, IEEE Transactions on*, vol. 3, pp. 257-271, 1999.
- [5] M. L. Eckart Zitzler, Lothar Thiele, "SPEA2: Improving the Strength Pareto Evolutionary Algorithm," Zürich 2002.
- [6] M. L. Eckart Zitzler, Stefan Bleuler., "A Tutorial on Evolutionary Multiobjective Optimization, Metaheuristics for Multiobjective Optimisation," Berlin, 2004.
- [7] D. F. Peelo, G. S. Polovick, J. H. Sawada, P. Diamanti, R. Presta, A. Sarshar, and R. Beauchemin, "Mitigation of circuit breaker transient recovery voltages associated with current limiting reactors," *Power Delivery, IEEE Transactions on*, vol. 11, pp. 865-871, 1996.
- [8] T. A. Bellei, E. H. Camm, and G. Ransom, "Current-limiting inductors used in capacitor bank applications and their impact on fault current interruption," in *Transmission and Distribution Conference and Exposition, 2001 IEEE/PES*, 2001, pp. 603-607 vol.1.
- [9] E. Calixte, Y. Yokomizu, H. Shimizu, T. Matsumura, and H. Fujita, "Reduction of rating required for circuit breakers by employing series-connected fault current limiters," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 151, pp. 36-42, 2004.
- [10] J. Lopez-Roldan, A. C. Price, F. De La Rosa, and F. Moriconi, "Analysis of the effect of a saturable-core HTS fault current limiter on the circuit breaker transient recovery voltage," in *Power and Energy Society General Meeting, 2011 IEEE*, 2011, pp. 1-8.
- [11] A. Greenwood, Ed., *Electrical transients in power systems*. New York: Wiley Interscience, 1991, p. pp. Pages.
- [12] F. Moriconi, N. Koshnick, F. De La Rosa, and A. Singh, "Modeling and test validation of a 15kV 24MVA Superconducting Fault Current Limiter," in *Transmission and Distribution Conference and Exposition, 2010 IEEE PES*, 2010, pp. 1-6.