A New Pulsed Power Supply Topology Based on Positive Buck-Boost Converters Concept

Sasan Zabihi, Firuz Zare, Gerard Ledwich, Arindam Ghosh
School of Electrical Engineering, Built Environment and Engineering Department
Queensland University of Technology, GPO Box 2434
G.P.C., 2 George St., Brisbane, QLD, 4001, Australia

and **Hidenori Akiyama**
Graduate School of Science and Technology, Kumamoto University
Kurokami 2-39-1, Kumamoto 860-8555, Japan

ABSTRACT

Improving efficiency and flexibility in pulsed power supply technologies is the most substantial concern of pulsed power systems specifically with regard to plasma generation. Recently, the improvement of pulsed power supply has become of greater concern due to the extension of pulsed power applications to environmental and industrial areas. With this respect, a current source based topology is proposed in this paper as a pulsed power supply which gives the possibility of power flow control during load supplying mode. The main contribution in this configuration is utilization of low-medium voltage semiconductor switches for high voltage generation. A number of switch-diode-capacitor units are designated at the output of topology to exchange the current source energy into voltage form and generate a pulsed power with sufficient voltage magnitude and stress. Simulations carried out in Matlab/SIMULINK platform as well as experimental tests on a prototype setup have verified the capability of this topology in performing desired duties. Being efficient and flexible are the main advantages of this topology.

Index Terms — **Pulsed power supply, high voltage, current source, voltage source, power converter, DC-DC topology, plasma.**

1 INTRODUCTION

PULSED power is the accumulation of energy over a relatively long period of time and releasing it very quickly which is a process aiming to increase the instantaneous power. The characteristics of this pulse, including voltage level and rising time are determined based on the load requirements.

Although single shot based pulsed power generators with extremely high peak power have been considered initially for military and nuclear fusion applications, repetitively operated pulsed power generators with a moderate peak power have been recently developed mainly for industrial applications such as food processing, medical treatment, water treatment, exhaust gas treatment, concrete recycling, ozone generation, engine ignition, ion implantation etc [1, 2]. Marx Generators (MG) [3, 4], Magnetic Pulse Compressors (MPC) [5, 6], Pulse Forming Network (PFN) [7, 8], Multistage Blumlein Lines (MBL)[9, 10] etc, are the most popular technologies which have been utilized so far as pulsed power supply. Hiring aged methods and technologies besides lack of agreement between power supply and load properties cause major issues in pulsed power area. Not tacking utilization of advanced knowledge and recent approaches in power electronics and semiconductors into account was due to lack of necessity to improve power supply technologies during past decades. Efficiency, flexibility and intricacy are major drawbacks of these power supplies. Controlling power flow is a critical skill which can improve the efficiency of power supply systems. On the other hand these pulsed power systems require high voltage, high power switches in which their voltage blocking and switching time are limited. The switches technology utilized for pulsed power generation has varied with respect to the development of power semiconductor devices over, the past few decades. Thyristor, IGBT, MOSFET, etc are some of those switches mostly classified as solid state semiconductor switches [11-13]. Since pulsed power applications demand for high dv/dt, fast switches with short switching transients have critical role in pulsed power supply topologies [14]. The timescales of these transients are from nanoseconds to microseconds, including a switching transition of power semiconductor devices, commutating processes, and drive signal transmissions. These transient processes directly affect the performance and reliability of power electronic systems with imposed restrictions over power conduction [15].

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Most pulsed power applications have resistive-capacitive characteristics [16]; therefore, a current source topology seems to be a proper candidate to supply such loads. With respect to this issue a combination of current and voltage sources is considered in this paper to develop the initial concept of high voltage pulse generation with low voltage switches. The circuit depicted in Figure 1 reveals a general configuration for the proposed topology. Same sort of fast and low-medium voltage semiconductor switches and diodes are used between two energy storages in order to control the energy delivery process. In this configuration the inductor and the capacitors, which can be supposed as the current and voltage sources, are in charge of supplying energy and generation of appropriate voltage level and stress respectively.

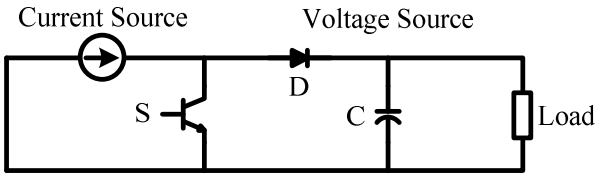


Figure 1. A general configuration of proposed concept.

2 CONFIGURATION AND ANALYSES

2.1 TOPOLOGY

2.1.1 GENERAL CONFIGURATION

The topology considered in this paper is based on the positive buck-boost converter concept. The general concept of this topology is presented in Figure 2.

An ac-dc converter rectifies grid ac voltage into a dc voltage and supplies the rest of the circuit. The source voltage charges an inductor, L, through switches, S_S, and S_1, S_2…, S_n, composing a current source. The level of current, stored in the inductor during charging mode, can be controlled via an appropriate duty cycle of S_S.

A freewheel diode, D, which is connected between the switch and the inductor, conducts the current in order to provide a current loop and keep the current constant, while S_S is switched off. The switches, S_1, S_2…, S_n, are connected to a series of capacitors through diodes which compose switch-diode-capacitor units. These units in a group association act as a combined voltage source and generate desired high voltage at the output. The inductor current flows through the unit's switches while they are on. As soon as the switches are turned off, the inductor current flows to the capacitors through the diodes. The received energy from the current source is stored in the capacitors in the form of voltage.

Most pulsed power applications have resistive and capacitive properties which can be modeled as a sample load with a capacitor, C_{Load}, a switch, S_{Load}, and two resistors, R_{1Load} & R_{2Load} as shown in Figure 2. The capacitor represents the capacitive specification of the loads and switching between large and small resistors, R_{1Load} & R_{2Load}, simulates the break down phenomena happening while pulsed power applies to the loads.

As shown in Figure 3, a double unit configuration is investigated in this paper as a simple model. The results can be extended for a multi unit topology.

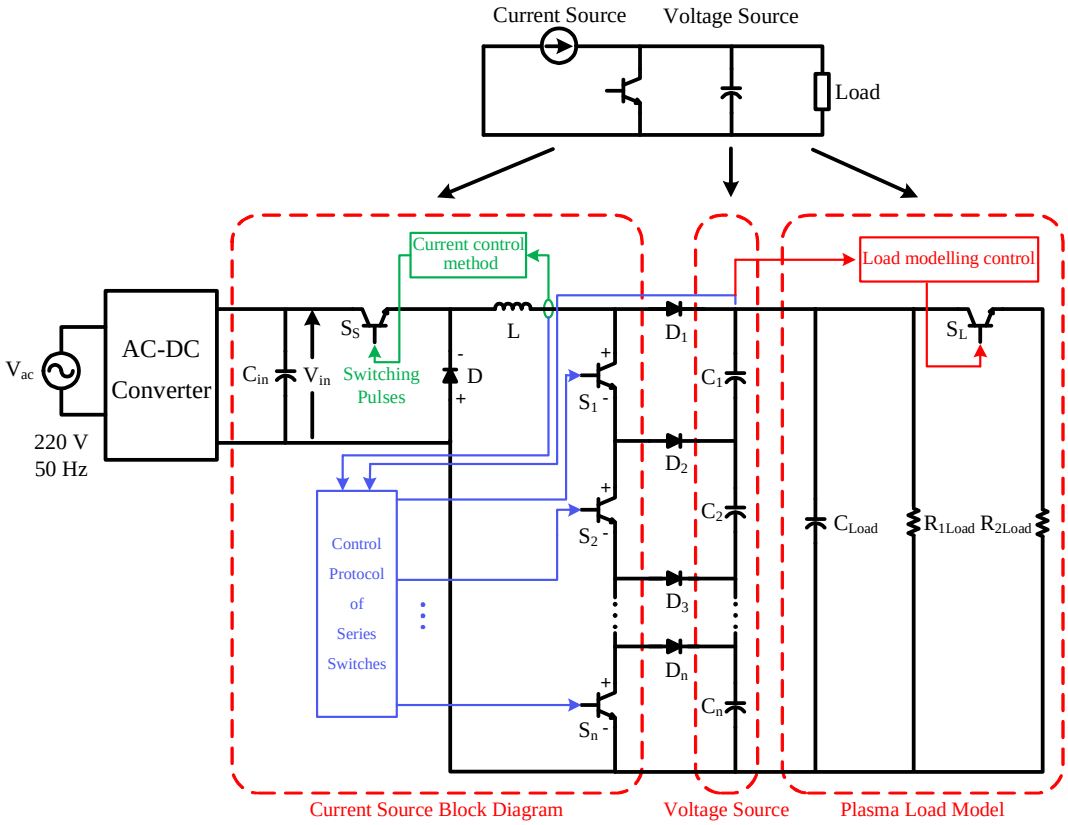


Figure 2. Pulsed power supply configuration with multi switch-diode-capacitor units.

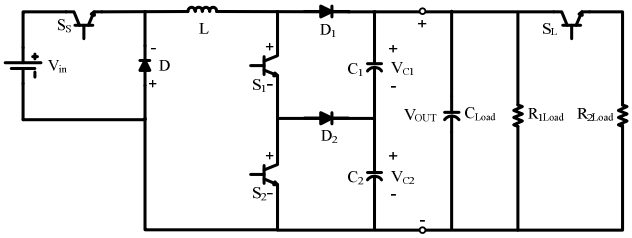


Figure 3. A pulsed power supply with two switch-diode-capacitor units and a non-linear load.

2.1.2 SWITCHING MODES

The operation modes of this topology are separated into two major groups. Switching states depicted in Figures 4a and 4b and Figures 4c and 4d are classified in current source category and voltage source category, respectively.

2.1.2.1 FIRST MODE: CHARGING INDUCTOR (S_S: ON, S_1: ON, S_2: ON)

As demonstrated in Figure 4a, in this switching state, all the switches, including current source switch, S_S, and units switches, S_1 & S_2, are turned on to increase the inductor current. Therefore the input voltage, V_{in}, appears across the inductor and the charging time can be calculated as follows.

$$V_L = V_{in} - (V_{S_S} + V_{S_1} + V_{S_2}) \tag{1}$$

$$V_L = L\frac{di}{dt} = L\frac{\Delta i}{\Delta t} \tag{2}$$

If the inductor is supposed to be with no initial current charge and $\Delta i = I$ then $\Delta t = \frac{L \cdot I}{V_L}$

2.1.2.2 SECOND MODE: CIRCULATING THE INDUCTOR CURRENT (S_S: OFF, S_1: ON, S_2: ON)

As soon as the inductor current crosses a defined amount, the control system turns off the current source switch, S_S, and disconnects the input voltage source, V_{in}, from the rest of topology. Henceforth, the freewheel diode, D, conducts and lets the inductor current to circulate through S_1 & S_2. In this mode, which is illustrated in Figure 4b, the low voltage drop across the diodes and switches discharges the inductor moderately. As the total voltage across the inductor is not significant, the discharging effect can be neglected and the circulating current is considered to be constant. This switching state keeps the current stored in the inductor and allows the load system to be prepared for the next cycle of energizing.

$$V_L = -(V_D + V_{S_1} + V_{S_2}) \tag{3}$$

This is a mandatory switching mode but the converter can stay in this mode for a short time in order to minimize conduction loss. Then the converter can be switched to the third switching mode if the load is prepared to be energized. Neglecting this switching state in order to avoid the conduction losses raises stability concerns and it is indeed a safety state which is necessary for this system. During this switching mode, the inductor is isolated from the source by turning S_S off, giving the possibility of disconnecting input voltage from the load during power delivery period.

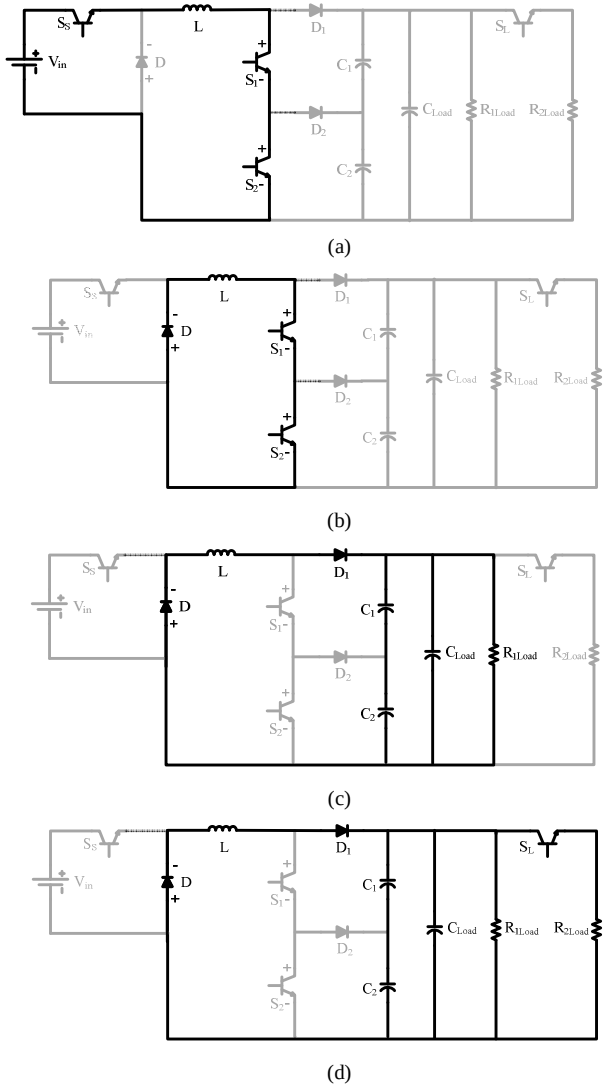


Figure 4. Switching states of the proposed power supply circuit (a) Inductor charging (b) Circulating the inductor current (c) Charging the capacitors (d) Supplying the load.

Therefore, even if there is an arc occurring at the load side, there will be no chance to waste a large amount of energy through the input source.

2.1.2.3 THIRD MODE: CHARGING CAPACITORS (S_S: OFF, S_1: OFF, S_2: OFF)

In this switching state, the current source delivers the inductor current to the capacitors and charges them. As exhibited in Figure 4c, the unit's switches, S_1 & S_2, are turned off in this mode and the inductor current is pumped into the capacitors and charges them to a certain level defined by the load.

$$\frac{\Delta V_{C_i}}{\Delta t} = \frac{I_{C_i}}{C_i} \quad \Rightarrow \quad \Delta V_{C_i} = \frac{I_{C_i}}{C_i} \cdot \Delta t \tag{4}$$

During this state, in reality, the resistivity of load considerably collapses due to the application of pulsed power to the load and plasma generation reaction. A plasma phenomenon has been modeled by decreasing the load

resistance from R_1 to R_2 through switch S_L as demonstrated in Figure 4d. The required energy is delivered to the load from the voltage and current sources in this mode. The capacitor bank and the inductor are discharged subsequently according to the proportion of energy stored in them. Once the load supplying process is finished, the topology can switch from the supplying mode to the charging inductor mode with no concern.

2.1.2.4 FOURTH MODE: SEPARATELY CHARGING THE CAPACITORS (S_S: OFF, S_1: OF, S_2: OFF)

This topology is also flexible in terms of charging capacitors separately. In this scenario, the unit's switches will be turned off subsequently and gives the feasibility of charging the capacitors in an appropriate sequence. As can be seen in Figure 5, S_2 is turned off while S_1 is still on in order to charge C_2 through D_2 in this mode. The achievement of this strategy is having a voltage storage continuously charged which provides a basic voltage level for the load. In the present model, C_2 is responsible for this function, so the other capacitors are dedicated to providing desired voltage stress.

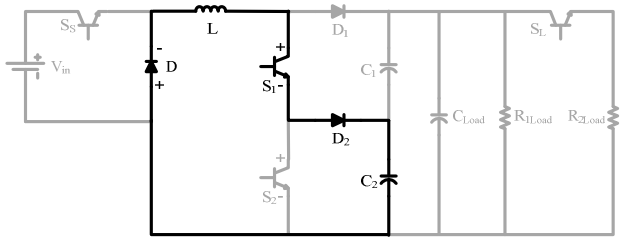


Figure 5. Switching state of charging capacitors separately

2.1.3 CIRCUIT ANALYSES

The voltage sharing of capacitors in different operation modes can be calculated as follows:

While S_1 and S_2 are turned on and off separately, there will be an initial charge in C_2, shown with fundamental voltage V_f in the following equations.

While C_2 become charged in the fourth mode (S_S:OFF, S_1:ON, S_2:OFF, S_L:OFF):

$$V_{C_1}(1) = 0 \tag{5}$$

$$V_{C_2}(1) = V_f \tag{6}$$

While S_1 is turned off, as well as S_2 in the next mode (S_S:OFF, S_1:OFF, S_2:OFF, S_L:OFF), the voltage sharing of capacitors would be:

$$V_{C_1}(2) = \frac{C_2 V_{out} - C_2 V_f}{C_1 + C_2} \tag{7}$$

$$V_{C_2}(2) = \frac{C_1 V_{out} + C_2 V_f}{C_1 + C_2} \tag{8}$$

Whereas V_{out} is the required voltage level for the load break down.

When the load discharges the capacitors energy, the capacitor allotted for dv/dt generation, C_1, will be fully discharged and then get negative charge from the capacitor allocated to fundamental voltage , C_2, since it still has energy and delivers it to the load which charges C_1 negatively. (S_S:OFF, S_1:OFF, S_2:OFF, S_L:ON):

$$V_{C_1}(3) = \frac{-C_2 V_f}{C_1 + C_2} \tag{9}$$

$$V_{C_2}(3) = \frac{C_2 V_f}{C_1 + C_2} \tag{10}$$

In a specific case when C_1=C_2, the above equations change in to:

(S_S:OFF, S_1:ON, S_2:OFF, S_L:OFF):

$$V_{C_1}(1) = 0 \tag{11}$$

$$V_{C_2}(1) = V_f \tag{12}$$

(S_S:OFF, S_1:OFF, S_2:OFF, S_L:OFF):

$$V_{C_1}(2) = \frac{V_{out} - V_f}{2} \tag{13}$$

$$V_{C_2}(2) = \frac{V_{out} + V_f}{2} \tag{14}$$

(S_S:OFF, S_1:OFF, S_2:OFF, S_L:ON):

$$V_{C_1}(3) = \frac{-V_f}{2} \tag{15}$$

$$V_{C_2}(3) = \frac{+V_f}{2} \tag{16}$$

The separate switching strategy has a number of advantages in comparison with simultaneous switching. As already mentioned, a fundamental dc voltage level which is almost invariable can be generated in this method. This source of energy will be helpful to save a part of the supplying process and increase the frequency of pulse supply.

2.2 CONTROL STRATEGIES

Switches used in this power supply have two different functions. A single switch at the front side of topology, S_S, can charge the inductor at a certain level. A range of switches, S_1 & S_2, at the output of the topology either circulates the current or conducts it to the capacitors. The switch used for modeling the plasma break down phenomena in the load, S_L, is controlled at a certain voltage level. As expected, each type of these switches is functionalized under a specific principle in order to meet assigned duties. A flowchart, shown in Figure 6, describes the logic of decisions which generate control signals to charge the inductor and capacitors.

2.2.1 CURRENT SOURCE CONTROL

The first stage is charging the inductor through the front part of the circuit. Assuming the switches S_1, and S_2 are on, the inductor can be charged when the switch S_S is turned on. The controller measures the inductor current and turns off the switch when the inductor current reaches I_{max}. In this case the energy stored in the inductor is $\frac{1}{2} L \cdot I_{max}^{\ 2}$.

As can be found in the flowchart shown in Figure 6, turning S_S off which means a transition between inductor charging and current source modes is carried out with a comparison

between actual inductor current and a specific amount, I_{max}, set as charging limit. Whereas, S_S is turned on while a load supplying cycle is spent and the energy is delivered to the load in this cycle. This will be detected for the system as soon as output voltage becomes less than a specific level; V_{min}. V_{min} is relevant to the load energy demand and determined by the programmer. The only concern which restricts V_{min} determination is diode's breakdown voltage, V_d.

$$V_{min} \leq V_d \quad (17)$$

To increase V_{min} level, it is possible to connect a number of low voltage diodes in series. In this way, the flexibility of stopping load supply in higher voltages will be brought to this configuration as another advantage.

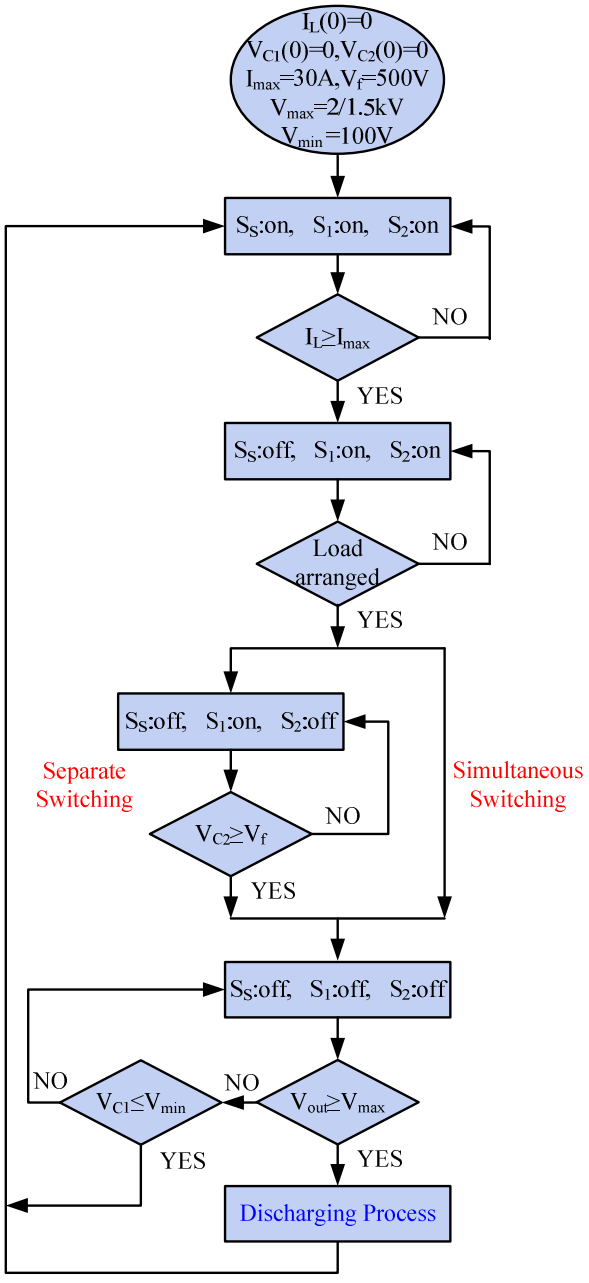


Figure 6. Flowchart of the control algorithm.

2.2.2 VOLTAGE SOURCE CONTROL

There are two control strategies, simultaneous and separate switching, applicable for this range of switches. Each has its own features and benefits.

Initially, the simultaneous switching method is considered to demonstrate the performance and the capabilities of this topology. In this method, all unit's switches will be turned off together after the inductor is fully charged. As a result, the inductor current will be pumped into all output capacitors and will charge them at the same time. Each capacitor generates a specific dv/dt and voltage level with respect to the capacitor amount. Assuming similar capacitors, the eventual voltage level will be shared among all capacitors equally. Pulsed power will be generated and applied to the load which subsequently discharges voltage and current sources. This trend will be repeated for the next pulse supplying cycles. The simulation results of this strategy are displayed in Fig 9.

Separate switching is another scenario which can be considered for controlling unit's switches and bringing inevitable advantages for this topology. In this switching strategy, unit's switches are turned off subsequently and as a consequence let the capacitors to be charged separately. This flexibility is particularly beneficial in the case of asymmetrical capacitors. In this feature, it is possible to assign different duties to different capacitors and recharge them with this respect. As an illustration, suppose that C_2 is allocated to provide a fundamental voltage level. On the other hand C_1 is allotted for providing required dv/dt. In this regard, C_2 should be appointed more capacitive than C_1. Here in this study, C_2 is determined ten times C_1. As already discussed in the switching modes, S2 is switched off while S1 is still on and conducts the current. As the circuit indicates in Figure 5, the current flows to C_2 through D_2 and charges it up to a specific level. Just after charging C_2, S_1 is switched off as well and allows the inductor current to be conducted through D_1 and charges both C_1 & C_2 simultaneously. Since C_2 is more than C_1 a similar current will charge it less than C_1 in a definite time. Therefore, the level of voltage provided by C_1 is significantly higher than that by C_2. In this regard, C_1 is dedicated to dv/dt, and C_2 is assigned for a basic and rather unvarying voltage level. The current and voltage waveforms accompanied by switching signal patterns of circuit controlled with this principal are exhibited in Figure 7.

2.2.3 LOAD MODELLING CONTROL

Load switch, S_L, is turned on when the output voltage reaches a specific voltage level. Therefore the resistivity of load suddenly collapses by turning S_L on, in order to simulate a plasma phenomenon. On the other hand, S_L becomes off while the reaction ends.

Discharging process appeared at the bottom of control algorithm flowchart is a safety procedure considered in situation of no prosperous plasma reaction. Once the output voltage increases to more than V_{max} level in these conditions, an external load will be connected to the power supply output and discharges the stored voltage. V_{max} selected with respect to the voltage tolerance of capacitors and diodes is almost 20% more than the voltage level in which plasma is expected to take place. In these circumstances, the diodes D, D_1, D_2

should tolerate high levels of voltage since the inductor current is supposed to be finished and the output voltage locates across D and D_1. As can be seen in Figure 4c and Figure 5, these diodes as well as D_2 should have breakdown voltages in an appropriate range in order to handle high levels of voltage

2.3 COMPONENTS DETERMINATION AND ENERGY DISCUSSION

Efficiency is the main concern when designing a power supply for pulsed power applications. To have the most possible efficient configuration, the topology structure, control algorithm and components sizes should be in the best correspondence with the application attributes and demands. In this configuration, having the least energy losses is considered in the topology in addition to the flexibility of the equipment, which needs to be adjusted for a diversity of pulsed power applications. The inductive and capacitive components (L & C_i), should be selected appropriately in order to both satisfy load requirements and avoid energy wasting. As the output voltage level and stress and delivered energy are defined by the load, the elements sizes can be determined with regard to those parameters.

The output equivalent capacitor $C_{eq} = C_1 \| C_2 \| \cdots \| C_n$ should be at least ten times the load capacitance to prevent any

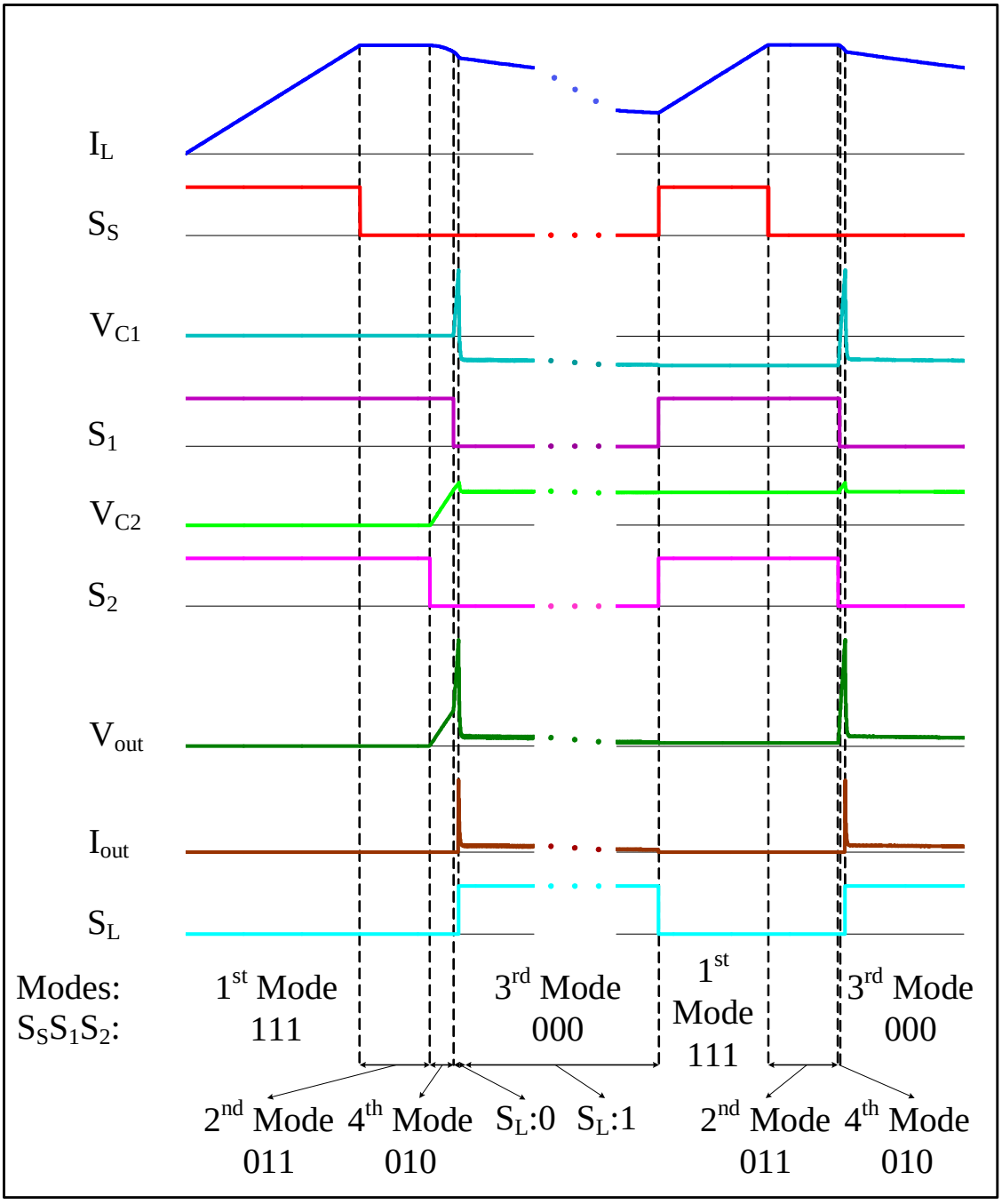


Figure 7. Current and voltage waveforms accompanied by relevant switching signals pattern in separate switching strategy.

loading problem. On the other hand, the equivalent capacitance needs to be as small as possible to generate voltage level and stress demanded by the load. Thus,

$$C_{eq} = 10\, C_{Load} \tag{18}$$

If the capacitors, C_i, are supposed identical then $C_{eq} = \frac{C_i}{n}$:

$$C_i = 10n \cdot C_{Load} \tag{19}$$

n is the number of switch-diode-capacitor units which is determined by the switches voltage and the demanded output voltage.

Assuming the inductor current is constant during the capacitor charging mode, the voltage stress can be calculated as follows.

$$I_L = (C_{eq} + C_{Load}) \frac{dV_{out}}{dt} \tag{20}$$

In the last stage, the demanded energy stored in the inductor defines the inductance value.

$$\frac{1}{2} L \cdot {I_L}^2 = E_{Load} \tag{21}$$

Finally, the recovery time for inductive and capacitive components and the frequency of pulsed power generated by the power supply can be determined as follows:

$$T_{r\_L} = \frac{L \cdot I_L}{V_{in}} \tag{22}$$

$$T_{r\_C} = \frac{(C_{eq} + C_{Load}) \cdot V_{out}}{I_L} \tag{23}$$

$$T_{r\_LC} = \frac{L \cdot {I_L}^2 + (C_{eq} + C_{Load}) \cdot V_{out} \cdot V_{in}}{V_{in} \cdot I_L} \tag{24}$$

In repetitive pulse generation, a time interval is designated to the load to be prepared for the next supplying cycle. For instance, in plasma generation, produced plasma needs to be exhausted and the reactor should be filled with fresh material. This interval is defined by T_{r_Load} in these equations. The frequency of load supply with pulsed power relies significantly on the load features and requirements, T_{r_Load}, but cannot be more than the recovery frequency of the power supply.

$$f_{s\_\max} < \frac{1}{T_{r\_LC} + T_{r\_Load} + T_d} \tag{25}$$

Load's capacitive and resistive characteristics in the interval of plasma phenomena define discharging time for the inductor (T_d). The inductor current in a load supplying cycle is shown in Figure 8 with detailed time intervals.

Regarding the above determinations, a model has been designed in Matlab/SIMULINK platform to analyze the performance of the proposed circuit. The detailed specifications of the circuit are given in Table 1.

Table 1. Specifications of the modelled circuit

V_{in}	*200V*	C_1	*10nF*	R_{1Load}	*10M Ω*	C_{Load}	*1nF*
L	0.6mH	C_2	100nF	R_{2Load}	10 Ω	f_S	2kHz

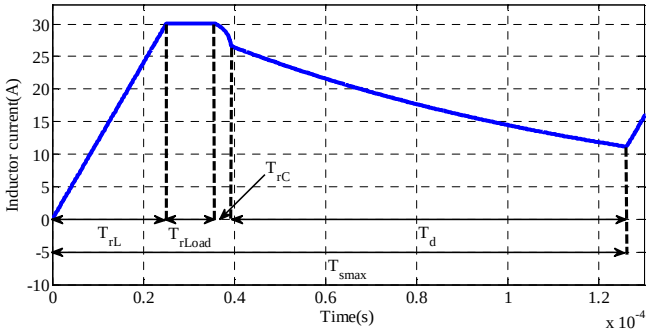


Figure 8. Times monitoring in a load supplying cycle.

These results indicate how the topology decreases the energy losses and improves power efficiency. For example, presume that the current source and the units switches, S_S & $S_1,\ldots,S_n$, get closed when the inductor still delivers 10 A to the load. This means 100 volt still exists across the 10 Ω load which is named as $V_{out\text{-}off}$. This voltage and the remaining inductor current can be stored in these components and be used in the recovery period of the next cycle. Therefore, no energy will be wasted in this topology in the process of delivering energy. Based on this issue, the power losses will be restricted to switching and conduction losses and the efficiency of this power supply in pulsed power supplying systems can be considered remarkable.

3 SIMULATION RESULTS AND ANALYSES

Several simulations at different conditions have been carried out to verify the validity of the proposed topology performance. The input voltage level, the components size, the inductor current magnitude and the load breakdown resistivity are the parameters varied in an extensive range to study the topology performance in different situations. The results presented in this part are revealed for two different switching strategies.

3.1 SIMULTANEOUS SWITCHING

In this case, the inductor is charged up to 30A and kept charged in this level until the load becomes prepared for the supplying cycle.

Then S_1 and S_2 are switched off simultaneously, allowing the inductor current to be pumped into the capacitor bank. The inductor energy delivered to the capacitors is exchanged to the voltage form. The generated dv/dt is in proportion with the inductor current level and the equivalent capacitors size. In this respect, the output DC link's voltage is charged up to 2kV, while each capacitor generates 1kV. This level of voltage, accompanied by an appropriate slope and rise time, dv/dt, is critical for the modeled load and causes a breakdown phenomenon in the load. Thus, load resistivity is markedly dropped and consumes the stored energy. Consequently, the capacitors are discharged in a considerably short time stint because of a very small time constant.

$$\tau = R \cdot C \tag{26}$$

The capacitors are not fully discharged because the inductor still supplies the load with the current. This current magnitude

times load resistivity creates a voltage across output capacitors during this period. The inductor is discharged afterwards because of a greater time constant.

$$\tau = \frac{L}{R} \tag{27}$$

The voltage remained at the output is also shared equally between two capacitors. This supplying process can be stopped at anytime and this moment is determined by the load demand for energy. The graphs exhibited in Figure 9 demonstrate the inductor current, the capacitors and the output voltage and the load current for a pulse generation moment respectively.

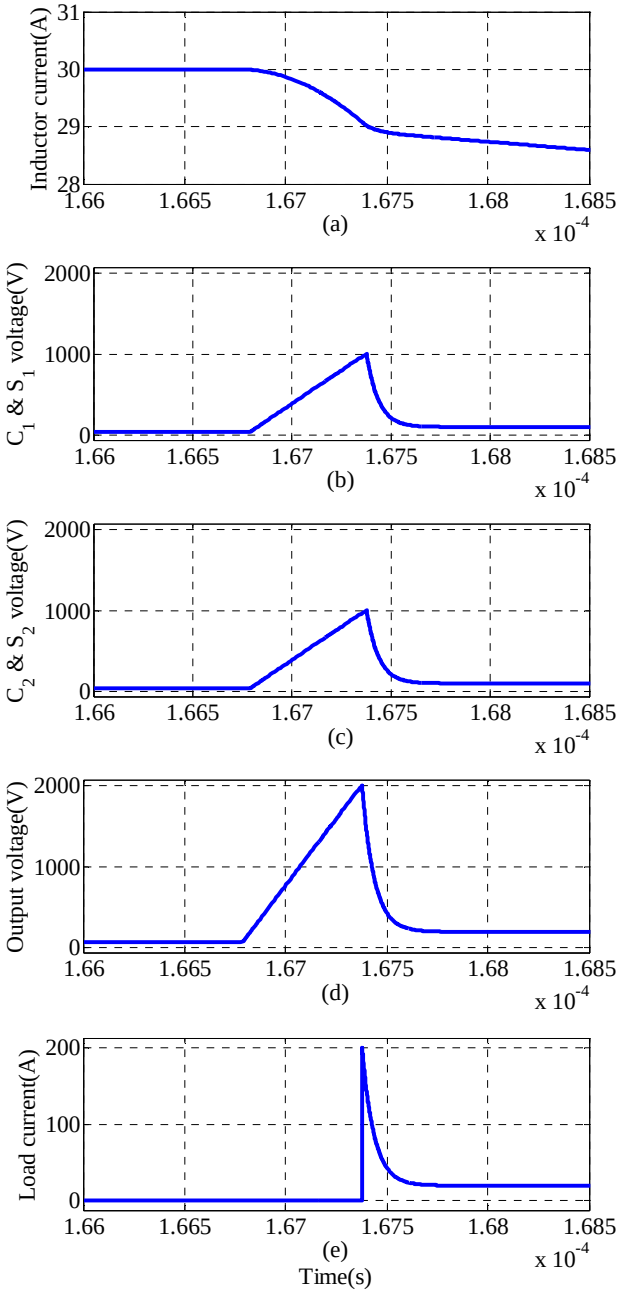


Figure 9. Output voltages and currents of power supply under simultaneous switching algorithm, (a) Inductor current (A), (b) C_1 & S_1 voltage (V), (c) C_2 & S_2 voltage (V), (d) Output voltage (V), (e) Load current (A).

3.2 SEPARATE SWITCHING

In the next case, the unit's switches are turned off separately, based on a particular logic, in order to charge asymmetrical capacitors for a specific purpose. The relevant results to this strategy are shown in Figure 10 in detail. In this scenario, different functions are defined for each capacitor. The capacitor which is opted larger is responsible for storing a definite amount of energy and serving an almost continuous level of voltage. The smaller one will be charged afterwards and is in charge for dv/dt. The discharging process is almost the same as the previous one except for voltage sharing at the end of the process. The smaller capacitor is discharged with a lower time constant than the bigger one.

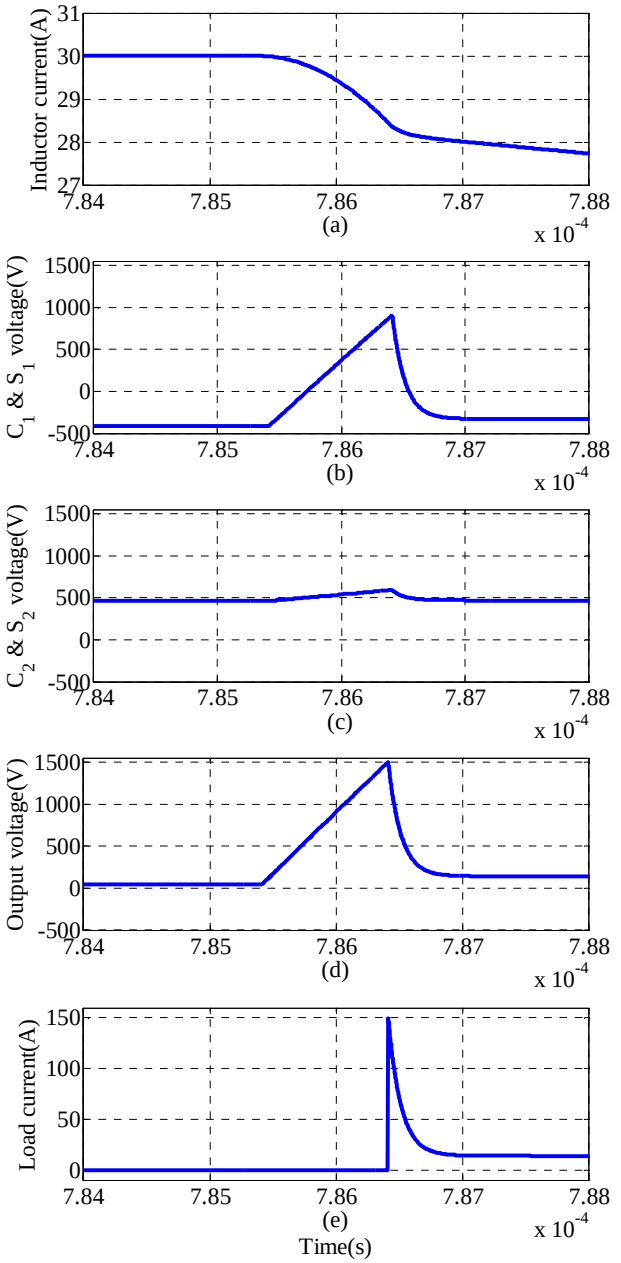


Figure 10. Output voltages and currents of power supply under separate switching algorithm, (a) Inductor current (A), (b) C_1 & S_1 voltage (V), (c) C_2 & S_2 voltage (V), (d) Output voltage (V), (e) Load current (A).

Although it has been charged to a higher voltage level, in comparison with the other capacitor, it will be discharged faster due to the lower time constant. C_2 is still charged while C_1 becomes fully discharged. Therefore, C_2 continues to deliver energy to the load through C_1 and this energy will charge C_1 with a negative polarity. This trend will be continued until the inductor is fully discharged. During this period, the output voltage, which is the resultant voltage of capacitors, is inductor current times the load resistor. At the end of this process, the output voltage will intend to be zero, corresponding with the inductor current reduction, while C_1 and C_2 are charged with negative and positive voltage respectively. This voltage balance creates initial provisions for the next supplying cycle of the circuit. The next supplying cycle starts with the inductor recovery modes and the topology will subsequently switch to capacitors separate charging mode. Although the expectation is the conduction of D_2 and recharging of C_2, D_1 conducts the inductor current due to a positive voltage caused by C_1 negative voltage across it. Thus C_1 and C_2 are recharged simultaneously but with different time constants. This procedure continues as far as C_1 voltage crosses zero level which is the time that the voltage across D_1 turns to be negative. Therefore D_1 stops conduction and D_2 conducts for the rest of this switching state. The next switching state commences while C_2 is charged up to the fundamental voltage level, V_f .

Once C_2 voltage becomes equal to this specific amount, S_1 will become off in order to charge C_1 as well as C_2. Although both capacitors are charged again in this mode the main goal of this switching state is charging C_1 to provide a desired dv/dt for a load. This concern is satisfied due to insignificancy of C_1. As soon as demanded voltage level accompanied by an appropriate dv/dt is generated the break down phenomena happens in the load and the accumulated energy will be delivered to the load. The supplying process can be stopped in any stage by turning S_1 and S_2 on. These sequences are repeated in all supplying cycles.

4 EXPERIMENTAL RESULTS

To investigate the validity and accuracy of the proposed topology and the control algorithm, a laboratory prototype has been developed with double switch-diode-capacitor units at the output of the converter. A photo of mentioned experimental setup including power and control boards, and the switches' drivers can be seen in Figure 11.

SEMIKRON products, SK50 Gar 065 and SK25 GB 065, are utilized as semiconductor components in the power circuit. SK50 Gar 065 consists of an Insulated Gate Bipolar Transistor, (IGBT) and a power diode module which are suitably arranged for buck configuration. This module is used in the power board as the front side switch and diode, S_S and D. SK25 GB 065 is also comprised of two IGBTs connected in series together. This composition is properly fitted to the output units design and consequently hired as the output switches, S_1 and S_2, in this converter. The controller for this setup has been developed utilizing an NEC 32-bit 64MHz V850/IG3 micro-controller.

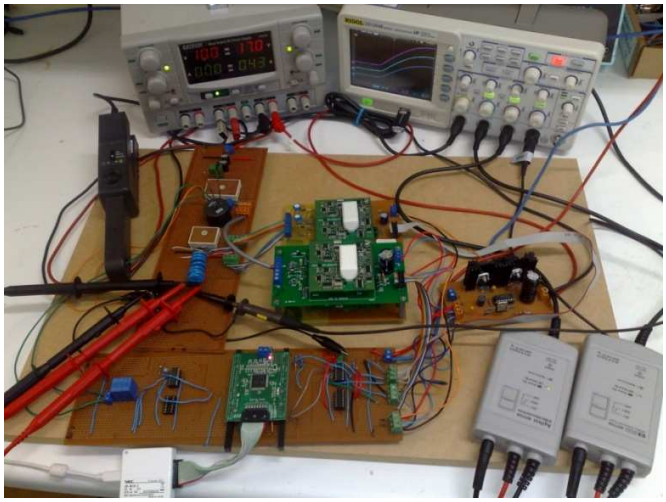


Figure 11. Laboratory prototype of pulsed power supply with double switch-diode-capacitor units.

Skyper 32-pro (SEMIKRON) is used as a gate drive circuit, which can drive two solid state switches independently and is compatible with the utilized IGBT modules.

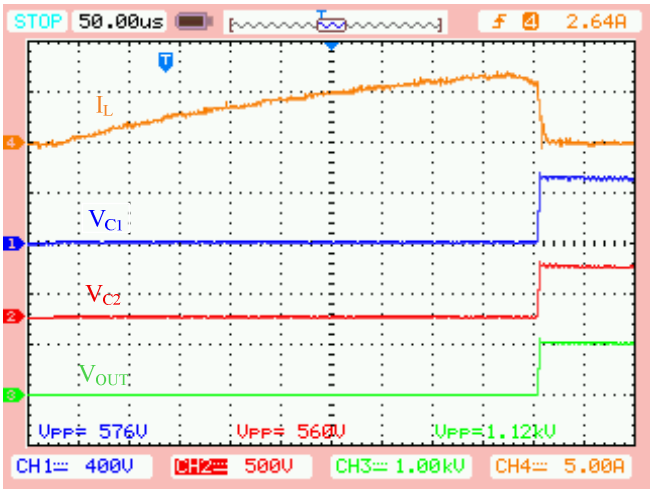
The laboratory setup in this study is designed in order to generate an output voltage level around one kilo volt. The IGBTs assembled in the SK25 GB 065 can withstand 600 V each, and based on this fact 1 kV is designated as the ultimate voltage level of power supply in order to have an appropriate safety margin. There are also other power switches with voltage ratings up to 1.5kV available commercially which can be utilized in this topology to develop the voltage escalating skill. This 1 kV level is also determined due to power supply and measurement equipment restrictions, as well as protection concerns. Hardware with such features complies with the initial purpose of experimental test and provides sufficient evidences to validate the true performance of proposed topology. The specifications of the components used in this prototype besides assigned adjustment level for the control of inductor current are given in Table 2.

Table 2. Specifications of the laboratory prototype circuit.

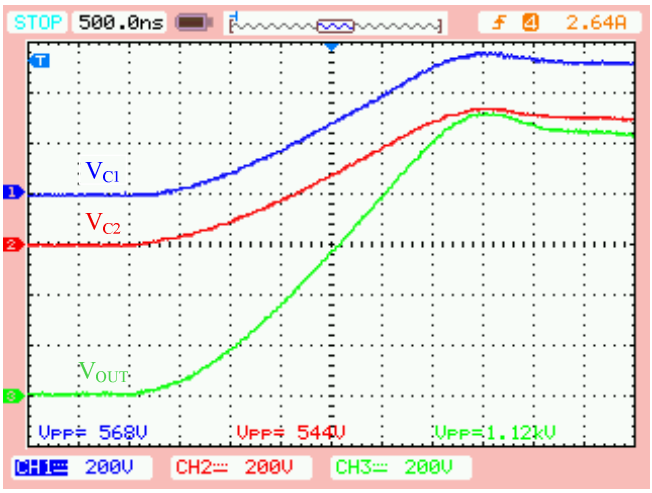
V_{in}	L	C_1	C_2	I_{Lmax}
15V	0.4mH	10nF	10nF	7A

The captured results are demonstrated in Figure 12a & b. As can be seen in Figure 12a, the inductor is charged up to 7 A, while the energy exchange process starts when the current is declined to 6 A. This reduction happens during circulating current mode. By turning S_1 and S_2 off, the inductor current flows into the capacitors and charges them up to 1.12 kV. The output voltage is split pretty equally across both capacitors since each capacitor is almost charged up to 560V. It indicates that the voltage sharing between the capacitors is rather done properly. On the other hand, a focused perspective in a more limited time frame, Figure 12b, gives a better vision of voltage rising trends. The low dv/dt in this test is due to a low inductor current level and can be markedly improved by raising the current level.

As anticipated, a portion of delivered energy is wasted during charging process due to conduction and switching losses. Active and passive components including power



(a)



(b)

Figure 12. Inductor current, capacitors and output voltages.

switches and diodes as well as circulating circuit normally consume a part of energy. In this case, comparing the stored energy in the inductive and capacitive elements reveals that the energy loss during exchanging energy procedure is considerable. Utilizing more efficient components can influence the efficiency of whole converter substantially.

5 CONCLUSION

This paper presents a current source based topology for pulsed power applications. A range of switch-diode-capacitor units connected in series together and in cascade to the current source is responsible for generating high voltage and high dv/dt. In this regard, both current and voltage sources are considered and utilized in this configuration as power sources despite of having distinguished duties. The novel contribution in this configuration is hiring low-medium voltage switches to tolerate a high voltage at the output. In addition, this topology has the flexibility of being easily adjusted for a wide range of pulsed power applications. Having control over power delivery to the load is another advantage of this power supply, which makes it thoroughly efficient. The proposal topology's true performance is investigated through several simulation models and the acquired results confirm the validity of this model to cover all desired duties. A laboratory prototype is also tested and the attained results have verified the initial concept of this configuration in generating high voltage pulses.

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Sasan Zabihi (S'09) was born in Iran in 1980. He received the B.Sc. degree in electrical engineering-telecommunication, from KhNT University of Technology, Tehran, Iran, in 2003 and the MSc degree in electrical engineering-power Electronics, from Mazandaran University, Babol, Iran in 2006. Since 2008, he has been pursuing the Ph.D. degree at Queensland University of Technology (QUT), Brisbane, Australia. In 2007, he joined Hadaf Institute of Higher Education in Sari, Iran, as a researcher and lecturer. His current research interests are Pulsed power and High voltage power supplies while he has been working in other power areas including Power electronics topologies and their applications in FACTS, as well as Power Quality and Renewable Energies.

Firuz Zare (M'97–SM'06) received his BSc (Eng.) degree in Electronic Engineering, from Gilan University, Rasht, Iran, his MSc degree in Power Engineering from KhNT University of Technology, Tehran, Iran, and his PhD degree in Power Electronics from Queensland University of Technology, Brisbane, Australia, in 1989, 1995 and 2001, respectively. Dr. Zare is an Associate Professor at QUT. His main research interests include Pulsed Power, Power Electronics Topologies and Control, Pulse Width Modulation Techniques and Renewable Energy Systems.

Gerard Ledwich (M'73–SM'92) received the Ph.D. degree in electrical engineering from the University of Newcastle, Newcastle, Australia, in 1976. He has been since 2006 Chair Professor in Power Engineering at Queensland University of Technology, Brisbane, Australia. From 1998 to 2005 he was the Chair in Electrical Asset Management at the same university. He was Head of Electrical Engineering at the University of Newcastle from 1997 to 1998. From 1976 to 1994 he was associated with the University of Queensland. His interests are in the areas of power systems, power electronics, and controls. Dr. Ledwich is a fellow of I.E.Aust.

Arindam Ghosh (S'80–M'83–SM'93–F'06) is the Professor of Power Engineering at Queensland University of Technology, Australia. He has received his Ph.D. in EE from University of Calgary, Canada in 1983. Prior to joining the QUT in 2006, he was with the Dept. of Electrical Engineering at IIT Kanpur, India, for 21 years. He is a fellow of Indian National Academy of Engineering (INAE) and IEEE. His interests are in Distributed Generation, Control of Power Systems and Power Electronic devices.

Hidenori Akiyama (M'87–SM'99–F'00) received the Ph.D. degree from Nagoya University, Nagoya, Japan, in 1979. From 1979 to 1985, he was a Research Associate at Nagoya University. In 1985, he joined the faculty at Kumamoto University, Kumamoto, Japan, where he is currently a Professor, the director of Bioelectrics Research Center and the director of global COE program on Pulsed Power Engineering. He received the IEEE Major Education Innovation Award in 2000, the IEEE Peter Haas Award in 2003 and the Germeshausen Award in 2008.