A Novel High-Voltage Pulsed-Power Supply Based on Low-Voltage Switch–Capacitor Units

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***Abstract*—This paper presents a high-voltage pulsed-power system based on low-voltage switch–capacitor units that are connected to a current source for several applications such as plasma systems. A modified positive buck–boost converter topology is used to utilize the current source concept, and a series of low-voltage switch–capacitor units is connected to the current source in order to provide a high voltage with a high voltage stress (dv/dt) as demanded by the loads. This pulsed-power converter is flexible in terms of energy control because the stored energy in the current source can be adjusted by changing the current magnitude to significantly improve the efficiency of various systems with different requirements. The output-voltage magnitude and stress (dv/dt) can be controlled by a proper selection of components and control algorithm to turn on and off the switching devices.**

***Index Terms*—Current source, high voltage stress, plasma, pulsed-power supply, switch–capacitor units.**

I. Introduction

A STEADY accumulation of energy, followed by its rapid release, can result in the delivery of a larger amount of instantaneous power over a shorter period of time (although the total energy is the same). The energy is delivered in the form of high-voltage short-duration pulses that are called as pulsed power. Voltage magnitude, pulse rising time duration, repetition, and energy are significant specifications of these pulses, which are defined based on the application requirements. Pulsed-power converters became widespread industrially, with increasing demands in applications such as ozonizing, sterilizing, recycling, exploding, winery, and medical and military applications [1], [2]. Plasma systems are currently the most substantial application of the pulsed-power technology [3]. However, there are still specific issues which hinder the wide-scale application of these systems. The main issue is power efficiency, which can affect the long-term usage of pulsed-power suppliers in industries.

Conventionally, Marx generators (MGs) [4]–[6], magnetic pulse compressors [7]–[9], pulse-forming networks [10], [11], multistage Blumlein lines [12], [13], etc., are employed to supply the pulsed-power systems. They are mostly classified under the voltage source topology category and are suffering from major drawbacks such as being inflexible in terms of controlling the output-voltage levels and stresses and the power delivery to the load. The circuit diagram of an MG is shown in Fig. 1.

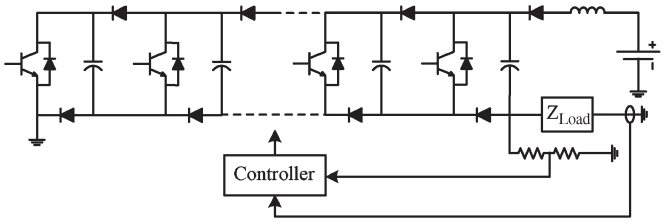

Fig. 1. MG.

Since plasma systems are naturally known as capacitive loads for the power supply equipment, current source topologies are suitable candidates, in terms of flexibility, in supplying these sorts of applications and in improving efficiency. With respect to this issue, a dc–dc converter that is based on the buck–boost converter concept is designed to feed these loads. This topology aims to generate a high voltage with a series of low–medium voltage switches. The novel idea in this proposal is employing a series of switch–capacitor units in order to provide a high dc voltage with a high voltage stress dv/dt, considering plasma load requirements. The modified version of this converter can generate high dc voltage levels in a few nanoseconds.

II. Configuration and Analyses

A. Topology

The proposed circuit diagram includes an ac–dc rectifier that is connected to a modified positive buck–boost converter, as shown in Fig. 2. The inductor that is connected to the dc source through a switch S_S acts as a current source. A controller is used to control the current through the inductor, which adjusts the energy required by a load. A flywheel diode is used to provide a current loop for the inductor when the switch S_S is turned off. A series of switch–capacitor units that are connected in cascade to the current source can generate a high-voltage pulse with a significant dv/dt.

Plasma applications are known as nonlinear resistive–capacitive loads. To simulate the plasma behavior for the pulsed-power supply, a simple resistive–capacitive model with a switch has been chosen to show the high and low resistivities

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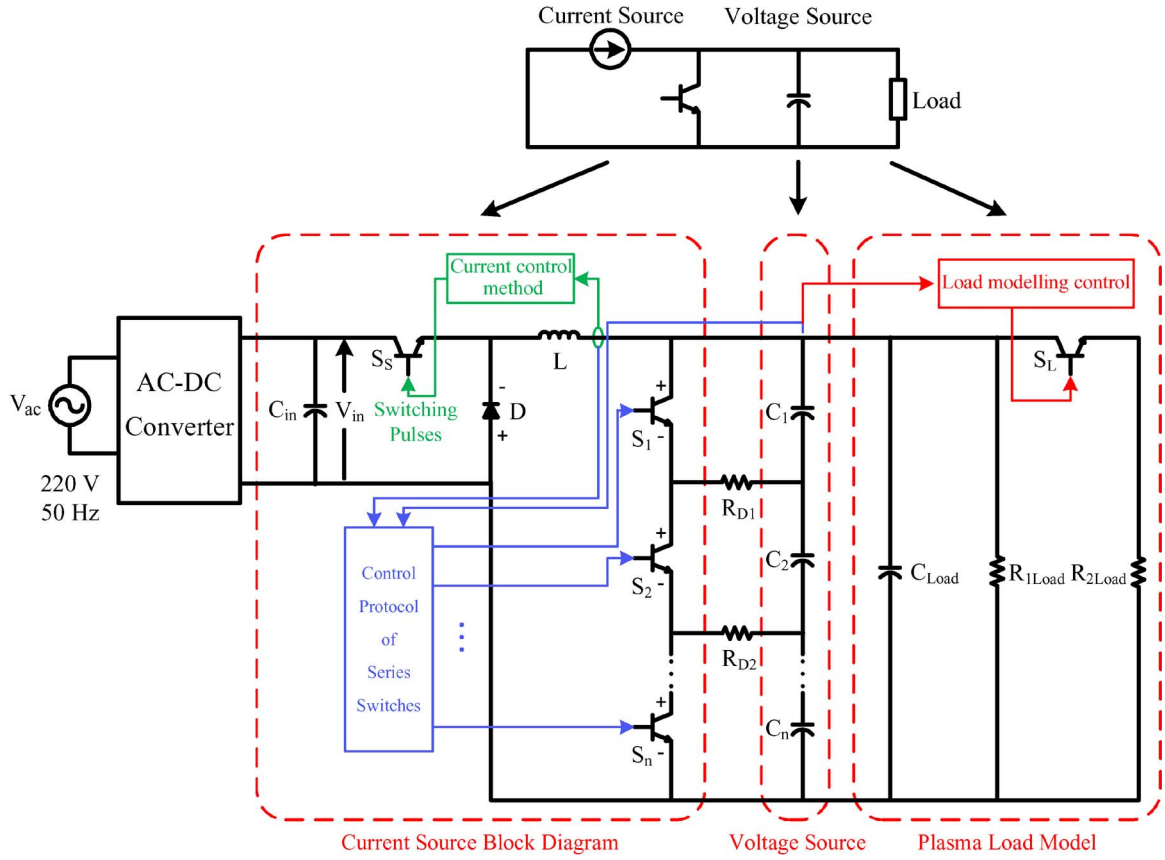

Fig. 2. Plasma power supply configuration with multi switch–capacitor units.

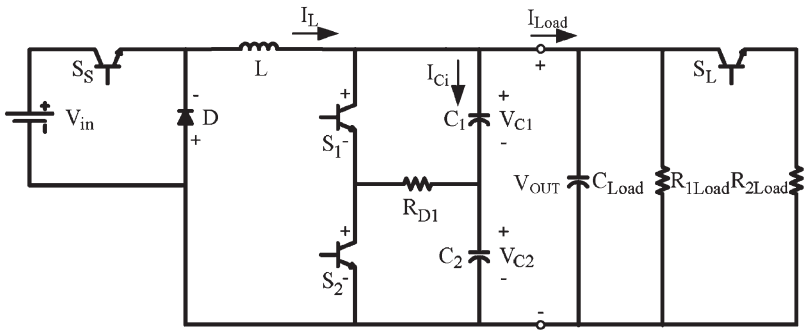

Fig. 3. Simplified two switch–capacitor unit plasma power supply and the load model.

of the load $R_{1\mathrm{Load}}$ and $R_{2\mathrm{Load}}$ in different physical situations. $R_{1\mathrm{Load}}$ in the mega-ohms range represents the load resistivity before a resumption of the plasma reaction in order to model the load's leakage current. $R_{2\mathrm{Load}}$ in the range of a few ohms represents the load resistivity in the period of the plasma reaction. This load model is shown in Fig. 2. In a real condition, the resistivity of the load substantially drops, and based on the proposed model, the load current is supplied by the voltage and current sources.

To analyze the pulsed-power supply converter, we have considered two switch–capacitor units, as shown in Fig. 3, and the analysis and simulations can be extended for n switch–capacitor units.

The general concept of this circuit is based on delivering the stored energy in the inductive and capacitive components to a load. To satisfy this condition, the inductor current should be pumped into the capacitor bank to charge the capacitors and to create a high voltage and a high dv/dt across the load.

B. Switching Modes

The operation modes of this topology are classified into the following two separate parts: the load-supplying part and the discharging of the capacitors part, which initializes the energy-storage components for the next supplying cycle. The load-supplying part, which is consist of three operation modes, is shown in Fig. 4.

1) First Mode (S_S Is On, S_1 Is On, and S_2 Is On): Fig. 4(a) shows the inductor's charging mode, while in the other three modes, the inductor is being discharged. Based on (1) and (2),

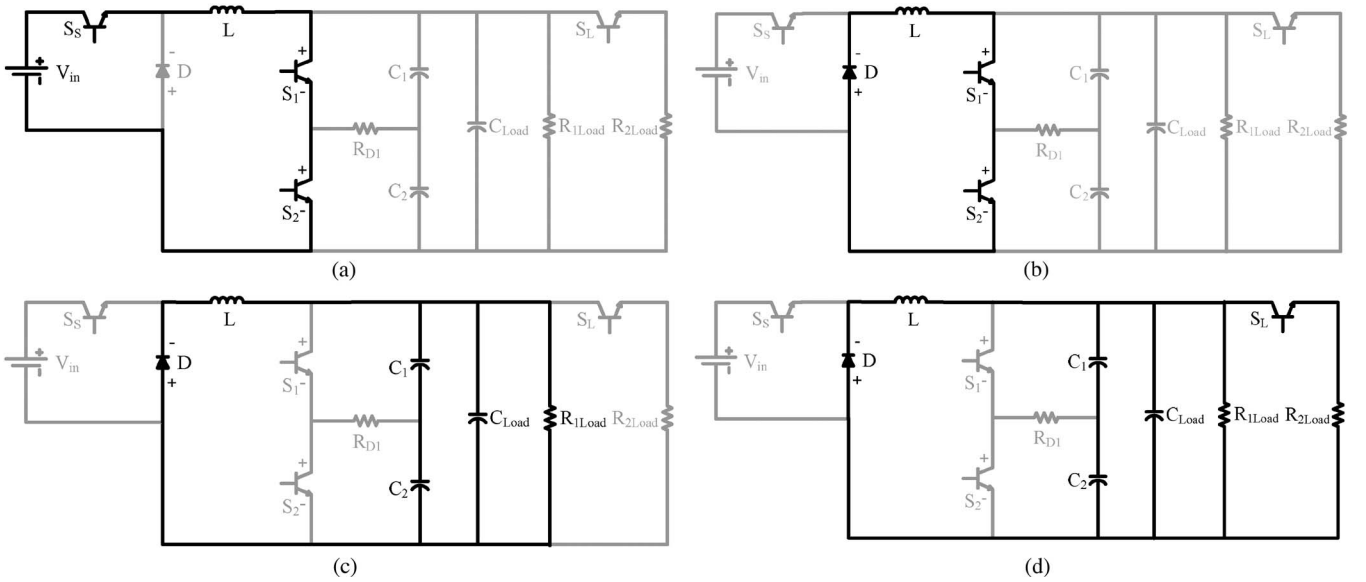

Fig. 4. Switching states of the proposed power supply circuit. (a) Current source in the charging mode. (b) Current source in the discharging mode. (c) Voltage source in the charging mode. (d) Load-supplying mode.

the input voltage is located across the inductor in this mode and charges it

$$V_L = V_{\text{in}} - (V_{\text{S}_\text{S}} + V_{\text{S}_1} + V_{\text{S}_2}) \tag{1}$$

$$V_L = L(di/dt) = L(\Delta i/\Delta t). \tag{2}$$

If the inductor is supposed to be with no initial current charge ($\Delta i = I$), then the time interval in charging the inductor to a certain level will be $\Delta t = (L \cdot I_{\max})/V_L$.

2) Second Mode (S_S *Is Off,* S_1 *Is On, and* S_2 *Is On):* In Fig. 4(b), the stored current circulates through a diode D, while S_S is turned off. In this mode, the inductor current reduces gently due to the low negative voltage across the inductor that is generated by the voltage drop across the diode and switches. The inductor current can be supposed to be constant due to the insignificance of this voltage. The charged inductor acts as a current source for the rest of the topology

$$V_L = -\left(V_D + V_{\text{S}_1} + V_{\text{S}_2}\right). \tag{3}$$

These two switching states illustrate how the current source receives energy and keeps it ready for delivery to the voltage source and the load subsequently.

There are arbitrary numbers of switch–capacitor units that are connected in series together and the whole unit that is connected in parallel with the current source of the system which charges the capacitors. The number of these units is determined by the required output voltage. Take into account that, when the inductor is being charged through S_S, all of those switches should be closed; otherwise, there may be an undesired resonant between the inductor and the capacitors. As soon as the inductor current reaches a defined current level, indicating that the inductor is fully charged, S_S is switched off, and the inductor current flows through diode D, as shown in Fig. 4(b). The voltage drop across the diode and the switches creates a small negative voltage across the inductor, which slightly discharges the inductor.

3) Third Mode (S_S *Is Off,* S_1 *Is Off, and* S_2 *Is Off):* In the next switching mode, which is called as the capacitor charging mode and is shown in Fig. 4(c) and (d), the switches (S_1 and S_2) are opened simultaneously to allow the inductor current to flow through the capacitors and to charge them. This can particularly create a high voltage across the capacitors, while the capacitors are selected in the nanofarad ranges. By assuming that the current I_C is constant, then

$$(\Delta V_{C_i}/\Delta t) = (I_{C_i}/C_i) \Rightarrow \Delta V_{C_i} = (I_{C_i}/C_i) \cdot \Delta t. \tag{4}$$

Since the capacitors are identical and since the same current flows through all capacitors, there will be a similar voltage across each capacitor. Therefore, the summation of these voltages appears at the output of the power supply

$$V_{\text{out}} = n \cdot V_{C_i} \tag{5}$$

$$\Delta V_{\text{out}} = n \cdot \Delta V_{C_i}. \tag{6}$$

n is the number of switch–capacitor units which can be extended to satisfy the load demands. Having more units reduces the equivalent capacitance of the capacitor bank in the output of the topology, and with a fixed injected current, there will be higher voltage level and stress in the output of the power supply

$$C_{\text{eq}} = C_i/n. \tag{7}$$

Based on the switching characteristics of the power switches in terms of the internal resistivity of the conducting and nonconducting modes, both sides of each capacitor are connected to the sides of each switch in order to provide voltage sharing over the switches.

Plasma reaction is resumed with respect to the stimulation of a high voltage over a related material. However, the key point is that this high voltage should be induced with an extremely high voltage stress dv/dt. Pumping the stored current into the series of capacitors which have considerably low capacitances can generate significant high voltage magnitude and stress to fulfill the plasma creation requirements.

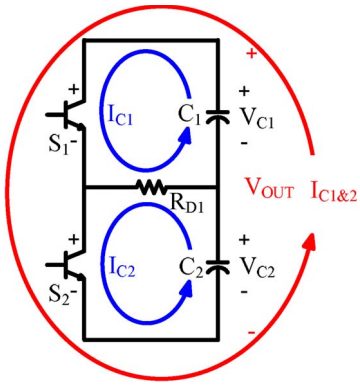

Fig. 5. Possible current loops during the short-circuit periods.

C. Discharging the Residual Energy

It should be noted that, based on this switching algorithm, all capacitors should get fully discharged to avoid a probable short circuit through the switches in the switch–capacitor units. In this control algorithm, the series switches should be turned off when a pulse voltage is to be generated, and they should be turned on when the capacitors are fully discharged. However, there is still a major concern. Even when the capacitors are almost discharged, the flowing current to the load creates a voltage over the capacitors, which may cause a short circuit when the unit switches are reclosed. There are several ways to either prevent or damp this phenomenon, such as putting either reverse blocking components or extra inductive or other damping elements in the short-circuit loop.

Since there is a possibility that the whole capacitor's energy will not be delivered to the load and that the unit switches will be closed for current recovery, there should be an appropriate number of damper components, like resistors or inductors, in the switch–capacitor units to prevent the probable inrush current, which is caused by the short circuit of the charged capacitors when the unit switches are closed.

Any inductive elements in the switch–capacitor loop exchange energy with the capacitor and lead to oscillations which cannot be prohibited by the diodes. Therefore, they are not suitable options for such a purpose in this topology.

Resistor is another alternative, which can be installed in common paths of units and which can damp the remaining energy of the inductor and capacitors. As shown in Fig. 5, although R_{D1} can prevent short circuits of two units, there is still another loop (which is consist of C_1, C_2, S_1, and S_2) that can be a short circuit. Putting a resistor in this path causes loss in charging the capacitors and in supplying the load periods. There are a couple of ways (hard and soft methods) to discharge the capacitors just by using the common path resistors.

1) Hard Methods: In the hard method, a parallel switch–resistor unit will be located in the return path, as shown in Fig. 6(a). This switch will be on unless the period of discharging the remaining energy which will be off. Therefore, the resistor will be in the flowing path in this period and will keep the topology away from short circuit.

Thermistors can also be employed in this regard. A thermistor is a type of resistor whose resistance varies with temperature. They can be installed in series with the switches, and

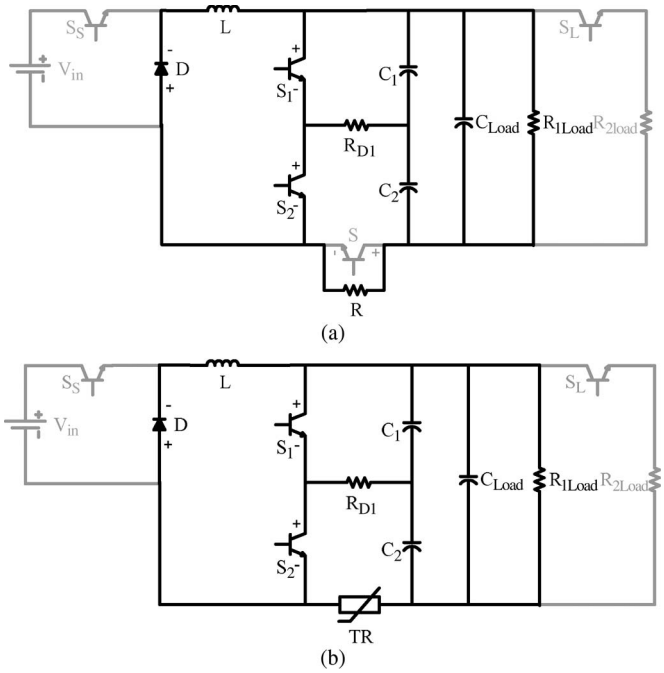

Fig. 6. Two examples of the hard methods for discharging the residual energy in the inductor and capacitors. (a) Parallel switch–resistor unit located in the return path. (b) Thermistor in the return path.

they will protect the circuit in the stint of the inrush current. As shown in Fig. 6(b), the resistivity of the circuit will be increased in the discharging mode.

These two solutions impose an initial cost to the whole topology, but the benefit they can bring for this power supply is the possibility to stop supplying load in any stage. Therefore, the remaining energy in the inductor after each supplying mode can be saved in each supplying cycle.

2) Soft Method, the Fourth and Fifth Switching Modes [(S_S Is Off, S_1 Is On, and S_2 Is Off) and (S_S Is Off, S_1 Is Off, and S_2 Is On)]: This should be considered to keep the power loss at the minimum possible level. In the soft method, which is used in this investigation, no extra element is installed in the return path. Instead, the remaining energy is discharged with the extra switching states. As can be inferred from the hard methods, the supplying path should be free from any energy-consuming elements during the load-supplying period; otherwise, the loss rate will substantially increase. Therefore, $n-1$ is the number of resistors used in this topology. The point is that, since there is no resistor in the supplying path, switches S_1 and S_2 cannot be turned on simultaneously; otherwise, short circuit is unavoidable. The unit's switches are turned on and off in such a manner that the remaining voltage across the output capacitors and plasma reactor will be discharged. Following this concept, a couple of switching states will be added to the former states after plasma creation and will be alternatively repeated to fully discharge the remaining voltage and current. The discharging the remaining energy part which is already addressed in the Switching Modes section, is composed of these states that are shown in Fig. 7.

Based on the designed control algorithm, the inductor and C_1 are fully discharged during the first state, while S_1 is on, and S_2 is off. In this switching mode, the inductor energy is

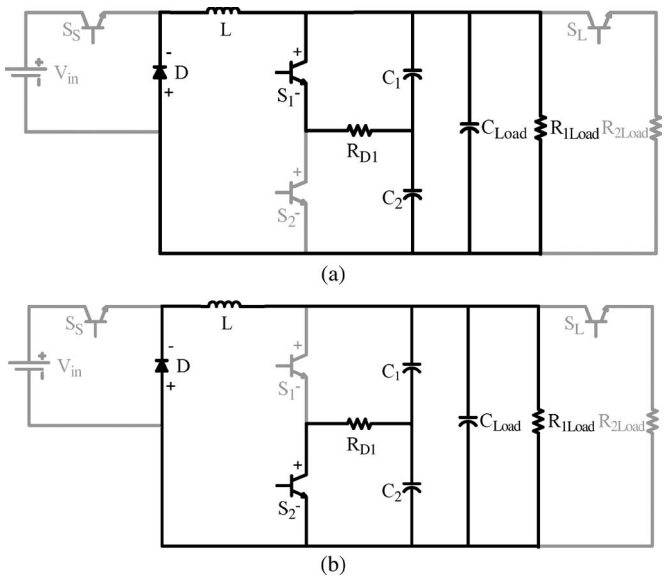

Fig. 7. Circuit's switching states in association with the soft method in order to discharge the remaining energy in the capacitors.

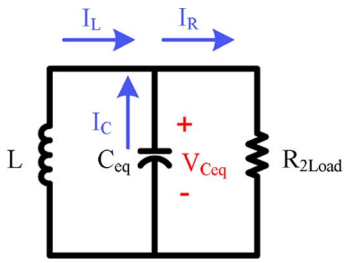

Fig. 8. Equivalent RLC circuit of the power delivery mode of the power supply.

delivered to C_2 and charges it. In the next state, while S_1 and S_2 are turned off and on, respectively, C_2 is discharged through R_{D1}. However, there is still a considerable voltage across the reactor capacitor C_{Load} which is going to be discharged through R_{D1} during this mode. Although C_1 is almost ten times the value of C_{Load}, this voltage can charge C_1 to a potentially hazardous level, and it needs to be discharged again. Therefore, the switching states change between these two modes until the capacitor voltage becomes less than a safe value.

In case of no prosperous plasma generation, a general step should be considered to discharge the capacitors before starting a new pulse process. In these circumstances, the output voltage will automatically increase and may cause a real trouble. Even if the capacitors can tolerate this high voltage, they need to be discharged, and they must be ready for the next cycle. The mentioned solution can be applied for such a problem as well. By taking into account this concern, the discharging resistors R_D should be considered as much as possible to handle such a high voltage and to prohibit a high current flow in the discharging period.

D. Analyses of the Load-Supplying Mode

In this mode, the equivalent circuit of the system would be the parallel RLC circuit shown in Fig. 8. To realize how the stored energy in the power-storage elements of the circuit will be delivered to the load, the instantaneous inductor current $I_L(t)$ and capacitor voltage $V_C(t)$ in this mode are the most prominent indicators of power delivery, which can be achieved as follows.

The inductor current of this mode in the Laplace S-domain is

$$I_L(s) = \frac{(LCI_L(0))\,S + \left(CV_C(0) - \frac{L}{R}I_L(0)\right)}{(LC)S^2 - \left(\frac{L}{R}\right)S + 1}. \tag{8}$$

Moreover, based on the considered range for the inductor, capacitor, and plasma resistance, it can be assumed that, in any condition

$$L/C > 4R. \tag{9}$$

Therefore, the time response of the inductor current $I_L(t)$ can be achieved as

$$I_L(t) = [1/(\alpha_2 - \alpha_1)] \cdot \left[(k_2 - k_1\alpha_1)e^{-\alpha_1 t} - (k_2 - k_1\alpha_2)e^{-\alpha_2 t}\right] \tag{10}$$

while

$$k_1 = LCI_L(0) \tag{11}$$

$$k_2 = CV_C(0) - (L/R)I_L(0) \tag{12}$$

$$\alpha_{1,2} = \left[-\left(\frac{L}{R}\right) \pm \sqrt{\left(\frac{L}{R}\right)^2 - 4(LC)}\right] \Big/ 2(LC). \tag{13}$$

Since

$$V_C(t) = -L \cdot [dI_L(t)/dt] \tag{14}$$

$$V_C(t) = \frac{1}{(\alpha_2 - \alpha_1)}\left[\alpha_1(k_2 - k_1\alpha_1)e^{(-\alpha_1 - 1)t} - \alpha_2(k_2 - k_1\alpha_2)e^{(-\alpha_2 - 1)t}\right]. \tag{15}$$

Since the capacitors are opted to be smaller in comparison with the inductor, they cannot store that much energy, and they will be discharged considerably faster than the inductor. Besides (10) and (15), the simulation results shown in Fig. 12(a) and (d) can also demonstrate the evidences to verify this statement. In this mode, there will be a high current for a short period of time, which discharges the capacitors. After that, if there are any demands for more current, the inductor would supply energy to the load until it will be fully discharged; otherwise, the supplying process would be stopped by closing the series units' switches alternatively, and the power supply can be prepared for the next power delivery cycle. The simulation results shown in Fig. 12 confirm this expression.

Several simulations and analyses under different load conditions have been carried out to verify the validity of the proposed topology and control strategy. As the simulation results will be demonstrated in the next parts, this power supply has the capability of generating pulsed power in an extensive range of amplitude and dv/dt.

III. Control Strategy

The power switches utilized in this configuration have three distinguished functions. With respect to these functions, appropriate control algorithms are designed to turn on and off the switches properly and to satisfy the desired duties thoroughly.

A. Current Control

To control the inductor current, the current-control block determines the duty cycle for switch S_S, located between the dc source and the inductor, in order to charge the inductor at a specific current level. In this strategy, the desired amount of the inductor current is selected as a limit to turn off S_S. The switching state in Fig. 4(a) shows the inductor charging mode. Based on the series switch condition, the energy can be either stored in the inductor or delivered to the load. On the other hand, while the inductor delivered energy to the load and became discharged, the control block switches on S_S in order to charge the inductor. There are also a couple of conditions that should be met before turning S_S on. The capacitor voltage should be under a specific level to turn on S_S. The control strategy in this block can be found as follows.

If $I_{\text{inductor}} \geq I_{\text{upper}}$, then $S_S = 0$.

If $I_{\text{inductor}} \leq I_{\text{upper}}$ and $V_{C1}, V_{C2}, V_{C\text{Load}} \leq V_{\min 2}$, then $S_S = 1$.

I_{inductor}, I_{upper}, and I_{lower} are the inductor actual current and the desired inductor's charging and discharging amounts, respectively. V_{C1}, V_{C2}, and $V_{C\text{Load}}$ are the capacitors voltage, and $V_{\min 2}$ is the safe level of the voltage for short circuit. The block can be implemented by a logic device or a simple program in a microcontroller.

B. Voltage Control

Series switches S_1 and S_2 are also controlled with respect to the inductor current, capacitor voltages, and the load condition. The switches can be turned off, while the inductor is fully charged, and S_S has already been turned off. The supplying repetition rate is another parameter that can define the switching moments. During the OFF state, the current flows through the capacitors and charges them. Then, at a specific voltage level, plasma occurs and discharges the inductor and capacitors but not thoroughly. The remaining energy should be discharged before turning on the unit's switches in order to refrain from short circuit and inrush current. On the other hand, if plasma does not take place to start another cycle, we need to discharge the capacitors. Based on the alternative switching of S_1 and S_2 but with different logics, two specific control programs are assigned for each of these cases. The logics are shown in Fig. 9. S_1 and S_2 are turned on and off alternatively to discharge the inductive and capacitive elements. For example, the remaining energy after each supplying cycle is discharged according to the following process.

In the switching mode shown in Fig. 7(a), while S_1 is on and S_2 is off, C_1 and L are discharged with different time constants. In the next switching state, S_1 is turned off, and S_2 is turned on simultaneously in order to discharge C_2 and C_{Load}. This procedure continues, and the circuit changes between these two modes for a few times to ensure that the output voltage is under

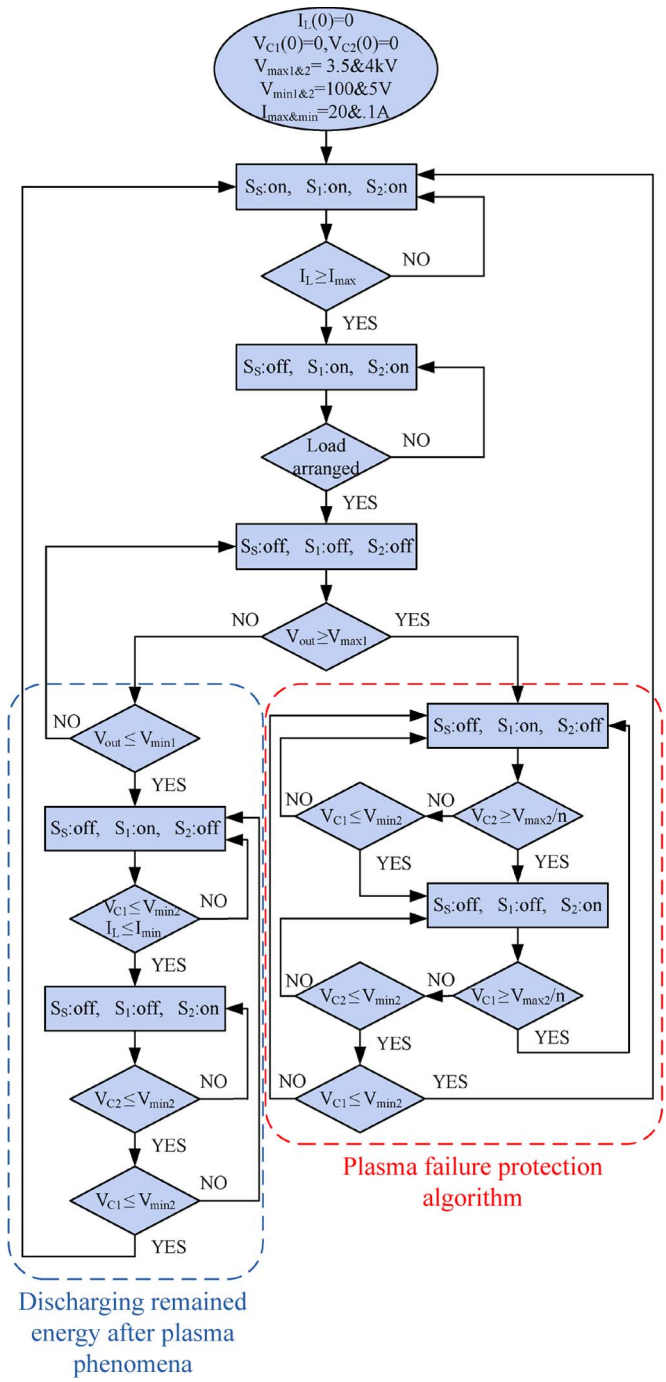

Fig. 9. Block diagram of the control algorithm.

a specific voltage level. The switches turn on together, while the inductor and capacitors are fully discharged. The flowchart shown in Fig. 9 demonstrates the control algorithm designed for this topology.

As shown in the control flowchart in Fig. 9, some voltage and current levels are defined as conditions for switching time determination in order to control the circuit performance with a maximum level of safety. In this regard, $V_{\max 1\&2}$ and $V_{\min 1\&2}$ are selected for the first and second upper and lower safety levels of the voltages, respectively. Fig. 10 shows an overview of these values in a general configuration. $V_{\max 1}$ indicates a margin above the voltage level in which the plasma phenomenon

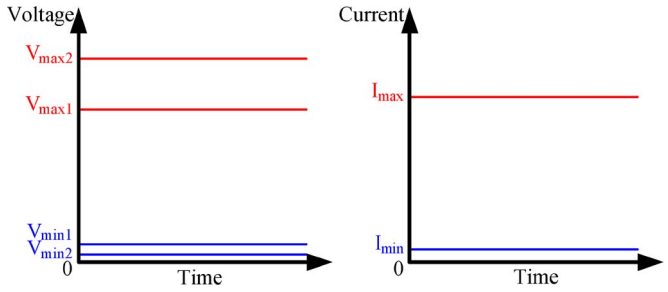

Fig. 10. Definition of the voltage and current levels for the control strategy.

occurs. $V_{\max 2}$ presents a summation of voltages that can be tolerated by all of the switches. This amount is assigned based on the switch characteristics, and the rise in voltage above that level can be critical for the switches. Based on the number of switch–capacitor units in the topology (n), each power switch should handle $V_{\max 2}/n$ volts. $V_{\min 1}$ is chosen with respect to the level of voltage in which the load-supplying process can be stopped, and $V_{\min 2}$ is a safe level of voltage for the capacitors in case of short circuit. $I_{\max}$ gives the inductor charging amount, and $I_{\min}$ is a safe level of current which cannot charge the capacitors more than the $V_{\min 2}$ level. As shown in the start block of this flowchart, the $V_{\max 1\&2}$, $V_{\min 1\&2}$, and $I_{\max \& \min}$ values are designated as 3500, 4000, 100, and 5 V, and 20 and 0.1 A, respectively, for a two-unit topology.

C. Load Control

In order to model the supplying mode, S_L is switched on as soon as the capacitor is charged up to a required voltage level. This voltage is defined by the load, and it may change for different applications. The load resistivity dramatically drops to a few ohms by turning S_L on. This low resistivity discharges the capacitors and inductor with high and low time constants. Turning S_L off prepares the system for the next cycle of load supplying. The control strategy that is adopted to generate the gate signals for this switch is almost similar to the current control, despite of measuring and comparing the output voltage instead of the inductor current. The switching signal pattern of the circuit is shown in Fig. 11.

IV. Simulation Results

According to (4), it can be deduced that a higher current can generate a higher dv/dt across the capacitors. Fig. 12 shows the results extracted from the simulation of the circuit operating in the mode shown in Fig. 4(c). In this figure, the voltage and current stresses of the circuit with two different inductors (L_1 and L_2) and current levels (I_{L1} and I_{L2}) are shown. To have the same stored energy in both inductors, for $L_2 = k \cdot L_1$, the inductor current should be adjusted as

$$I_{L2} = (1/\sqrt{k}) \cdot I_{L1} \tag{16}$$

since

$$(1/2)L_1 \cdot I_{L1}^2 = (1/2)L_2 \cdot I_{L2}^2. \tag{17}$$

In this example, L_1 and L_2 are 1 and 9 mH, respectively, and consequently, $I_{L2} = 3\ I_{L1}$ in order to have the same energy

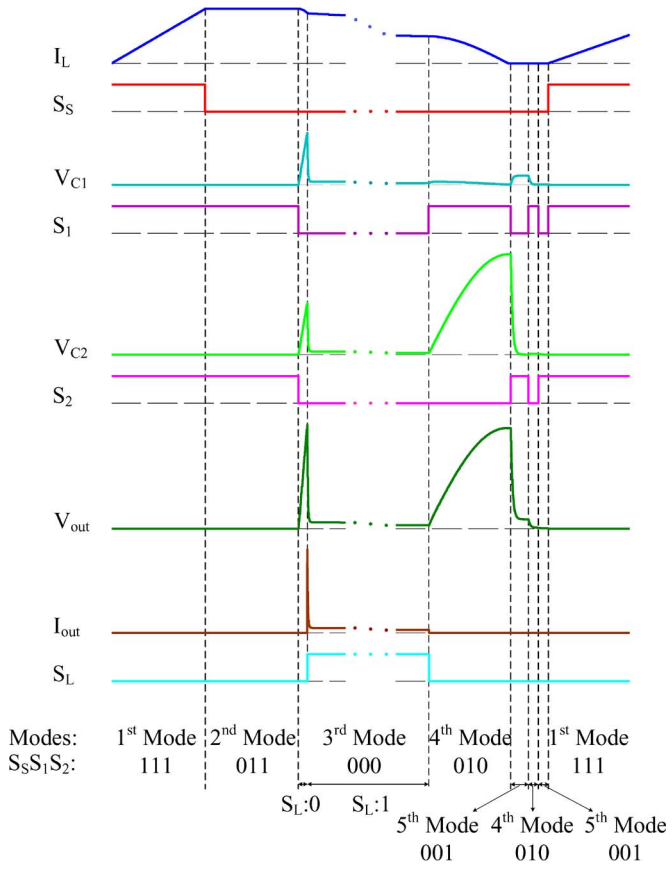

Fig. 11. Switching signal pattern.

stored in the inductors L_1 and L_2. As shown in Fig. 12(a) and (c), the inductor currents are controlled at 45 and 15 A for I_{L1} and I_{L2}, respectively. Ultimately, the voltage level of the capacitor is based on the stored energy in the inductor

$$V_{\text{out}} = \sqrt{(L/C_{\text{eq}})} \cdot I_L. \tag{18}$$

There are the same stored energies in the inductors for both cases. Therefore, the final values of the voltages are similar, and they reach the level of 18 kV. However, dv/dts vary with respect to the inductor current levels. In the first case, the inductor current is set to 45 A, which creates a 4.5-V/ns voltage stress across the capacitors, while in the second case, the inductor current (15 A) causes the output voltage to rise with a 1.5-V/ns slope.

To show how this power supply circuit works and to verify the validity and accuracy of the foreseen circuit analyses which came earlier, a 10-Ω load is assumed as the resistivity of the load in the plasma reaction period, and the results are shown in Fig. 13.

As shown in Fig. 13(d), the plasma resumes at a 3-kV voltage, while each capacitor provides half of the voltage level shown in Fig. 13(b) and (c). At the plasma reaction period, first, the load discharges the capacitors, and then, the inductor energy can be either delivered to the load with a bigger time constant or discharged in the assigned resistors. The load voltage created by the inductor current, which is the remaining voltage across the capacitors after discharging, is balanced identically. These results remove all concerns with regard to the capacitor's

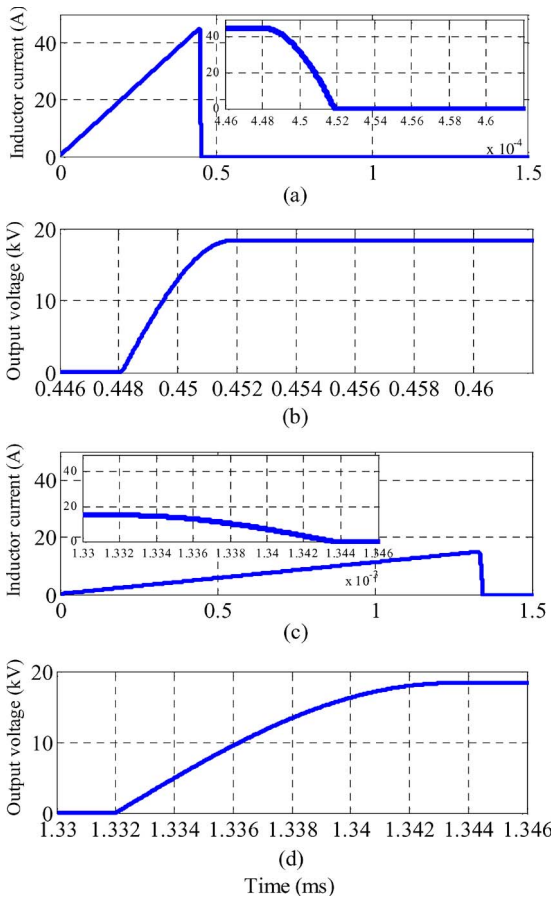

Fig. 12. dv/dts generated by different inductors with similar inductive energy. (a) Current of a 1-mH inductor. (b) Output voltage of a 1-mH inductor. (c) Current of a 9-mH inductor. (d) Output voltage of a 9-mH inductor.

voltage sharing issues. The remaining current and voltage in the inductor and capacitors are discharged through the previously described discharging modes. While L and C_1 are being discharged, the current passes through C_2 and recharges it to almost 3 kV. In the next mode, C_2 is being discharged, while the voltage across C_{Load} is recharging C_1 again. Hence, these switching states continue alternatively in order to fully discharge the remaining energy.

The results shown in Fig. 14 demonstrate the case of lacking plasma reaction and energy delivery. A brief review over these results can be beneficial for the analyses of power supply operation in this particular case. As anticipated, the inductor energy is delivered to the capacitor bank and charges it, and if this energy is not depleted, the system will face a major trouble.

There is no plasma at 3-kV voltage; thus, the capacitors should be discharged when the output voltage reaches a higher voltage level (e.g., 4 kV). The power supply switches to the fifth mode, but the point is that the inductor current is in a considerable level and may charge C_2 to a high level of voltage, which is out of the tolerable range for the switches. Therefore, it is not possible to entirely discharge the inductor current in a single discharging state. Hence, the switching mode changes, while each capacitor voltage crosses a specific value (e.g., 3 kV) until the inductor current is fully discharged. Then, the exchange manner follows to ensure discharging of the capacitors. Now, the system is prepared for the next supplying cycle.

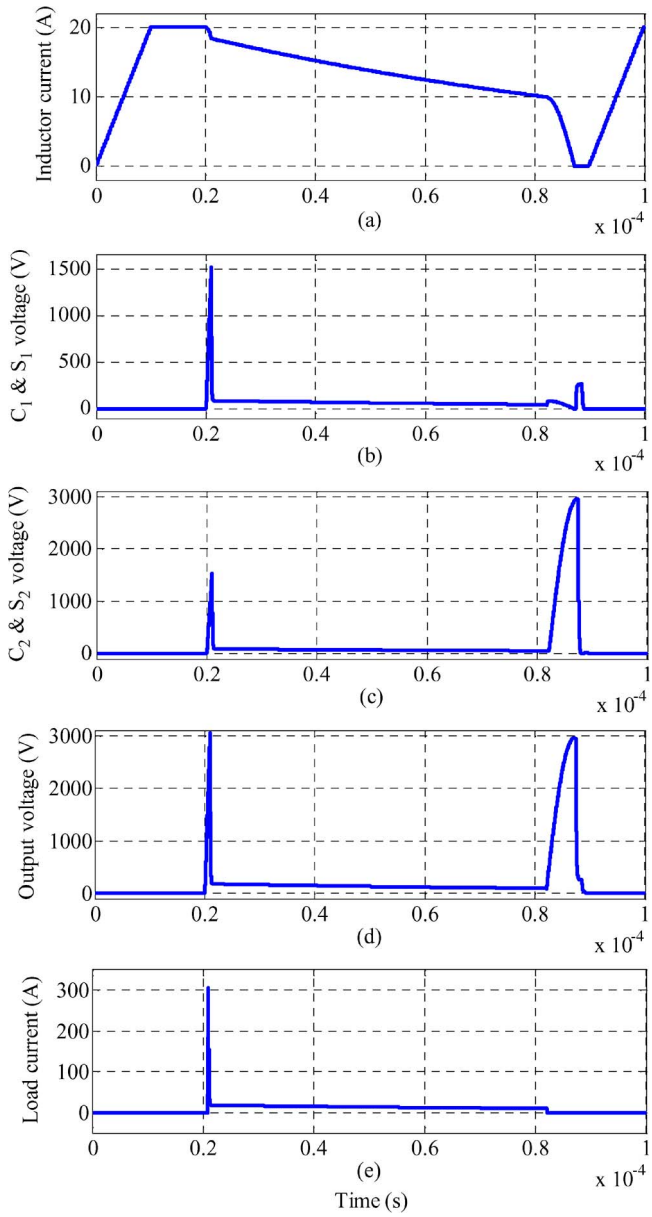

Fig. 13. Output voltages and currents of the power supply. (a) Inductor current (in amperes). (b) C_1 and S_1 voltages (in volts). (c) C_2 and S_2 voltages (in volts). (d) Output voltage (in volts). (e) Load current (in amperes).

V. Component Determination and Energy Discussion

Efficiency is the main concern when designing a power supply for plasma applications. In this topology, having the least energy losses is considered in addition to the flexibility of the equipment, which needs to be adjusted for a diversity of pulsed-power applications. The inductive and capacitive components (L and C_i) should be selected appropriately in order to both satisfy the load requirements and avoid energy wasting. As the output-voltage level and stress and the delivered energy are defined by the load, the element sizes can be determined with regard to those parameters.

The output equivalent capacitor $C_{\text{eq}} = C_1 \| C_2 \| \cdots \| C_n$ should be at least ten times the load capacitance to prevent any loading problems. On the other hand, the equivalent capacitance

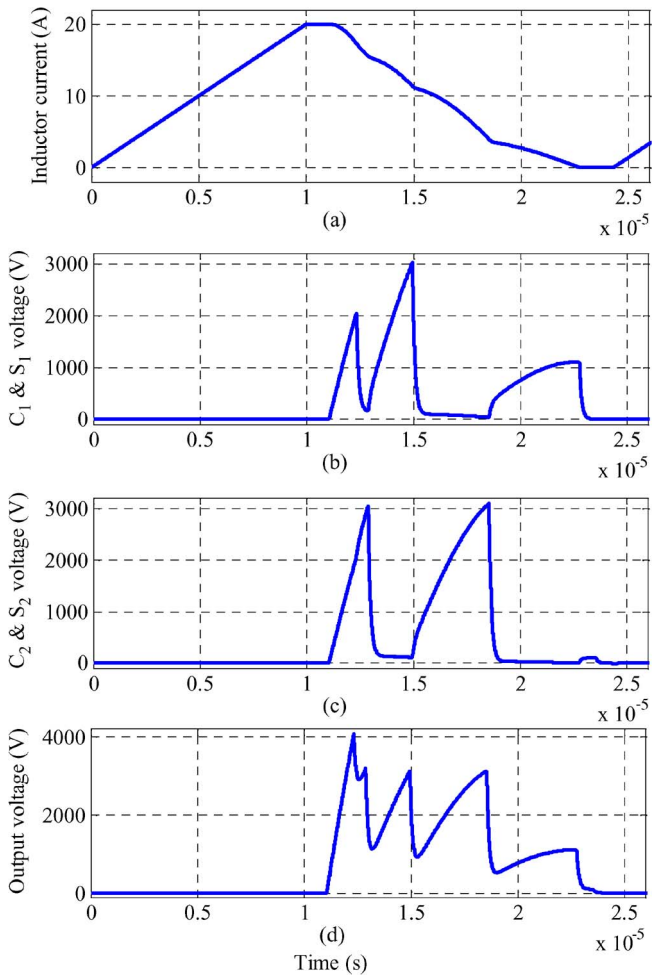

Fig. 14. Inductor current and output voltages of the power supply in the case of no prosperous plasma phenomena. (a) Inductor current (in amperes). (b) C_1 and S_1 voltages (in volts). (c) C_2 and S_2 voltages (in volts). (d) Output voltage (in volts).

needs to be as small as possible to generate the voltage stress and level demanded by the load. Thus

$$C_{\rm eq} = 10C_{\rm Load}. \tag{19}$$

If the capacitors C_i are supposed to be identical, then $C_{\rm eq} = (C_i/n)$

$$C_i = 10n \cdot C_{\rm Load}. \tag{20}$$

n is the number of switch–capacitor units which is determined by the switch voltage and the demanded output voltage.

By assuming that the inductor current is constant during the capacitor charging mode, the voltage stress can be calculated as follows:

$$I_L = (C_{\rm eq} + C_{\rm Load}) \cdot (dV_{\rm out}/dt). \tag{21}$$

In the last stage, the demanded energy stored in the inductor defines the inductance value

$$(1/2)L \cdot I_L^2 = E_{\rm Load}. \tag{22}$$

Finally, the recovery time for the inductive and capacitive components and the frequency of the pulsed power generated

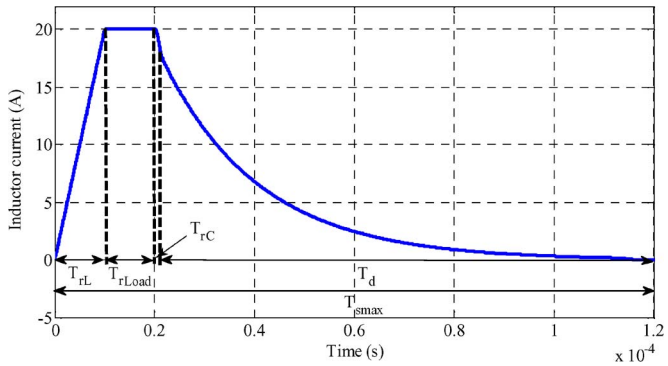

Fig. 15. Time monitoring in a load-supplying cycle.

TABLE I
SPECIFICATIONS OF THE MODELED CIRCUIT

V_{in}	L	R_D	C_i	R_{1Load}	R_{2Load}	C_{Load}	f_s
200V	0.6mH	10 Ω	10nF	10MΩ	10 Ω	1nF	2kHz

by the power supply can be determined as follows:

$$T_{r\_L} = (L \cdot I_L)/V_{\rm in} \tag{23}$$

$$T_{r\_C} = \left[(C_{\rm eq} + C_{\rm Load}) \cdot V_{\rm out}\right]/I_L \tag{24}$$

$$T_{r\_LC} = \left[L \cdot I_L^2 + (C_{\rm eq} + C_{\rm Load}) \cdot V_{\rm out} \cdot V_{\rm in}\right]/(V_{\rm in} \cdot I_L). \tag{25}$$

In repetitive pulse generation, a time interval is designated to the load to be prepared for the next supplying cycle. For instance, in plasma generation, the produced plasma needs to be exhausted, and the reactor should be filled with fresh material. This interval is defined by $T_{r\_\rm Load}$ in these equations. The frequency of the load supply with pulsed power significantly relies on the load features and requirements ($T_{r\_\rm Load}$), but it cannot be more than the recovery frequency of the power supply

$$f_{s\_\max} < \left[1/(T_{r\_LC} + T_{r\_\rm Load} + T_d)\right]. \tag{26}$$

The load's capacitive and resistive characteristics in the interval of the plasma phenomena define the discharging time of the inductor (T_d). The inductor current in a load-supplying cycle is shown in Fig. 15 with detailed time intervals.

Regarding the aforementioned determinations, a model has been designed in the MATLAB/SIMULINK platform to analyze the performance of the proposed circuit. The detailed specifications of the circuit are given in Table I.

These results indicate how the topology decreases the energy losses and improves power efficiency. For example, presume that the current source and the unit switches S_S and $S_1, \ldots, S_n$ get closed when the inductor still delivers 1 A to the load. This means that 10 V still exists across the 10-Ω load, which is named as $V_{\rm out-off}$. Closing the switches results in discharging the inductor and output capacitors through unit loops and in losing energy. This energy loss for a delivery cycle can be estimated as

$$E_{\rm Loss} = (1/2) \cdot \left(L \cdot I_{L-\rm off}^2 + C_{\rm eq} \cdot V_{\rm out-off}^2\right) = 0.5(0.6 \times 10^{-3} \times 1^2 + 6 \times 10^{-9} \times 10^2) = 3.003mj.$$

The total stored energy in the inductor is

$$E_{\rm Total} = (1/2) \cdot \left(L \cdot I_L^2\right) = 0.5 \times 0.6 \times 10^{-3} \times 20^2 = 120mj.$$

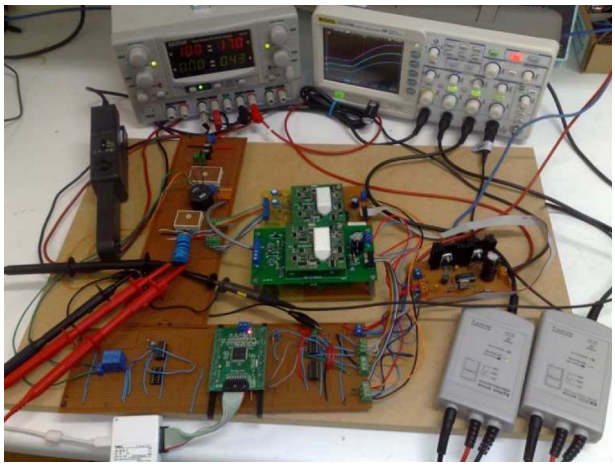

Fig. 16. Laboratory prototype of the pulsed-power supply with double switch–capacitor units.

Regarding the calculation and analyses, in this strategy, for example, if the intrinsic conduction and switching losses of the circuit are neglected, the energy losses will be almost less than 2.5% of the total stored energy in the inductor. This loss is negligible in comparison with the delivered energy to the load, so the efficiency could be considered to be more than 97.5% in the power delivery process.

VI. Experimental Results

To verify the validity of the proposed topology and the control strategy in satisfying energy exchange among the inductive and capacitive components, a laboratory prototype of a double switch–capacitor unit converter has been developed. The instantaneous value of the inductor current is used to control the level of the stored energy in the inductor. The control signals are fed into the gates of the main switching devices (S_S, S_1, S_2) through the gate driver circuits, which provide the necessary isolation between the switching signal ground and the power ground. The laboratory prototype, including the control and the power modules, is shown in Fig. 16.

In the power board, an SK50 Gar 065 (SEMIKRON) switch, which is a compact design of an insulated gate bipolar transistor (IGBT) and a diode module that is suitable for the buck converter, and an SK25 GB 065 (SEMIKRON), including a series connection of two IGBTs, are used as the main switching devices for S_S, D, S_1, and S_2. The controllers for this setup have been developed by utilizing an NEC 32-bit 64-MHz V850/IG3 microcontroller. Skyper 32-pro (SEMIKRON) is used as the gate drive circuit, which can drive two switches independently and which is compatible with the utilized IGBT modules.

This prototype has been designed to conduct a test at a low-voltage range. Due to power supply and measurement equipment restrictions, and protection concerns, the low-voltage test is initially performed in order to investigate and verify the general concept of this topology and its control algorithm. The inductor current range was adjusted around 2.5 A, and consequently, the output voltage was under 300 V. The captured

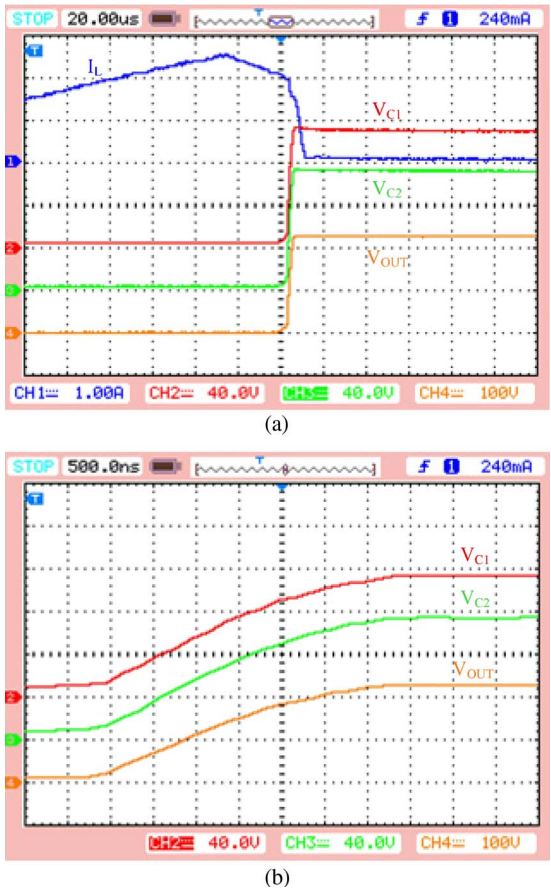

Fig. 17. Inductor current, capacitors, and output voltages.

results are shown in Fig. 17(a) and (b). The inductor current, capacitors, and output voltages are shown in Fig. 17(a) in a wider time range, while a focused shot of these voltages in Fig. 17(b) shows the voltage rise in the capacitors. Both capacitor voltages (V_{C1} and V_{C2}), separately shown with different colors, attain 110 V, while the output voltage of the converter, which is the summation of those two voltages and is depicted under them, reaches 220 V.

The high rising time of the voltages and the low ultimate voltage magnitudes are due to the adjustment of the inductor current in the low ranges.

VII. Conclusion

This paper has proposed a new topology based on switch–capacitor units that are connected in series to generate high voltage level and stress for pulsed-power applications. The general concept of this pulsed-power supply is based on a current source topology that is connected to a series of low–medium voltage switch–capacitor units, which considerably improves the efficiency of plasma systems. Simulations have been carried out to validate the proposed topology and control. The simulation results show that there is no restriction in the generation of higher voltage levels and stresses by increasing the number of the switch–capacitor units. A laboratory prototype is also implemented, and the test results verified the

whole concept of the topology in low voltage. Utilizing pretty small capacitors and having no diode in the configuration of this power supply are some advantages of this topology in comparison with former technologies, such as MGs, which are utilized as pulsed-power supply. In addition, the output-voltage level is flexible, and it can be adjusted in a high range through the control switching signals, which is not possible in the Marx technology. Although the output voltage in the Marx modulator can be adjusted by changing either the number of stages or the input voltage, the proposed topology has the potential to vary the output voltage in a wider range by controlling the inductor current, which is accomplished through the duty cycle of S_S. Changing a software parameter is clearly easier in comparison with varying the Marx stages or the input voltage (with power supply restrictions). Having no control over the power flow to the load is the main shortage of this circuit, which can be neglected, while there is a possibility to define the amount of stored energy with respect to the load demands.

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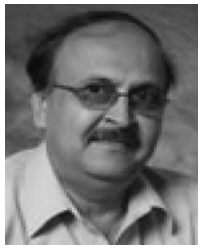

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