Static Shunt and Series Compensations of an SMIB System Using Flying Capacitor Multilevel Inverter

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***Abstract*—The flying capacitor multilevel inverter (FCMLI) is a multiple voltage level inverter topology intended for high-power and high-voltage operations at low distortion. It uses capacitors, called flying capacitors, to clamp the voltage across the power semiconductor devices. A method for controlling the FCMLI is proposed which ensures that the flying capacitor voltages remain nearly constant using the preferential charging and discharging of these capacitors. A static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) based on five-level flying capacitor inverters are proposed. Control schemes for both the FACTS controllers are developed and verified in terms of voltage control, power flow control, and power oscillation damping when installed in a single-machine infinite bus (SMIB) system. Simulation studies are performed using PSCAD/EMTDC to validate the efficacy of the control scheme and the FCMLI-based flexible alternating current transmission system (FACTS) controllers.**

***Index Terms*—FCMLI, multilevel inverter, power oscillation damping, SMIB, SSSC, STATCOM.**

I. Introduction

THE multilevel inverters have gained considerable interests over the past decade in industries as well as in academia over the multistep inverters and the conventional two-level inverters for high voltage and power applications [1]–[7]. In the multilevel inverters, all the devices are individually controlled and hence can provide better control over voltage magnitude and harmonic suppression. Further, switching each device from a voltage that is a fraction of the total dc-link voltage avoids the problem of designing the costly and bulky snubber circuits. The term multilevel starts with the three-level inverter. With the increase in levels the synthesized output waveform approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems. Unfortunately, the number of achievable voltage levels is limited due to voltage unbalance problems, voltage clamping requirements, circuit layout, cost and packaging constraints [3].

At present, there are three benchmark multilevel inverter topologies: i) diode-clamped multilevel inverter (DCMLI), ii) cascade H-bridge inverter, and iii) flying capacitor multilevel inverter (FCMLI). DCMLI suffers from the limitations of dc-link voltage unbalance, indirect clamping of the inner devices and multiple blocking voltages of the clamping diodes [3]–[5]. H-bridge cascade inverter has limitations such as, the requirement of large number of inverters to decrease the harmonics and complex dc-voltage regulation loop. It needs separate dc sources for real power conversion and thus has somewhat limited applications. Connecting separate dc sources between two converters in a back-to-back arrangement (e.g., in UPFC) is not possible because a short-circuit will be introduced when two back-to-back converters are not switching synchronously [4]. In this inverter, the switching modulation needs to be optimized for high-performance applications due to a limited combination of switching patterns. Moreover, for reactive power exchange, the power pulsation at twice the output frequency occurring with the dc-link of each H-bridge inverter necessitates over-sizing of the link capacitors [2]–[5].

The FCMLI attempts to address some of the limitations imposed by the above-mentioned inverters. With the increase in the number of output voltage levels, the number of dc-link capacitors in cascade and in DCMLI increase and hence their control become more complex especially in transient conditions. However, the dc-capacitor control loop in FCMLI is as simple as in the conventional two-level inverter and is independent of the number of output voltage levels. The typical structure of FCMLI makes it possible to split the voltage constraints and to distribute them on several switches of smaller ratings in series. This also makes it possible to obtain a significant improvement of the output waveform and to increase the apparent frequency of this wave, allowing a significant reduction of the filtering requirements [3], [4]. The use of capacitors for the voltage clamping instead of diodes as in DCMLI, permits several switch combinations for a particular voltage level generation, which may be used for preferential charging and discharging of capacitors. The control strategy proposed in this paper uses this inherent feature of FCMLI and is sufficient to have balanced dc voltages of the flying capacitors if the voltage of the main dc bus capacitor is balanced. Therefore, a complex dc capacitor voltage control loop is not required in an FCMLI-based FACTS controllers and independent control of the output voltage and flying capacitor voltages can be achieved. Even though the FCMLI offers various features, extensive researches have not been reported on its potential FACTS applications. It is probably due to some of its limitations such as requirements of large number of capacitors and their efficient control. Some researches such as [6] have reported control schemes for balancing the flying capacitor voltages, which use PI controllers for each flying capacitor voltage balancing. This control action makes the performance sluggish, controller parameters dependent and it may fail in transient conditions.

This paper proposes the design of a five-level FCMLI-based static synchronous compensator (STATCOM) and SSSC.

Manuscript received May 26, 2004; revised November 12, 2004. Paper no. TPWRD-00249-2004.

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Digital Object Identifier 10.1109/TPWRD.2005.855433

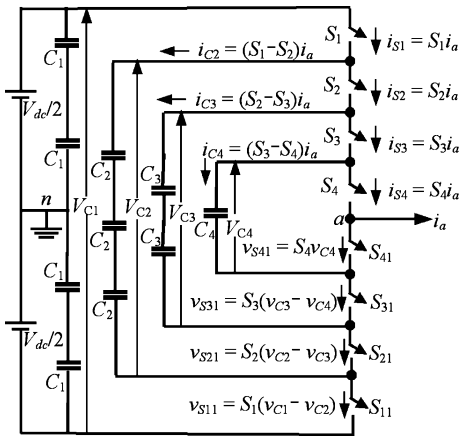

Fig. 1. One phase leg of a five-level Flying capacitor inverter.

A control scheme is derived which ensures that the flying capacitor voltages remain constant using their preferential charging and discharging. The stability studies of an SMIB system, compensated by the STATCOM and SSSC are performed using the PSCAD/EMTDC software.

II. Flying Capacitor Multilevel Inverter

A. Basic Configuration

Fig. 1 shows one phase of a five-level flying capacitor inverter. In the figure each switch S_1 to S_4 and S_{11} to S_{41} consists of a power semiconductor switch and an antiparallel diode. The pairs of the switches $(S_1, S_{11}), (S_2, S_{21}), (S_3, S_{31})$, and (S_4, S_{41}) are closed in complementary manner. Thus, if S_1 is ON, S_{11} is OFF and vice-versa. Each capacitor shown in the figure is of equal voltage rating. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor and call them C_1, C_2, C_3, and C_4. Then, C_1 is the main dc-link capacitor, which is required to be regulated externally. Therefore, either a battery of suitable rating is connected in place of C_1, or C_1, without the battery connected across it is regulated around a reference dc-link voltage using the real power exchange from the line as discussed in Sections III and IV. For a three-phase inverter two more phases of the same construction are coupled to the same dc-link. C_2, C_3, and C_4 are flying capacitors that provide the multilevel voltage ability to the converter. The flying capacitors of one phase are independent from those of other phases. If the voltage $V_{\rm C1}$ is $V_{\rm dc}$, then $V_{\rm C2}, V_{\rm C3}$, and $V_{\rm C4}$ are 3 $V_{\rm dc}/4, V_{\rm dc}/2$, and $V_{\rm dc}/4$, respectively. For any initial state of clamping voltages the inverter output voltage is given by

$$V_{\rm an} = S_1(V_{C1} - V_{C2}) + S_2(V_{C2} - V_{C3}) + S_3(V_{C3} - V_{C4}) + S_4 V_{C4} - V_{C1}/2. \quad (1)$$

In Fig. 1 and in (1), the switching states S_1 to S_4 take the value 1 if the corresponding switch is conducting and 0 otherwise. Based on (1), the switch combinations given in Table I are used to synthesize the output voltage $V_{\rm an}$ of phase-a with respect to the neutral point n. Table I also indicates the states of the flying capacitors corresponding to the switching combinations chosen. The state NC indicates that the capacitor neither charges nor discharges in this mode. The states + and − denote the charging and discharging respectively of the corresponding capacitors. The switching states given are for the positive half cycle of the current waveform (indicated as outgoing current i_a in Fig. 1). The capacitor states (+ and −) will reverse for the negative half cycle of the current.

TABLE I
Switching Scheme for One Phase Leg of a Five-Level FCMLI

S_1	S_2	S_3	S_4	C_2	C_3	C_4	V_{an}
ON	ON	ON	ON	NC	NC	NC	$+V_{dc}/2$
ON	ON	ON	OFF	NC	NC	+	$+V_{dc}/4$
ON	ON	OFF	ON	NC	+	−	
ON	OFF	ON	ON	+	−	NC	
OFF	ON	ON	ON	−	NC	NC	
OFF	OFF	ON	ON	NC	−	NC	0
OFF	ON	OFF	ON	−	+	−	
OFF	ON	ON	OFF	−	NC	+	
ON	OFF	OFF	ON	+	NC	−	
ON	OFF	ON	OFF	+	−	+	
ON	ON	OFF	OFF	NC	+	NC	
ON	OFF	OFF	OFF	+	NC	NC	$-V_{dc}/4$
OFF	ON	OFF	OFF	−	+	NC	
OFF	OFF	ON	OFF	NC	−	+	
OFF	OFF	OFF	ON	NC	NC	−	
OFF	OFF	OFF	OFF	NC	NC	NC	$-V_{dc}/2$

The output voltage for an n-level inverter can similarly be defined. In general, an n-level FCMLI requires $(n-1)$ pairs of power semiconductor devices and $(n-1)\times(n-2)/2$ clamping capacitors per phase leg in addition to $(n-1)$ main dc bus capacitors provided all the capacitors are of equal value. The number of capacitors can be reduced by sizing the capacitors in a single leg as an equivalent one. The size of the voltage increment between two consecutive clamping legs defines the size of voltage steps in the output waveform. The voltage of the innermost clamping leg (e.g., C_4 in Fig. 1) clamping the innermost two devices is $V_{\rm dc}/(n-1)$. The voltage of the next innermost clamping leg will be $V_{\rm dc}/(n-1) + V_{\rm dc}/(n-1) = 2V_{\rm dc}/(n-1)$ and so on. Thus, each next clamping leg will have the voltage increment of $V_{\rm dc}/(n-1)$ from its immediate inner one. The voltage stress across each capacitor is $V_{\rm dc}/(n-1)$. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assure that the voltage stress across each main device is same and is equal to $V_{\rm dc}/(n-1)$. The line-to-line output voltage of the inverter varies from $+V_{\rm dc}$ to $-V_{\rm dc}$ and has $(2n-1)$ levels in the output, while the phase voltage varies from $+V_{\rm dc}/2$ to $-V_{\rm dc}/2$ with n-levels.

It can be seen from Table I that the structure offers multiple switching combinations for $V_{\rm an} = V_{\rm dc}/4, 0$, and $-V_{\rm dc}/4$. Since such redundancies are available, one can choose a preferential switching state that will help in maintaining the capacitor voltages constant. However, the switching combination chosen affects the current rating of the capacitors. For example, for $V_{\rm an} = V_{\rm dc}/4$, if the first and the last combinations are used (Table I), only one capacitor (C_4 or C_2) is involved. In the other two combinations more than one capacitor are required to be charged or discharged. Therefore, the rms current ratings of the capacitors will necessarily be higher for the single capacitor case than that in the two-capacitor case. This feature of different current rating is present in almost every case (except

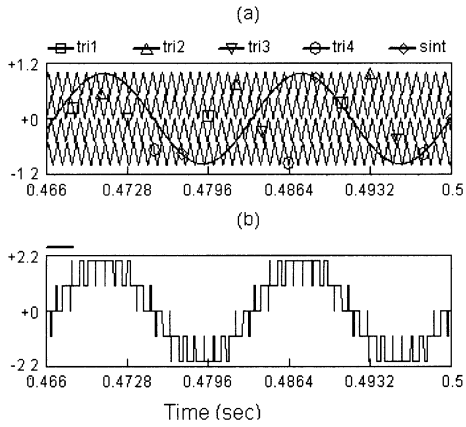

Fig. 2. Modulation scheme. (a) SPWM. (b) Output waveform.

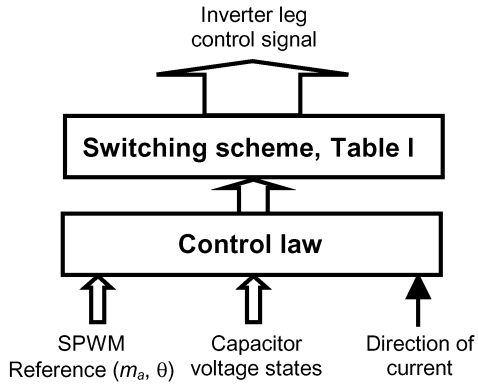

Fig. 3. Control algorithm block diagram.

for the levels of $V_{\rm dc}/2$ and $-V_{\rm dc}/2$). The switching sequence chosen therefore affects the rms current ratings of the capacitors. Thus, optimization of the switching sequence is required, i.e., one that minimizes the capacitor cost and the system losses. This is not readily available in the literature for the FCMLI.

B. Modulation Scheme

Of the various strategies developed to improve the output voltage and reduce the harmonics, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method for an n-level inverter, $(n-1)$ carrier waves are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by their intersections. The output signal of the comparator resembles with the output voltage waveform of the inverter and decides the voltage level that must be generated at a particular instant. For a five-level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter as shown in Fig. 2. The modulating signals of each phase are displaced from each other by 120°. The phase shift angle of the modulating signal, i.e., θ depends on the application requirements, as discussed Sections III and IV. The modulation index m_a is given by

$$m_a = A_m/2A_c \tag{2}$$

where A_m is the amplitude of the modulating signal and A_c is that of one carrier wave (peak to peak). Some researches have been reported about the relations between the phases and frequencies of the carrier waves and the shape of the modulating signal to reduce the output voltage harmonics of the multilevel inverters [3], [4], [8], [9]. Here, the carrier waves are taken to have phase displacement of 120° for smallest distortion in the output [3] and their frequency is taken as n_c times to that of the modulating signal, where n_c is a multiple of three so that triplen harmonic cancellation takes place across the three-phase inverter load [9].

The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from $+0.98$ to -0.98. The amplitudes of the four carrier waves are from 0 to 0.5, 0.5 to 1, in the positive half cycle of the modulating signal, and from 0 to -0.5, -0.5 to -1 in the negative half cycle. The modulating signal and four carrier waves are compared in four comparators, on instantaneous basis. The comparator output is $+1$ when the modulating signal exceeds the carrier wave and zero otherwise. The binary outputs of these comparators are combined arithmetically to produce the levels $(+2, +1, 0, -1, -2)$. The so-generated SPWM output reference signal is shown in Fig. 2(b). This signal resembles the output voltage waveform of the inverter and decides the voltage level, which is to be generated at a particular instant.

C. Control Strategy for FCMLI

In an n-level inverter, there are $(n+1)$ possible switching states that supply the zero voltage level, $(n-1)$ possible switching states for the next higher level, and so on (excepting the levels $\pm V_{\rm dc}/2$, which have only one switching combination each). The control scheme proposed here utilizes this feature to readily control the flying capacitor voltages around their reference values while at the same time generating the desired voltage level at the output. The control system block diagram is shown in Fig. 3. The main dc bus voltage is assumed here to be regulated externally as discussed later in Sections III, IV. For a five-level inverter with the dc bus voltage of $V_{\rm dc}$, the reference values of the capacitor voltages V_{C4}, V_{C3}, and V_{C2} (Fig. 1) are $V_{\rm dc}/4, V_{\rm dc}/2$ and $3V_{\rm dc}/4$, respectively. The modulation scheme discussed in Section II–B defines the voltage level to be generated at a particular instant (Fig. 2). In addition, the control scheme requires the information about the direction of the output current of the inverter and about the capacitor voltage states, which are obtained from suitable sensors and circuits.

Suppose the desired output voltage level is $V_{\rm dc}/4$ and the direction of current is positive, i.e., outgoing (Fig. 1). Referring to Table I, out of the four possible combinations of the switches for $+V_{\rm dc}/4$, a particular combination is chosen comparing the capacitor voltage states with respect to their reference values. Thus, the capacitor voltage level will be characterized by a logic signal, which is either *high* or *low*. The signal is *high* if the capacitor voltage is greater than its reference (e.g., $V_{\rm dc}/4$ for the innermost clamping leg) and is *low* if it is lower. Based on this information a switching combination will be chosen, which will cause the flying capacitor voltage to increase or decrease toward its reference value. Therefore, depending upon the time

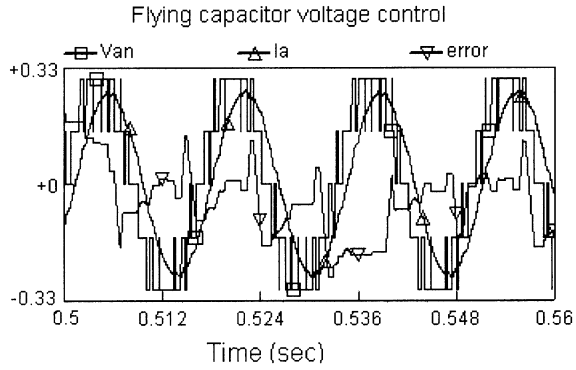

Fig. 4. Control scheme response.

interval for a particular voltage level output, the control scheme may choose more than one combination (one after another) for the same voltage level output, if the difference between the reference and the actual capacitor voltage changes its sign. If for a particular desired voltage level, all the flying capacitors are at their reference values, the control scheme will choose the combination of switches, which will have most "NC" capacitor states (Table I).

Fig. 4. shows the inverter output phase voltage $(v_{\rm an})$, corresponding current (i_a) (amplified by 10 times in the plot) and the error (error) (amplified by 50 times) between the reference voltage of the innermost leg $(V_{\rm dc}/4)$ and its actual value (V_{C4}), i.e., error $= 50 \times (V_{\rm dc}/4 - V_{C4})$. Units in this figure are kilovolts for voltage and kiloamps for current.

It can be seen that the capacitor (C_4) either charges or discharges or remains unaffected depending on the output voltage level and the direction of current. In a similar manner all the other flying capacitor leg voltages are regulated and hence are managed to remain balance. The reference values for the flying capacitor voltages are taken with respect to the main dc-link voltage $V_{C1} = V_{\rm dc}$. Therefore, in a certain application if the external control changes V_{C1} and the dc battery is absent, the flying capacitor voltages accordingly follow their new reference values in a time that depends on the current and on the capacitors.

D. Five-Level FCMLI Simulation Results

A five-level FCMLI is simulated using PSCAD/EMTDC (version 3) simulation package. The inverter is supplying a balanced three-phase star connected *RL*-load with $R = 10\ \Omega$ and $L = 15.416$ mH. The five-level inverter parameters are given in Table II. The inverter devices have been assumed to be nearly ideal in this simulation. Total of nine flying capacitors are used-three of 8000 μF, three of 4000 μF, and the other three of 2666.67 μF (equivalent capacitor in each leg is used) (Fig. 1). The dc-link voltage is $V_{\rm dc} = 0.6$ kV, carrier wave frequency is 1260 Hz and the system frequency is 60 Hz. The modulation index is 0.98. The performance of the control algorithm proposed above is evident when considering the phase voltage and the capacitor voltages shown in Fig. 5 and line voltages and currents shown in Fig. 6.

The phase voltage waveform is composed of voltage amplitudes having levels of $V_{\rm dc}/2, V_{\rm dc}/4, 0, -V_{\rm dc}/4$, and $-V_{\rm dc}/2$.

TABLE II
FIVE-LEVEL INVERTER PARAMETERS

Number of main switches	24
Device ON resistance	0.01 Ω
Device OFF resistance	1.0E6 Ω
Forward voltage drop	0.0 kV
Forward breakover voltage	0.2 kV
Reverse withstand voltage	0.2 kV
Snubber resistance	500.0 Ω
Snubber capacitance	25 μF

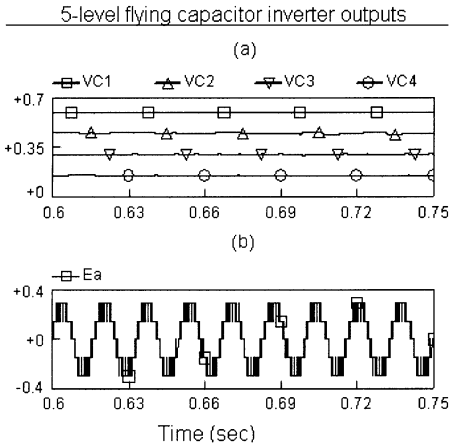

Fig. 5. Capacitor voltages and phase voltage. (a) Capacitor voltage (in kilovolts). (b) Phase-a output voltage (in kilovolts).

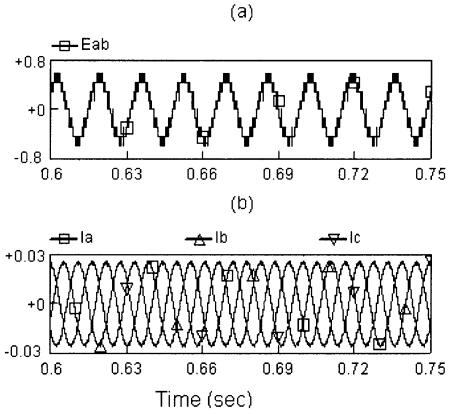

Fig. 6. Line voltages and currents. (a) Output line voltage (in kilovolts). Eab. (b) Output currents (in kiloamps).

This implies that the control algorithm is able to keep the requested discrete voltage level. On the other hand, the clamping leg voltages have been tightly regulated around their reference values, i.e., 0.15 kV $(V_{\rm dc}/4)$, 0.30 kV $(V_{\rm dc}/2)$, and 0.45 kV $(3\ V_{\rm dc}/4)$, as expected. The fluctuations in capacitor voltages are small and within 3.0% of their corresponding reference values. This can be further reduced by increasing capacitance values and the carrier frequency. Hence, by having balanced flying-capacitor voltages, the regular amplitude of the discrete voltage levels are assured and at the same time the input voltage is equally shared by the serial-connected power semiconductor devices. The line to line voltages have nine levels with peak values $\pm$ 0.6 kV. The current can be smoothed further by increasing the inductances of the load. The voltages and

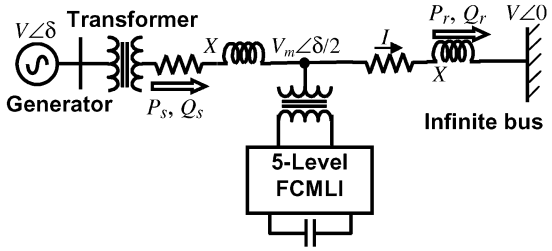

Fig. 7. STATCOM compensated single machine infinite bus system.

TABLE III
MACHINE DATA

S_N	700 MVA	X_d	1.014 p.u.
H	3.117 sec	X_p	0.163 p.u.
X_q	0.770 p.u.	X_d^1	0.314 p.u.
X_d^{11}	0.280 p.u.	T_{do}^1	6.55 sec
X_q^{11}	0.315 p.u.	T_{do}^{11}	0.039 sec.
T_{qo}^{11}	0.071 sec.	ω	376.9911 rad sec^{-1}

currents shown in Fig. 6 are analyzed with the Fourier series analysis. The resulting total harmonic distortion (THD) of the output line voltage $E_{\rm ab}$ is 0.98% and that of the current i_a is 0.93%, which is much less than that observed with other control methods and even for higher levels with comparable carrier wave frequency in [3]–[7] and are well within the limits of IEEE Stand. 519–1992 [10]. Hence, the multilevel inverter is capable of generating a "more sinusoidal" waveform without using much higher switching frequency and with lower device ratings. The THD can be further minimized by increasing the capacitance of the flying capacitors and/or increasing the carrier wave frequency.

III. FIVE-LEVEL FCMLI BASED STATCOM

This section describes the use of the STATCOM based on the five-level flying capacitor inverter for power oscillation damping and voltage control of power system. The study is based on an SMIB system with the STATCOM connected in shunt at the midpoint of the transmission line.

A STATCOM is a device that can provide reactive power support to a bus. It is useful in improving the transient stability, power oscillation damping, voltage stability, and increase in power transfer limit of the connected power system [1]. It consists of a voltage source inverter connected to an energy storage device on one side and to the power system on the other side. A STATCOM can be viewed as a controllable ac voltage source, which appears behind a transformer leakage reactance. The active and reactive power transfer is caused by the voltage difference across this reactance. Usually, the inverter output voltage is almost in phase with the voltage of the ac system. Therefore, only reactive power transfer occurs, whose quantity and sign depend on the magnitude of the inverter output voltage vis-à-vis that of midpoint ac voltage. If it is higher than ac system voltage the reactive power is supplied to the system and if it is lower the converter circuit absorbs the reactive power. The magnitude of the inverter output voltage depends on the modulation index and the dc-link voltage.

TABLE IV
TRANSMISSION LINE SPECIFICATIONS

Length of the line	100 km
+ve seq. resistance	0.36294e–4 (Ω m^{-1})
+ve seq. inductive reactance	0.5031e-3 [Ωm^{-1}]
+ve seq. capacitive reactance	302.151 (Ω^{-1} m)
Zero seq. resistance	0.37958e–3 (Ω m^{-1})
Zero seq. inductive reactance	0.13277e–2 (Ω m^{-1})
Zero seq. capacitive reactance	419.34 (Ω^{-1} m)
Number of conductors	3

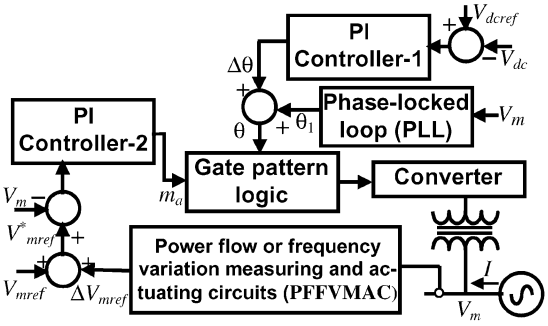

Fig. 8. Block diagram of the STATCOM control scheme.

The schematic diagram of the test system is shown in Fig. 7. The specifications of the generator are given in Table III.

The generator is installed with an exciter of type AC1A and the system frequency is 60 Hz. The phase of the machine terminal voltage at time $t = 0$ is 10° and is connected to the transmission line through a $13.8(\Delta)/230(\Upsilon)$-kV, 700-MVA transformer with delta winding lagging the star winding. The positive sequence leakage reactance of the transformer is 0.005 p.u. and is assumed to have zero no load losses. The Bergeron model (built in transmission line model in PSCAD/EMTDC version 3) of transmission line of 100 km. has been used in this simulation. The specifications of the transmission line are given in Table IV. The infinite bus corresponds to an ideal voltage source with line-to-line rms voltage of 230 kV. The inverter is connected at the mid point of the power system through a $40(\Delta)/400(\Upsilon)$-kV, 400-MVA transformer, with the high-voltage side connected to the power system and having zero no-load losses. Its positive sequence leakage reactance is 0.11 p.u. The inverter parameters are the same as given in Table II, except that the forward breakover and reverse withstand voltages of the power semiconductor devices are now taken as 10 kV. In addition to the nine-flying capacitors, discussed in Section II.D, two more capacitors of 4000 μF are needed for dc-link (Fig. 1) without the dc-battery connected across it.

There are many strategies to control the operation of STATCOM such as PI control, pole placement control and linear quadratic control [11]. The PI control scheme has been used here to study the performance of the system. The control system block diagram is given in Fig. 8. In normal operation, for the voltage control of a bus, the value of $V^*_{m\rm ref}$ depends on the desired voltage profile at that particular bus; therefore, the power flow or frequency variation measuring and actuating circuits (PFFVMAC) are not needed. The rest of the control logic is the same, as shown in Fig. 8. The PFFVMAC block is needed

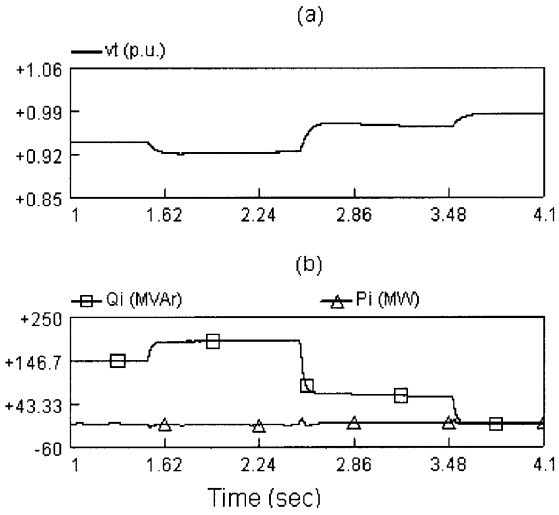

Fig. 9. Mid-point voltage regulation and powers supplied by the inverter. (a) Mid-point voltage. (b) Real and reactive power supplied by the inverter.

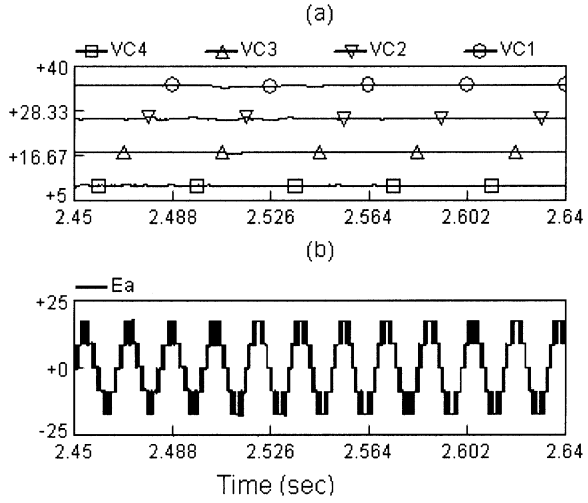

Fig. 10. Capacitor voltages and output phase voltage of the inverter. (a) Capacitor voltages (in kilovolts). (b) Inverter output phase Voltage (in kilovolts).

when some feedback signal is taken from the power system for improving the transient stability of the system. There are two control objectives in the STATCOM control: ac-bus voltage control and dc-link voltage control. Therefore, two internal control loops containing two PI controllers are used here. The dc capacitor voltage $V_{\rm dc}$ is regulated around a reference value $V_{\rm dc\,ref}$, which is kept fixed and is chosen considering the rating of the STATCOM. Since the output voltage of the inverter and V_m should be in phase, a phase-locked loop (PLL) is used that has V_m as input and angle θ_1 as output. Ideally, for pure reactive power exchange between the compensator and the line, the dc link voltage should remain constant. However, the capacitor discharges due to losses in switching, snubber circuits, and in transformers. Therefore, to keep the capacitor voltage constant, some amount of real power exchange is needed between the inverter and the ac system. The PI controller-1, with an input of the error between $V_{\rm dc\,ref}$ and $V_{\rm dc}$ and output $\Delta\theta$ facilitates this power exchange. If the inverter output voltage is made to lag the voltage of the ac system then the active power flow is from the ac system to the dc side of the inverter charging the capacitor. The reverse will happen when the corresponding phase relation is reversed.

Another control loop (PI contoller-2) generates the modulation index (m_a) (Section II-B). The input to this PI controller is the difference between the reference rms value $V^*_{m\rm ref}$ and the actual rms value of the voltage V_m at the point of connection. Therefore, in the control system shown in Fig. 8, one loop sets the angle of the injected voltage to regulate the dc capacitor voltage while the other loop sets the modulation index to generate the required voltage profile. In Fig. 8, the Gate pattern logic block corresponds the control block diagram shown in Fig. 3 and m_a and θ corresponds to the SPWM reference input to the block.

Before making the inverter functional, the dc-link capacitor and the individual flying capacitors are initially charged to their reference values using the method given in [7]. Typically, the modulation index control would be faster than the phase angle control, as there is a significant charging and discharging "inertia" of the capacitors, whereas the modulation index has an immediate effect on the output voltage of the controller. Based on these, the PI controller-1 gains are chosen as $K_P = 5.0, K_I = 0.01$, and that of the controller-2 are $K_P = 200, K_I = 10.0$. The reference value of the dc-link voltage is set at 35 kV. Fig. 9 shows the mid-point voltage regulation and the corresponding real and reactive power supplied by FCMLI.

The reference midpoint voltage $(V^*_{m\rm ref})$ is changed in steps at the interval of 1.0 sec, and it can be seen that the STATCOM is able to regulate the midpoint voltage in accordance with $V^*_{m\rm ref}$. The settling time of the midpoint voltage is 0.1 sec, which depends on the interconnecting circuit parameters of the inverter and the power system. The reactive power transfer varies as per the requirements, showing the operation of the STATCOM in both inductive and capacitive modes. The real power required by the STATCOM has an average value of 1.45 MW, which corresponds to the losses in the inverter and in the interconnecting transformer and circuits. The maximum and minimum values of real power exchange are 1.98 and 0.92 MW, respectively, whose differences from the average value correspond to the charging and discharging of capacitors. Fig. 10 shows the main dc link capacitor voltage V_{C1}, flying capacitor voltages V_{C2}, V_{C3}, and V_{C4} of one phase, and the phase-a output voltage of the inverter.

At 2.50 sec, when $V^*_{m\rm ref}$ changes, the inverter output voltage changes almost without any time lag, as is evident from Fig. 10. The dc-link voltage, and hence, the flying capacitor voltages are unaffected following the change in $V^*_{m\rm ref}$. Thus, the simulation results justify the control scheme for independent control of the output voltage and the dc-link and, hence, flying capacitor voltages.

The dynamics of the power system can be expressed by the transient model given by

$$\frac{d\delta}{dt} = \Delta\omega \approx \Delta f \approx \int P_e dt$$
$$\frac{d\omega}{dt} = \frac{\omega_o}{2H}\left[P_m - P_e - \frac{D}{\omega_o}\Delta\omega\right] \tag{3}$$

where δ is the rotor angle of the generator (in radians), ω is the speed of the rotor shaft (in radians per second), f is the frequency of the system (in Hertz), H is the inertia constant (in megawatt secons per MVA), P_m is the mechanical power (per unit), P_e is the electrical power (per unit), and D is the damping coefficient (per unit). The real power expression with the STATCOM connected at the midpoint is given by

$$P_e = \frac{VV_m}{X} \sin \delta/2 \tag{4}$$

where V is the source voltage, and the other parameters correspond to that shown in Fig. 7.

In the case of an underdamped power system, any minor disturbance may cause the machine angle to oscillate around its steady state value at the natural frequency of the total electromechanical system. This results in a corresponding power oscillation around the steady state power transmitted. The lack of sufficient damping may be a major problem in some power systems, and in some cases, it may be the limiting factor for the transmittable power. It can be seen from (3) and (4) that the angle dynamics can be changed by varying P_e. When the rotationally oscillating generator accelerates and angle δ increases $(d\delta/dt > 0)$, the electric power transmitted must be increased to compensate for the excess mechanical input power. Conversely, when the generator decelerates and δ decreases $(d\delta/dt < 0)$, the electric power must be decreased to balance the insufficient mechanical input power. (The mechanical input power is assumed to be essentially constant in the time frame of an oscillation cycle). The STATCOM does this function by transmitting reactive power to the power system. The capacitive output of the compensator increases the midpoint voltage and hence the transmitted power when $d\delta/dt > 0$, and it decreases those when $d\delta/dt < 0$. The control scheme for the STATCOM shown in Fig. 8 uses the PFFVMAC block, which senses the variations in the frequency or power flow across the line following the disturbance, as is evident from (3) and (4). The PFFVMAC block outputs $\Delta V_{m\text{ref}}$, which has either positive value for $d\delta/dt > 0$ or negative value for $d\delta/dt < 0$. Positive $\Delta V_{m\text{ref}}$ is summed to the fixed reference voltage signal $V_{m\text{ref}}$, producing a higher reference value $V^*_{m\text{ref}}$ and, hence, higher P_e. Similarly, negative $\Delta V_{m\text{ref}}$ lowers the value of P_e and in this way the oscillations are damped out within few cycles. On the basis of this model, the contribution of the STATCOM in improving transient stability and damping system oscillations are studied through the next simulations.

A bolted three-phase fault is applied at the middle of the line near the STATCOM at 3.0 sec. The fault is applied for 0.30 sec, after which, it is cleared. After the fault is cleared, it is required to transfer maximum or minimum power across the line considering the rating of the STATCOM. This is achieved by setting the controllable parameter i.e., $\Delta V_{m\text{ref}}$ (Fig. 8) to its maximum (or minimum) value determined by the STATCOM rating [1], [12]. The simulations results shown in Figs. 11 and 12 show the effectiveness of power system oscillations damping using the proposed STATCOM. Fig. 11 shows the rotor speed and power oscillations following the fault of both the compensated and uncompensated systems. The uncompensated system corresponds to the same SMIB system without the STATCOM connected

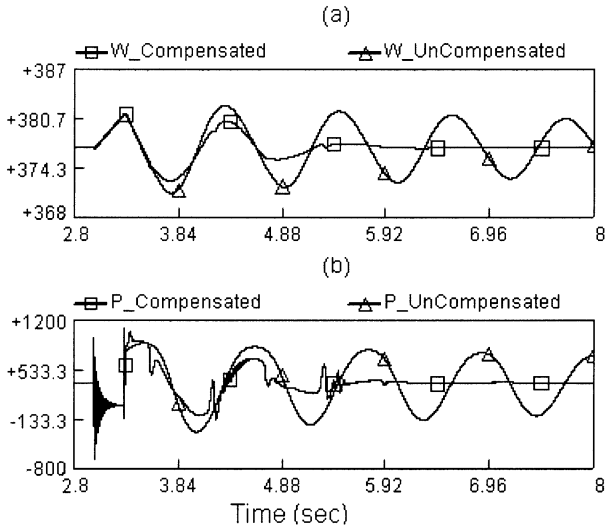

Fig. 11. Rotor speed and active power oscillations following the fault. (a) Rotor speed oscillation (in radians per second). (b) Power oscillation.

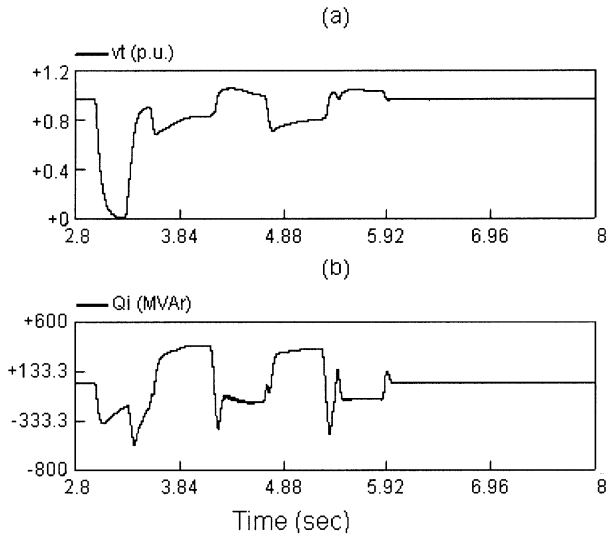

Fig. 12. Midpoint voltage and the reactive power supplied by the inverter.

to it. While the uncompensated system keeps on oscillating for the operating time shown, the compensated system achieves its steady state values within few cycles. Fig. 12 shows the reactive power supplied by the inverter, which varies from capacitive to inductive zone as required for damping and the corresponding midpoint voltage variation. These attain their steady-state values with the speed and rotor angle. It can be seen from Fig. 11 that the controller can be effectively applied to damp out the oscillations in two to three cycles with the proposed STATCOM for fault duration of as large as 0.30 sec. The damping can be further improved by using more robust controls as are discussed in [11].

The rapid response of the inverter corresponding to a changed reference and its effective control strategy to balance the flying capacitor voltages, assure better operations as compared to other inverters discussed in Section I and causes the system to attain its steady state relatively faster. Further, it can be seen from Fig. 12 that a reactive power exchange of maximum 370.5 MVAr occurs with the power system in the first swing and correspondingly in the others to damp out the fault within

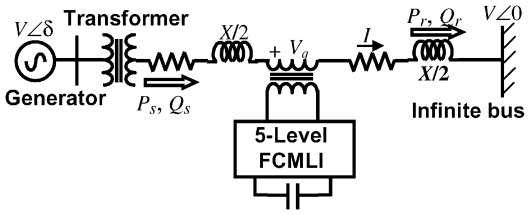

Fig. 13. SSSC compensated single machine infinite bus system.

three cycles. A higher rating inverter will damp out the oscillations even faster. Conventional inverters have practical limits in achieving such higher rating as is discussed in Section I. A practical STATCOM discussed in [13] employing three-level inverters of different configuration and another one in [1] using multistep inverter use more number of power semiconductor devices and capacitors of comparable ratings in addition to large filters as compared to that discussed in the present paper. They achieve ratings of $+133/-41$ MVA and ± 120 MVAr, respectively. With such large number of devices as in [13], a seven level of flying capacitor inverter can be designed, which will have even higher rating and much less THD. Therefore, for high power applications, FCMLI with the proposed control strategy is better suited as compared to the other inverters. In addition, it offers less THD and therefore the filter size requirements are less.

IV. Five-Level FCMLI-Based SSSC

This section describes the use of SSSC based on a five-level flying capacitor inverter for power flow control and transient stability improvement of a power system. An SSSC has same configuration of power circuit as STATCOM but different configuration of control. It is connected in series with the transmission line and injects a voltage of controllable magnitude and phase, which is almost in quadrature with the line current and thereby controlling the transmitted electric power. The detailed description of the SSSC can be found in [1], [12], and [14].

The schematic diagram of the test system is shown in Fig. 13. The specifications of the SMIB system used are same as given in Section III.

The five-level inverter is connected to the transmission line through three single-phase transformers. Each transformer has a leakage reactance of 0.10 p.u., zero no-load loss, and a rating of $40/20$ kV, 200 MVA. To allow the zero sequence currents to flow during faults, the secondary windings of these three transformers are connected in delta. The inverter parameters are the same as used for STATCOM application in Section III. The injected voltage V_q can be expressed as

$$V_q = -jX_q I \tag{5}$$

where X_q is the equivalent reactance imposed by the SSSC to the power system. It takes negative value when the SSSC operates in inductive mode and positive for capacitive mode. Then, the real and reactive power transfer from the source of the compensated system can be expressed as

$$P_s = \frac{V^2}{X_{\text{eff}}} \sin\delta, \quad Q_s = \frac{V^2}{X_{\text{eff}}}(1-\cos\delta) \tag{6}$$

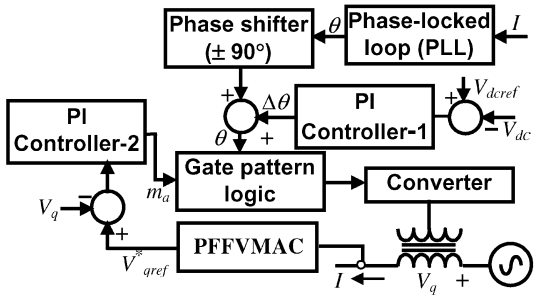

Fig. 14. Control system block diagram of the SSSC.

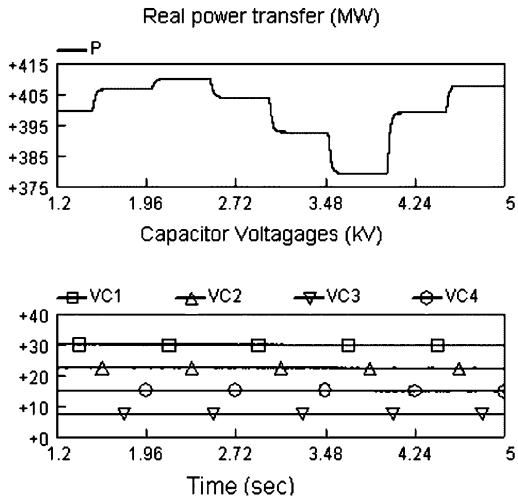

Fig. 15. Power flow control by the SSSC.

where $X_{\text{eff}} = X - X_q$. The magnitude of the inverter output voltage depends on the modulation index and the dc-link voltage.

The control system block diagram is given in Fig. 14. The scheme is similar to that shown in Fig. 8.

For reactive compensation by the SSSC, the voltage injected by it (V_q) should be in phase quadrature with that of the line current. Therefore, a phase shift of $\pm 90°$ is introduced with θ_1. The input to PI controller-2 is the difference between the reference rms value of the injected voltage $(V^*_{q\text{ref}})$ and the actual rms value of the injected voltage (V_q). To control the power flow across the line in normal operation of the SSSC, the PFFVMAC block (discussed in Section III) is not needed and $V^*_{q\text{ref}}$ is calculated from the power flow demand over the line with the help of the known system parameters [1], [12], [14].

Before making the inverter functional, the dc-link capacitor and the flying capacitors are charged [7]. Fig. 15 shows the power flow control action by the SSSC, as power flow demand and hence $V^*_{q\text{ref}}$ is changed each time at the interval of 0.50 sec. in the operating time shown. For power flow control, the generator is taken as a constant voltage source, i.e., with constant δ of same rating as what considered in Section III. The PI controller-1 gains are chosen as $K_P = 0.001$, $K_I = 0.0001$, and that of the controller-2 are $K_P = 80$,$K_I = 4.5$. The reference value of the dc-link voltage is set at 30 kV. The smooth and fast power flow control shown in Fig. 15 leads to similar

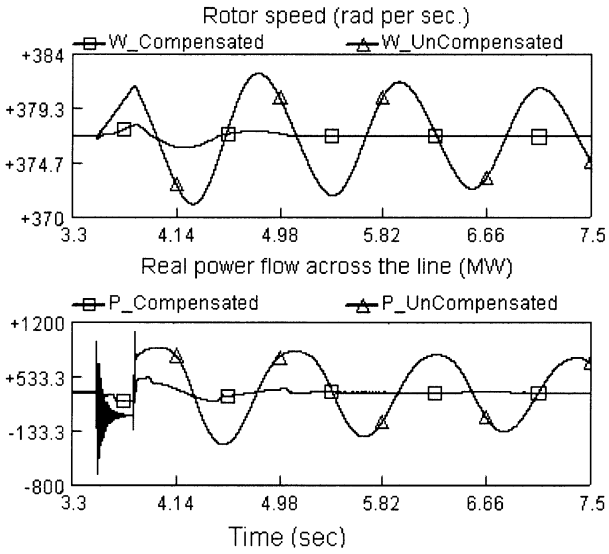

Fig. 16. Rotor speed and active power oscillations following the fault.

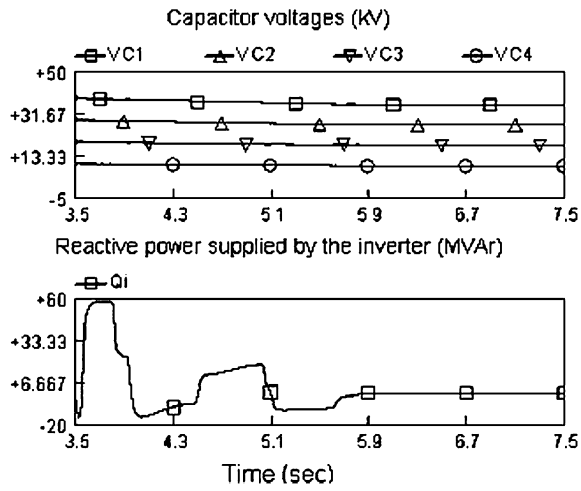

Fig. 17. Capacitor voltages and reactive power supplied by the inverter.

observations that made in Section III for midpoint voltage regulation. It can be seen that with the smooth power flow control, the dc-link voltage and hence the flying capacitors voltages remain balanced. The results show the effectiveness of the FCMLI-based SSSC for power flow control and also of the control scheme employed.

Following a disturbance or a fault, which has resulted in the angle and power oscillations, the SSSC works in capacitive mode when $d\delta/dt > 0$ and in inductive mode when $d\delta/dt < 0$ and thereby increasing the damping. This can be justified from (3), (5), and (6). In this way, the oscillations are damped out within few cycles. The PFFVMAC block, discussed in Section III, performs this operation by sensing the frequency or power flow variation across the line. A positive value of $V^*_{q\mathrm{ref}}$ does the capacitive operation and its negative value does the inductive operation. Following the fault as extreme power transfers have to be achieved, the controllable parameter, i.e., $V^*_{q\mathrm{ref}}$ is set to its maximum (minimum) value depending on the inverter rating [12].

The simulations results shown in Figs. 16 and 17 show the effectiveness of power system oscillations damping using the proposed SSSC. A bolted three-phase fault is applied in the middle of the line near the SSSC location at 3.50 sec. The fault lasts for 0.3 sec and is then cleared. The system conditions are same as what taken in Section III for power oscillation damping. Fig. 16 shows the rotor speed and power oscillations following the fault of both the SSSC compensated and uncompensated systems.

While the uncompensated system keeps on oscillating for the operating time shown, the compensated system achieves its steady state within two to three cycles.

Fig. 17 shows the dc-link capacitor voltage and the flying capacitor voltages of phase-a. It can be seen that the dc-link, and hence, the flying capacitors hold their voltages under changing system conditions. The result verifies the control scheme and its objectives proposed in Section II-C. The reactive power supplied by the inverter is also shown, which is either inductive or capacitive depending on the mode of operation.

It can be observed that for same rating of the inverter, the SSSC is more effective in damping the oscillations than the STATCOM following the same disturbance in an identical power system [12].

The simulation results confirm the operation of the flying capacitor voltage balancing mechanism for the FCMLI. The proposed FACTS controllers based on the FCMLI also show satisfactory results. Time response in all cases is about or less than three cycles, which is adequate for transmission systems.

V. Conclusion

In this paper, a proposal has been made for series and shunt compensations based on five-level flying capacitor inverter. The basic concepts and operational features of the inverter have been explored. A control scheme has been proposed which uses the preferential charging or discharging of flying the capacitors to balance their voltages. The control scheme allows balanced flying capacitor voltages and, hence, output phase and line voltages as desired with much less THD using the SPWM. The simulation results verify the control scheme proposed. A STATCOM and an SSSC have been simulated based on the five-level inverter. The proposed STATCOM and SSSC generate output voltage waveform with lower harmonic distortion and allow higher power handling capability. The control circuits for both the compensators have been described for power oscillations damping and for their normal operations. The performances of the compensators have been tested on an SMIB system, subjected to a bolted three-phase fault. The simulation results confirm that the proposed STATCOM and SSSC have satisfactory performances.

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