Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter

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***Abstract*—This paper proposes a flying-capacitor-based chopper circuit for dc capacitor voltage equalization in diode-clamped multilevel inverters. Its important features are reduced voltage stress across the chopper switches, possible reduction in the chopper switching frequency, improved reliability, and ride-through capability enhancement. This topology is analyzed using three- and four-level flying-capacitor-based chopper circuit configurations. These configurations are different in capacitor and semiconductor device count and correspondingly reduce the device voltage stresses by half and one-third, respectively. The detailed working principles and control schemes for these circuits are presented. It is shown that, by preferentially selecting the available chopper switch states, the dc-link capacitor voltages can be efficiently equalized in addition to having tightly regulated flying-capacitor voltages around their references. The various operating modes of the chopper are described along with their preferential selection logic to achieve the desired performances. The performance of the proposed chopper and corresponding control schemes are confirmed through both simulation and experimental investigations.**

***Index Terms*—Chopper, diode-clamped multilevel inverter (DCMLI), flying capacitor, four-level, multilevel, three-level.**

I. Introduction

AMONG THE multilevel voltage-source-inverter configurations, the diode-clamped multilevel inverter (DCMLI) is widely accepted for applications in high-power drives and utility systems [1]–[22]. It possesses some of the desirable features like the following: 1) the dc capacitors can be easily precharged as a group; 2) switching control is easiest; and 3) the protection circuit required is least complex among the multilevel inverters, etc. [1]–[7]. Moreover, by using a DCMLI, the multilevel voltage outputs are easily obtained with a low-cost string of the dc capacitors. However, these features, for more than three levels, are achieved at the expense of the divergence of dc capacitor voltages, resulting in the collapse of some and rise of others due to the nonuniform power drawn from them [1]–[3], [8]–[18], [23]–[38]. This may result in poor quality voltage outputs, affecting the control performance and causing a violation in the safe operating limits leading to inverter malfunctioning. Therefore, balancing of the dc capacitor voltages is required under all conditions, which determines both the safety and efficiency of DCMLIs [1]–[3].

Two possible solutions of the voltage imbalance problem exist: 1) installing of voltage-balancing circuits on the dc side of the inverter [8]–[16], [23]–[25] and 2) modifying the converter switching pattern according to a control strategy [17], [18], [26]–[38]. The latter is definitely preferable in terms of cost, as the former requires additional circuits and power hardware, which add to the system cost and complexity. For applications involving only reactive power [like static compensators (STATCOMs)], the switching pattern modification strategies can be used for voltage balancing. However, voltage balancing would influence reactive power control if priority were given to voltage balancing [8]. Moreover, the switching pattern modification strategy cannot be used to control the capacitor voltage, except at low modulation indexes [24], [36], [37]. For higher level inverters, the voltage balancing through switching pattern modification strategies limits the output voltage to 50% of the maximum [25]. Furthermore, a medium- or high-voltage power converter intended for installation on a utility grid is required to be more reliable and robust against line faults and transients. It is also to be noted that, for applications like a unified power flow controller (UPFC), where two such converters are connected back to back, the switching modification strategy necessitates the two converters to operate at a fixed ac voltage ratio for the capacitor voltage equalization [10]. This constraint would seriously limit the flexibility of UPFC. Therefore, extra capacitor voltage control circuits are preferably used in practice [1], [2], [7]–[15].

There are many articles available in literature discussing the extra control circuits for dc capacitor voltage balancing in DCMLIs, which are mostly bidirectional buck–boost choppers [8]–[16], [23]–[25]. In [8]–[12], such circuits are successfully tested when DCMLI is used for STATCOM applications. Similar chopper-based capacitor voltage balancing is achieved when DCMLI is used for UPFC applications as reported in [13] and [14]. The performance of the back-to-back-connected five-level diode-clamped converters supported by a pair of buck–boost choppers for dc capacitor voltage balancing is found to be effective as well [15], [16]. A similar buck–boost chopper was implied for unidirectional current control for the dc capacitor voltage balancing in [23]. A balancer circuit based on the three-level diode-clamped chopper configuration is reported in [24]. It has the advantage that lower rated devices may be used in

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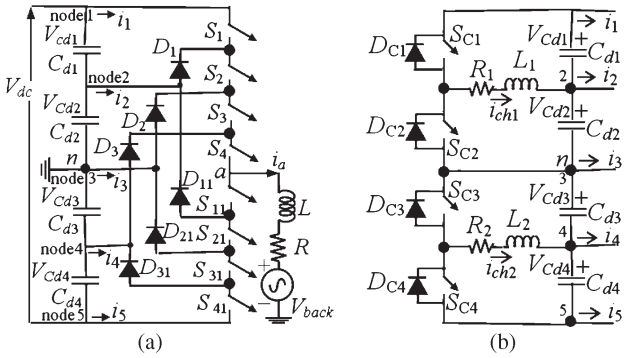

Fig. 1. (a) One phase leg of a five-level diode-clamped inverter and (b) conventional chopper for dc capacitor voltage balancing in DCMLI.

TABLE I
SINGLE-PHASE FIVE-LEVEL DCMLI SWITCHING SCHEME

S_1	S_2	S_3	S_4	S_{11}	S_{21}	S_{31}	S_{41}	V_{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

the chopper compared with that in the conventional buck–boost choppers.

In this paper, a flying-capacitor-based chopper circuit is proposed to overcome the voltage imbalance problems among the dc capacitors of a DCMLI. As compared to the conventional chopper, it requires additional power semiconductor devices of lower rating and capacitors. For generalization purposes, the proposed topology is analyzed using two configurations which are termed as three-level and four-level choppers, respectively. The various control schemes and switching decision rules of the chopper devices are derived to regulate the capacitor voltages close to the reference value in this topology. The principles presented are verified by both detailed PSCAD/EMTDC simulation and experimental investigations for a five-level inverter.

II. DCMLI AND CONVENTIONAL CHOPPER CONFIGURATIONS

A single-phase five-level DCMLI is considered here, and its schematic is shown in Fig. 1(a). Two similar additional phase legs connected to the same dc bus would be required for a three-phase inverter. The dc link consists of four capacitors $(C_{d1}-C_{d4})$ with a nominal voltage of $V_{\rm dc}/4$ across each. The voltage stress across each switching device is limited to $V_{\rm dc}/4$ through the clamping diodes (D_1-D_{31}). Table I lists the inverter output voltage levels possible with the neutral point n taken as a reference. State condition 1 means that the switch is on, and 0 means that the switch is off. The other structural and operational details of the inverter can be found in [1]–[4] and [22].

As stated earlier, the dc capacitors in DCMLI suffer from voltage imbalance as the currents i_2 and i_4 have nonzero average values [Fig. 1(a)] under most of the practical conditions [4]–[21]. To prevent this, a chopper circuit like that shown in Fig. 1(b) is used conventionally [8]–[16], [23]–[25]. In this figure, the inverter circuit [Fig. 1(a)] is not shown but assumed to be connected to the chopper. The resistances R_1 and R_2 in Fig. 1(b) represent the winding resistances of the corresponding inductors. Using this circuit, the capacitor voltages are controlled within a band by transferring the extra energy from the overcharged capacitor to an inductor and then transferring it back from the inductor to the undercharged capacitor. This chopper consists of two parts. In the upper part, L_1 is used to exchange the energy between C_{d1} and C_{d2} using S_{C1}, S_{C2}, D_{C1}, and D_{C2}, while in the lower part, L_2 exchanges the energy between C_{d3} and C_{d4} using S_{C3}, S_{C4}, D_{C3}, and D_{C4} [Fig. 1(b)]. By using this circuit, it is possible to transfer the charge both from C_{d2} (C_{d3}) to C_{d1} (C_{d4}) or from C_{d1} (C_{d4}) to C_{d2} (C_{d3}). However, in a steady-state operation of DCMLI, the voltages of C_{d1} and C_{d4} always tend to increase while those of C_{d2} and C_{d3} tend to decrease [1]–[3], [8]–[18], [23]–[38].

There are many schemes available in the literature for controlling the chopper in Fig. 1(b) [8]–[15], [28]. The easiest approach is single-pulse control in which a band is set across the reference capacitor voltage, so that, if a capacitor voltage comes out of this band, the corresponding chopper operation is initiated. This implies that, when the capacitor voltages are within the defined bands, the switches $S_{C1}-S_{C4}$ in Fig. 1(b) remain open. Note that two independent chopper controllers are used to control the capacitors C_{d1} and C_{d2} and C_{d3} and C_{d4}, respectively. The detailed operating principles of this chopper and different control schemes can be found in [8]–[16], [22], and [23].

III. FLYING-CAPACITOR-BASED CHOPPER CIRCUIT

In the conventional chopper in Fig. 1(b), the semiconductor devices are subjected to half of the net dc-link voltage, when not conducting. Therefore, these devices need to be at least of twice the voltage rating compared with those of the main devices in the five-level inverter circuit. Similarly, for higher level inverters, the ratio of the required voltage rating of chopper semiconductor devices to that of the inverter main devices correspondingly increases. This higher voltage rating requirement of the chopper devices contradicts with one of the main motives of using a multilevel inverter, which states that, in a multilevel inverter, smaller rating devices are used to produce a correspondingly higher voltage output. Therefore, it can be said that, by using the conventional chopper, the advantages of a multilevel inverter are not fully exploited as the higher rating devices are still required. A possible solution is to use a series connection of low-rating devices acting as a single switch. However, in this case, the synchronization of the switching is very difficult and may result in voltage unbalance between the devices. Large snubber circuit parameters are also required to compensate for transient voltage imbalance. More switching losses may be incurred with a relatively longer switching time to achieve static voltage balancing. Therefore, this solution is not preferred for many applications [4], [39], [40].

Another possibility is to use a multilevel structure of the chopper that consists of a commutation cell using series-connected semiconductors with clamping circuits ensuring the voltage sharing across the blocking switches. The multilevel technique solves the problems of static and dynamic sharing of

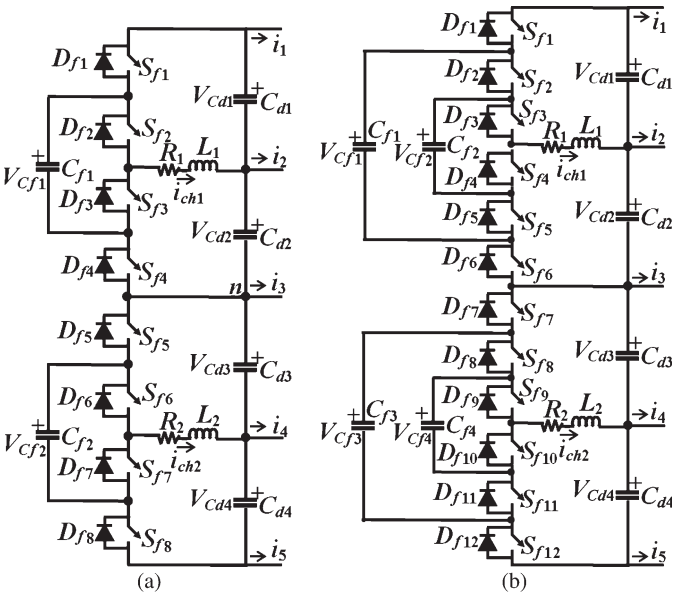

Fig. 2. (a) Three-level and (b) four-level flying-capacitor-based chopper circuit for a five-level diode-clamped inverter.

the voltage and limits the dv/dt to standard levels [1]–[4], [39], [40]. In this paper, a new flying-capacitor-based chopper circuit for dc capacitor voltage equalization in a DCMLI is proposed. This particular multilevel chopper structure is considered because it offers many advantages in terms of the regular chopper operation in the same manner as obtained with the conventional chopper, as well as its unique feature to support the dc-link capacitors in case of transient or supply disturbances. It also possesses most of the advantages of the multilevel structure configuration.

In Fig. 2, the schematics of the three-level [Fig. 2(a)] and four-level [Fig. 2(b)] flying-capacitor chopper circuits are shown. Again, for clarity, only the capacitors and corresponding chopper circuits are shown while the inverter [Fig. 1(a)] is assumed to be present. Similar to those in Fig. 1(b), the chopper circuits in Fig. 2 consist of two identical and separate sets of circuits to equalize $v_{\rm Cd1}$ and $v_{\rm Cd2}$ and $v_{\rm Cd3}$ and $v_{\rm Cd4}$, respectively. The three-level chopper circuit in Fig. 2(a) requires a total of four power switches as compared with only two in Fig. 1(b) for each set. It also requires a capacitor, called flying capacitor [C_{f1}, as shown in the upper set in Fig. 2(a)], to clamp the voltage stress across each corresponding power semiconductor device at $V_{\rm dc}/4$, where $V_{\rm dc}$ is the total dc-link voltage. It is evident that the three-level chopper circuit in Fig. 2(a) resembles that of a single-leg three-level flying-capacitor inverter. Similarly, the four-level chopper circuit in Fig. 2(b) resembles that of a single-leg four-level flying-capacitor inverter [1]–[3]. In a similar manner, an n-level chopper circuit can be represented, resembling in structure an n-level single-phase flying-capacitor inverter. Therefore, the chopper circuits in Fig. 2(a) and (b) are named as three-level and four-level chopper circuits, respectively. The higher level chopper circuits may also be used but at the cost of an increase in the number of semiconductor devices and capacitors.

If the flying capacitors are ignored in the chopper circuits and $v_{\rm Cd1}$ increases beyond the set limit, the switches S_{f1} and S_{f2} in Fig. 2(a) and S_{f1}, S_{f2}, and S_{f3} in Fig. 2(b) are closed together in a similar manner as S_{C1} in Fig. 1(b) to transfer the extra energy from C_{d1} to L_1. After this process is completed, D_{f1} and D_{f2} in Fig. 2(a) and D_{f1}, D_{f2}, and D_{f3} in Fig. 2(b) are forward biased in a similar manner as D_{C1} in Fig. 1(b) to transfer the energy stored in L_1 to C_{d2}. A similar action is performed in lower sets of the chopper circuits. To limit the voltage stress across the chopper power devices to $V_{\rm dc}/4$, it is required to maintain $v_{\rm Cf1}$ [Fig. 2(a)] at $V_{\rm dc}/4$. Similarly, $v_{\rm Cf1}$ is required to be maintained at $V_{\rm dc}/6$ and $v_{\rm Cf2}$ at $V_{\rm dc}/3$ to limit the voltage stress across the chopper power devices to $V_{\rm dc}/6$ in Fig. 2(b). Similar definitions may be set for the higher level chopper circuits.

A. Capacitor Voltage Balancing Using Three-Level Flying-Capacitor-Based Chopper

The balancing of the flying-capacitor voltages at their respective reference values is the primary requirement to keep the switching device voltage stresses limited. By doing so, the chopper can also be able to perform other important functions detailed later. A control methodology with reference to the upper set of the three-level chopper in Fig. 2(a) is presented as follows.

The reference of $v_{\rm Cf1}$ in Fig. 2(a) is set at $V_{\rm dc}/4$. A hysteresis band is placed around this reference so that, when $v_{\rm Cf1}$ increases beyond the upper limit of the band, discharging of C_{f1} is required, while its charging is required when $v_{\rm Cf1}$ falls below the lower limit of the band. The chopper operation can be divided into two regions: regions (A) and (B). In region (A), the process of equalization of $v_{\rm Cd1}$ ($v_{\rm Cd3}$) with $v_{\rm Cd2}$ ($v_{\rm Cd4}$) takes place. This region of chopper operation is initiated when the dc-link capacitor voltages increase and decrease beyond their allotted band limits. In region (B), all the dc-link capacitor voltages are within their allotted limits, and therefore, no further action to equalize the dc-link capacitor voltages is required. Region (B) of chopper operation takes place following region (A) of chopper operation, i.e., when the dc-link capacitor voltages get equalized and the chopper current is negligible. In the proposed chopper circuits in Fig. 2, the control over $v_{\rm Cf1}$ is achieved during these two operating regions of the chopper by utilizing different switching combinations to either charge or discharge C_{f1}, while the main function of the chopper, i.e., to equalize $v_{\rm Cd1}$ and $v_{\rm Cd2}$, remains unaffected.

It should be noted that, in the normal operation of the three-level chopper, S_{f1} and S_{f2} act together to transfer energy from C_{d1} to L_1, and D_{f3} and D_{f4} act together to force the energy from L_1 to C_{d2}. Therefore, ideally, there should not be any change in $v_{\rm Cf1}$, as in the normal chopper operation, the energy transfer paths do not include C_{f1}. However, due to snubber resistances, small switching transients, asymmetric device behaviors, and other disturbances, flying-capacitor voltages may deviate from their reference value. In that case, the control scheme presented here is employed to regulate the capacitor voltages near to their references. It is therefore always necessary to keep on checking the flying-capacitor voltages against their reference.

In Table II, the possible switching states for the upper half of the chopper circuit in Fig. 2(a) are listed. The symbols S_{f1}/D_{f1}

TABLE II
SWITCHING SCHEME FOR THREE-LEVEL CHOPPER

State no.	C_{f1}	S_{f1}/D_{f1}	S_{f2}/D_{f2}	S_{f3}/D_{f3}	S_{f4}/D_{f4}	i_{ch1}	*Energy transfer*
1	NC	1	1	0	0	$i_{ch1} > 0$	C_{d1} *to* L_1
						$i_{ch1} < 0$	L_1 *to* C_{d1}
2	NC	0	0	1	1	$i_{ch1} < 0$	C_{d2} *to* L_1
						$i_{ch1} > 0$	L_1 *to* C_{d2}
3	NC	0	0	0	0	$i_{ch1} < 0$	L_1 *to* C_{d1}
						$i_{ch1} > 0$	L_1 *to* C_{d2} (through antiparallel diodes)
4a	+	1	0	1	0	$i_{ch1} > 0$	C_{d1} *to* L_1 *for* $v_{Cd1} > v_{Cf1}$
4b	−					$i_{ch1} < 0$	C_{f1} *to* L_1 *for* $v_{Cd1} > v_{Cf1}$
5a	+	0	1	0	1	$i_{ch1} < 0$	C_{d2} *to* L_1 *for* $v_{Cd2} > v_{Cf1}$
5b	−					$i_{ch1} > 0$	C_{f1} *to* L_1 *for* $v_{Cd2} > v_{Cf1}$

to S_{f4}/D_{f4} in Table II are binary variables, which represent the switch states of the corresponding devices in Fig. 2(a) and attain the values 1 and 0 if the corresponding switch or the antiparallel diode are conducting and not conducting, respectively. The charging state of the flying capacitor is indicated by $+$ and discharging by $-$, and "NC" indicates no change in the capacitor state. The possible number of switches conducting at a certain instant in the three-level chopper circuit is limited to two out of four. The simultaneous closing of any of the three switches either results in a short-circuiting of C_{f1} or equivalently forces C_{f1} in parallel with C_{d1} and C_{d2} in series. These are the undesired conditions as no control over the chopper operation remains. Furthermore, out of the six possible combinations of any of the two switches in the three-level chopper circuit, only four are useful. The combination S_{f2}/D_{f2}, S_{f3}/D_{f3} is not allowed as it results in shorting of C_{f1}, and S_{f1}/D_{f1}, S_{f4}/D_{f4} is not allowed as it causes C_{f1} in parallel with C_{d1} and C_{d2} in series. The other four useful switching combinations of the two switches are listed in Table II. By adding these states with the state of all the main switches off (state number 3), it can be seen from Table II that there are seven possible states of the energy transfer among the capacitors C_{d1}, C_{d2}, and C_{f1}. A similar table is valid for the lower chopper set with switches S_{f5}/D_{f5}, S_{f6}/D_{f6}, S_{f7}/D_{f7}, and S_{f8}/D_{f8} and capacitors C_{d3}, C_{d4}, and C_{f2} [Fig. 2(b)].

It can be seen from Table II that the energy can be transferred from C_{d1} or C_{d2} to L_1 without affecting C_{f1} using states 1 and 2. Alternately, C_{f1} can be charged using states 4a and 5a during the same energy transfer from C_{d1} or C_{d2} to L_1. Furthermore, C_{f1} can be discharged to L_1 using the state sequence 4b, 5b if its voltage is greater than v_{Cd1} or v_{Cd2}. The state sequences 1, 3 and 2, 3 leave C_{f1} unchanged while transferring energy between C_{d1} and C_{d2}. The state sequences 4a, 3 and 5a, 3 transfer energy between C_{d1} and C_{d2} with the charging of C_{f1}. The state sequences 4b, 3 and 5b, 3 do the same while discharging C_{f1}. Thus, energy can be transferred between C_{d1} and C_{d2} with or without charging C_{f1}. Furthermore, energy can be transferred between C_{f1} and C_{d1} or C_{f1} and C_{d2} whenever C_{f1} is charged or discharged above or below the voltages of capacitors C_{d1} or C_{d2}. Based on these state sequences and possible energy transfer paths, Table III lists the preferable state sequences and their energy transfer effects based on the desired capacitor states for the two regions of chopper operation.

Based on the aforementioned preferable state sequence, a control methodology is formulated, and its block diagram is shown in Fig. 3. To control the chopper, as shown in Fig. 3, the differences of v_{Cd1} and v_{Cd2} with $V_{\mathrm{dc}}/4$ (ΔV_{Cd1} and ΔV_{Cd2}, respectively) are sensed and compared in a three-level comparator with a band of width $\pm\Delta V_C$. The comparator outputs decide the chopper operating region as stated in Table III. If ΔV_{Cd1} is greater than ΔV_C, state 1 is selected, and it is followed by state 3. Similarly, if ΔV_{Cd2} is greater than ΔV_C, state 2 is selected followed by state 3. It is to be noted that, in these states, it is assumed that no change in v_{Cf1} is required (Table III). If both ΔV_{Cd1} and ΔV_{Cd2} are within $\pm\Delta V_C$, region (B) is selected. Another three-level comparator is used to compare the flying-capacitor voltage error ΔV_{Cf1} with the band $\pm\Delta V_{\mathrm{Cf}}$, which sets the desired state of flying capacitor in the manner stated previously. Now, a control law is designed, which senses the desired chopper region of operation and flying-capacitor voltage state to output the chopper switching signals by following the considerations listed in Table III. The functioning of the chopper is detailed as follows.

It is evident from Table III that, if ΔV_{Cf1} lies within $\pm\Delta V_{\mathrm{Cf}}$ in region (A) of the desired chopper operation, S_{f1} and S_{f2} are turned on (state 1) to transfer the energy from C_{d1} to L_1 without affecting C_{f1}. Under region (A) of chopper operation, another state is possible to transfer the energy from C_{d1} to L_1, i.e., state 4a (Table III). As indicated in Table III, this switching combination is chosen when ΔV_{Cf1} is less than $-\Delta V_{\mathrm{Cf}}$ and discharging of C_{d1} is required. The value of ΔV_{Cf} is usually taken to be less than that of ΔV_C. By doing so, it always remains possible to transfer some charge, if required, from C_{d1} to C_{f1} under region (A). Once v_{Cf1} increases to come within $V_{\mathrm{dc}}/4 \pm \Delta V_{\mathrm{Cf}}$ under region (A) by using the state sequence (4a, 3) while v_{Cd1} still remains outside $V_{\mathrm{dc}}/4 + \Delta V_C$, switch S_{f2} is again turned on so that further charging of C_{f1} stops.

Following the extra energy transfer from C_{d1} to L_1, the voltage developed in L_1 forward biases D_{f3} and D_{f4}, and state 3 of the chopper operation starts. It is also when L_1 transfers energy to a dc-link capacitor that no preferential charging or discharging of C_{f1} can take place. For example, in the aforementioned state case, D_{f3} and D_{f4} always remain forward biased until the complete transfer of energy from L_1 to C_{d2}. Following state 3, when a complete transfer of energy from L_1 to C_{d2} has taken place, both ΔV_{Cd1} and ΔV_{Cd2} are

TABLE III
PREFERABLE STATE SEQUENCES FOR THREE-LEVEL CHOPPER

Chopper operating region	*Desired capacitor states*			*Selected State Sequence*	*Resulting energy transfer*
	C_{d1}	C_{d2}	C_{f1}		
A	−	+	NC	1,3 with $i_{ch1}>0$	C_{d1} to C_{d2} with *no change* in C_{f1}
A	−	+	+	4a,3 with $i_{ch1}>0$	C_{d1} to C_{d2} with *Charging* of C_{f1}
A	−	+	−	1,3 with $i_{ch1}>0$	C_{d1} to C_{d2} with *no change* in C_{f1}
A	+	−	NC	2,3 with $i_{ch1}<0$	C_{d2} to C_{d1} with *no change* in C_{f1}
A	+	−	+	5a,3 with $i_{ch1}<0$	C_{d2} to C_{d1} with *Charging* of C_{f1}
A	+	−	−	2,3 with $i_{ch1}<0$	C_{d2} to C_{d1} with *no change* in C_{f1}
B	NC	NC	+	4a,3 with $i_{ch1}>0$	C_{d1} to C_{f1} with charging of C_{d2} (for $V_{Cd1}>V_{Cd2}$)
B	NC	NC	+	5a,3 with $i_{ch1}<0$	C_{d2} to C_{f1} with charging of C_{d1} (for $V_{Cd2}>V_{Cd1}$)
B	NC	NC	−	4b,3 with $i_{ch1}<0$	C_{f1} to C_{d1} with charging of C_{d2} (for $V_{Cd2}>V_{Cd1}$)
B	NC	NC	−	5b,3 with $i_{ch1}>0$	C_{f1} to C_{d2} with charging of C_{d1} (for $V_{Cd1}>V_{Cd2}$)

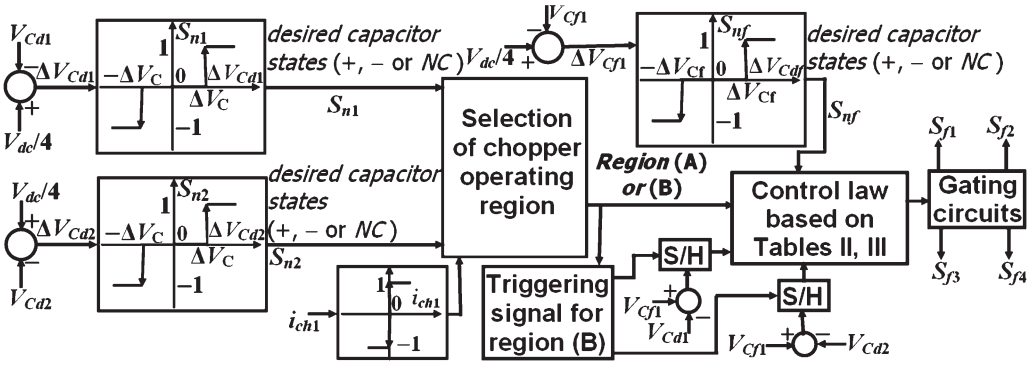

Fig. 3. Control block diagram of a three-level flying-capacitor-based chopper.

within $\pm\Delta V_C$ [region (B)] and remains for a while depending on the various factors stated earlier. In a similar manner, the other state sequences are chosen in region (A) with either no change or charging of C_{f1} as is evident from Tables II and III. It should be noted that the state sequences (2, 3) and (5a, 3) do not come into picture under normal steady-state chopper operation in region (A).

The chopper may also be operated in region (B) to regulate v_{Cf1} if required. When ΔV_{Cf1} comes out of the band $\pm\Delta V_{\mathrm{Cf}}$, the four switching sequences listed for region (B) in Table III are used to regulate v_{Cf1}. As shown in Fig. 3, the chopper operation under region (B) triggers the two sample-and-hold (S/H) circuits, which sense the differences between v_{Cf1} and v_{Cd1} and v_{Cf1} and v_{Cd2}. The control law is designed in such a way that it requires and processes the output of the two S/H circuits only when ΔV_{Cf1} is out of the limits and the chopper is in region (B). For any other condition, the S/H circuit outputs are ignored by the control law. In region (B), since v_{Cd1} and v_{Cd2} are within their limits, preference is given to v_{Cf1} so that it can be regulated without overcharging or undercharging C_{d1} and C_{d2} beyond the limits. As stated earlier, the value of ΔV_{Cf} is usually taken to be smaller than that of ΔV_C. Therefore, it could be possible to transfer the extra energy from (to) C_{f1} to (from) either C_{d1} or C_{d2} without increasing (decreasing) their voltages beyond $V_{\mathrm{dc}}/4 \pm \Delta V_C$. For this purpose, ΔV_C should be at least of double in magnitude to that of ΔV_{Cf}.

To exemplify the chopper function in region (B), let us suppose that v_{Cf1} is required to be discharged at a particular instant under region (B). The controller then checks if any or both of v_{Cd1} and v_{Cd2} are smaller than v_{Cf1} and, if so, which one is smaller between v_{Cd1} and v_{Cd2}. The capacitor with a lower voltage is selected to transfer the extra energy from C_{f1}

so that, following the energy transfer, the increased capacitor voltage remains within limits. From Table III, if v_{Cd2} is lesser than v_{Cd1} and v_{Cf1}, state 5b is chosen, and if v_{Cd1} is lesser than v_{Cd2} and v_{Cf1}, state 4b is chosen. Once v_{Cf1} comes within limits, S_{f2} and S_{f4} in state 5b and S_{f1} and S_{f3} in state 4b are turned off so that further discharging of C_{f1} stops. However, the remaining energy in L_1 forward biases D_{f3} and D_{f4} in state 5b (state sequence 5b, 3) and D_{f1} and D_{f2} in state 4b (state sequence 5b, 3) to transfer it further to C_{d2} and C_{d1}, respectively (Table III). In a similar manner, an undercharged C_{f1} prompts the controller to select the larger one between v_{Cd1} and v_{Cd2} so that it could be charged within the limits without forcing v_{Cd1} and v_{Cd2} out of the limits. The state sequence 4a, 3 is chosen to transfer energy from C_{d1} to C_{f1}, while choosing the state sequence 5a, 3 transfers energy from C_{d2} to C_{f1}. Again, once v_{Cf1} comes within limits, S_{f1} and S_{f3} after state 4a and S_{f2} and S_{f4} after state 5a are turned off so that further charging of C_{f1} stops. The stored energy in L_1, however, then forward biases D_{f3} and D_4 after state 4a and D_{f1} and D_{f2} after state 5a to transfer it to C_{d2} and C_{d1}, respectively (state 3, Table III). In this way, the flying-capacitor voltage is regulated in region (B).

It should be noted that, since under steady-state, C_{f1} is not affected by the exchange of energy between C_{d1}, C_{d2} and L_1, which is the main function of the chopper, the variation in v_{Cf1} is minimal. This minimal change in v_{Cf1} from its reference value, which may be due to the switching transients or due to losses in the devices, can be compensated using the control scheme in Fig. 3. It is also evident from Tables II and III that, since there is no state sequence available under region (A) for the discharging of C_{f1}, equal charging and discharging actions of the capacitor are not guaranteed. Therefore, in steady state, only the state sequences under region (A) are used for regulating v_{Cf1} so that an equal number of charging and discharging actions could be achieved (Table III).

Since state sequences 4a, 3 and 5a, 3 in region (A) refer to a heavy charging of C_{f1} (as v_{Cd1} or v_{Cd2} is out of the limits) as compared with the state sequences in region (B), it is used separately only under transient conditions or for the charging of C_{f1} at the start. This logical setting of the control is also strengthened from the fact that, under steady state, changes in v_{Cf1} are minimal, and the state sequences under region (B) should be sufficient enough for regulating it by properly designing ΔV_{Cf} and ΔV_C. If, due to a transient, v_{Cf1} increases by a large extent, C_{f1} cannot be discharged in the same way as it is charged under region (A), as there is no state sequence available for discharging it in this region. In that case, the state sequences under region (B) are used to discharge it in a step-by-step manner. It is however clear that the discharging of C_{f1} under region (B) will be slower compared with the charging of C_{f1} under region (A) by an equal amount. The rate of charging and discharging of C_{f1}, if its voltage is well beyond the set limit, can be set equal by charging C_{f1} also in region (A) only in the same manner as it is discharged following any amount of dip or rise in the voltage of C_{f1}. By applying the similar control scheme, the capacitor voltages v_{Cd3} and v_{Cd4} can be controlled in a similar manner in addition to have the control over v_{Cf2}.

B. Capacitor Voltage Balancing Using Four-Level Flying-Capacitor-Based Chopper

The four-level chopper in Fig. 2(b) can also be controlled in a manner similar to that of the three-level chopper discussed in the previous section. For the four-level case, the control scheme remains the same as in Fig. 3 except that, now, both the flying-capacitor states are required to be checked [v_{Cf1} and v_{Cf2} in the upper chopper set in Fig. 2(b)]. In a manner similar to that in the three-level chopper, three switches are to be closed at a time to complete a path in the four-level chopper. Out of 20 possible combinations of any of the three switches (out of six), only eight combinations are useful. The remaining 12 combinations either cause short-circuiting of the flying capacitors or put C_{f1} in parallel with C_{f2} or with C_{d1} and C_{d2} in series. It can be seen from Fig. 2(b) that the switch pairs (S_{f3}, S_{f4}), (S_{f1}, S_{f6}), and (S_{f2}, S_{f5}) should not be closed together. The eight useful switching states and corresponding energy transfer paths are listed in Table IV. In this table, an additional state (state number 3) with all the switches open is also listed in which the inductor energy is transferred to a dc-link capacitor through the antiparallel diodes. A similar table exists for the lower chopper circuit set with switches S_{f7}/D_{f7}, S_{f8}/D_{f8}, S_{f9}/D_{f9}, S_{f10}/D_{f10}, S_{f11}/D_{f11}, and S_{f12}/D_{f12} and capacitors C_{f3} and C_{f4} [Fig. 2(b)].

It can be seen from Table IV that the energy can be transferred from C_{d1} or C_{d2} to L_1 without affecting the two flying capacitors (state sequences 1, 2). Alternately, C_{f2} can be charged using state sequences (4a, 3) or (6a, 3) during the similar energy transfer from C_{d1} or C_{d2} to L_1 if its voltage becomes lower than its reference voltage value of $V_{\mathrm{dc}}/6$. The reference voltage of C_{f1} is $V_{\mathrm{dc}}/3$, which is greater than the reference voltages of C_{d1} and C_{d2}. Therefore, it is not directly possible to charge C_{f1} without involving C_{f2}, which is also evident from Table IV. The states 5a and 7a do offer charging possibilities of C_{f1} but only when v_{Cf1} is lesser than either v_{Cd1} or v_{Cd2}. These states can be used only under transient conditions or for the charging of C_{f1} from its sufficiently low voltage value until $V_{\mathrm{dc}}/4$. To charge it further to its reference value of $V_{\mathrm{dc}}/3$, states 8a and 9a can be used, which, however, involve simultaneous discharging of C_{f2} as well. The states 4b and 6b are not used under steady state to discharge C_{f2} as it requires v_{Cf2} to be greater than either v_{Cd1} or v_{Cd2}. However, it may be used under transient conditions involving a large drop in v_{Cd1} and v_{Cd2}. Therefore, if, under normal operating conditions, v_{Cf2} increases above its reference, states 8a or 9a can be used to discharge it and, simultaneously, to charge C_{f1}. These states will then be followed by 5b or 7b to force v_{Cf1} back toward its reference. Therefore, it can be concluded that it is possible to charge C_{f2} and discharge C_{f1} individually while performing the balancing of v_{Cd1} and v_{Cd2}. The simultaneous charging of C_{f1} and discharging of C_{f2} is also possible along with the balancing of v_{Cd1} and v_{Cd2}. However, to have only C_{f1} charged and C_{f2} discharged, two-step processes, as detailed earlier, are required. These two-step processes of balancing the two flying capacitors are repeated until both v_{Cf1} and v_{Cf2} fall within limit. Therefore, as compared with the three-level chopper operation, the four-level chopper operation is relatively

TABLE IV
SWITCHING SCHEME FOR FOUR-LEVEL CHOPPER

State no.	C_{f1}	C_{f2}	S_{f1}/D_{f1}	S_{f2}/D_{f2}	S_{f3}/D_{f3}	S_{f4}/D_{f4}	S_{f5}/D_{f5}	S_{f6}/D_{f6}	i_{ch1}	Energy transfer
1	NC	NC	1	1	1	0	0	0	$i_{ch1}>0$	C_{d1} to L_1
									$i_{ch1}<0$	L_1 to C_{d1}
2	NC	NC	0	0	0	1	1	1	$i_{ch1}<0$	C_{d2} to L_1
									$i_{ch1}>0$	L_1 to C_{d2}
3	NC	NC	0	0	0	0	0	0	$i_{ch1}<0$	L_1 to C_{d1}
									$i_{ch1}>0$	L_1 to C_{d2} (through antiparallel diodes)
4a	NC	+	1	1	0	1	0	0	$i_{ch1}>0$	C_{d1} to L_1 for $v_{Cd1}>v_{Cf2}$
4b	NC	–							$i_{ch1}<0$	C_{f2} to L_1 for $v_{Cd1}<v_{Cf2}$
5a	+	NC	1	0	0	1	1	0	$i_{ch1}>0$	C_{d1} to L_1 for $v_{Cd1}>v_{Cf1}$
5b	–	NC							$i_{ch1}<0$	C_{f1} to L_1 for $v_{Cd1}<v_{Cf1}$
6a	NC	+	0	0	1	0	1	1	$i_{ch1}>0$	C_{d2} to L_1 for $v_{Cd2}>v_{Cf2}$
6b	NC	–							$i_{ch1}<0$	C_{f2} to L_1 for $v_{Cd2}<v_{Cf2}$
7a	+	NC	0	1	1	0	0	1	$i_{ch1}>0$	C_{d2} to L_1 for $v_{Cd2}>v_{Cf1}$
7b	–	NC							$i_{ch1}<0$	C_{f1} to L_1 for $v_{Cd2}<v_{Cf1}$
8a	+	–	1	0	1	0	1	0	$i_{ch1}>0$	C_{d1} to L_1 for $v_{Cd1}>v_{Cf1}-v_{Cf2}$
8b	–	+							$i_{ch1}<0$	C_{f1} to L_1 for $v_{Cf1}-v_{Cf2}>v_{Cd1}$
9a	+	–	0	1	0	1	0	1	$i_{ch1}<0$	C_{d2} to L_1 for $v_{Cd2}>v_{Cf1}-v_{Cf2}$
9b	–	+							$i_{ch1}>0$	C_{f1} to L_1 for $v_{Cf1}-v_{Cf2}>v_{Cd2}$

TABLE V
PREFERABLE STATE SEQUENCES FOR FOUR-LEVEL CHOPPER

Chopper operating region	Desired capacitor states				Selected State Sequence	Resulting energy transfer
	C_{d1}	C_{d2}	C_{f1}	C_{f2}		
A	–	+	NC	NC	1,3	C_{d1} to C_{d2}, *No Change* in C_{f1}, C_{f2}
A	–	+	NC	+	4a, 3	C_{d1} to C_{d2}, *Charging* of C_{f2}, *No Change* in C_{f1}
A	–	+	+	–	8a, 3	C_{d1} to C_{d2}, *Charging* of C_{f1}, *Discharging* of C_{f2}
A	+	–	NC	NC	2, 3	C_{d2} to C_{d1}, *No Change* in C_{f1}, C_{f2}
A	+	–	NC	+	6a, 3	C_{d2} to C_{d1}, *Charging* of C_{f2}, *No Change* in C_{f1}
A	+	–	+	–	9a, 3	C_{d2} to C_{d1}, *Charging* of C_{f1}, *Discharging* of C_{f2}
B	NC	NC	NC	+	4a, 3	C_{d1} to C_{f2}, charging of C_{d2} (for $V_{Cd1}>V_{Cd2}$)
B	NC	NC	NC	+	6a, 3	C_{d2} to C_{f2}, charging of C_{d1} (for $V_{Cd2}>V_{Cd1}$)
B	NC	NC	–	NC	5b, 3	C_{f1} to C_{d1}, charging of C_{d2} (for $V_{Cd2}>V_{Cd1}$)
B	NC	NC	–	NC	7b, 3	C_{f1} to C_{d2}, charging of C_{d1} (for $V_{Cd1}>V_{Cd2}$)
B	NC	NC	+	–	8a, 3	*Charging* of C_{f1}, *Discharging* of C_{f2} using C_{d1}
B	NC	NC	+	–	9a, 3	*Charging* of C_{f1}, *Discharging* of C_{f2} using C_{d2}

slower. Based on these state sequences and possible energy transfer paths, Table V lists the preferable state sequences and their energy transfer effects based on the desired capacitor states in the two regions of chopper operation.

In a manner similar to the three-level chopper, the different possible state sequences are allotted under a different region of the four-level chopper operation as is evident from Table V. In Table V, not all the desired states of C_{f1} and C_{f2} are listed under the two regions of chopper operation. This is because, as stated earlier, charging C_{f1} only and discharging C_{f2} only is not possible. To achieve charging in C_{f1} or discharging in C_{f2}, the two-step process, as detailed previously, is employed.

It is observed from Table IV and the afore-presented discussion that the flying-capacitor voltage balancing performance gets slower with increasing the chopper levels. Therefore, the three-level chopper in Fig. 2(a) seems most suitable for the five-level inverter as it uses the devices of same rating as of the inverter main devices, and also, there is no delay involved in flying-capacitor voltage balancing.

C. Features of the Flying-Capacitor-Based Chopper Circuit

Compared with the conventional chopper-based solution in Fig. 1(b), the proposed flying-capacitor-based chopper circuit offers a number of advantages, which are described as follows.

The flying-capacitor-based chopper has a unique advantage that it may be used for ride-through voltage support in emergencies. This can be achieved since the chopper has inherent additional capacitors (flying capacitors), which can store energy. It is evident from Tables III and V that the flying capacitors can feed energy to the dc-link capacitors when their voltages fall below a set value. This could be a case in the events of voltage sags or load swings experienced at the utility interface connection, dc bus fault, or other electric power disturbances [41]. The extent of ride-through enhancement depends on the capacitor size and chopper inductors. It is also to be noted that the ride-through enhancement extent increases with the number of chopper levels.

The proposed circuit-supported DCMLI system is expected to be more reliable compared with the conventional chopper-supported system. If a component fails in the flying-capacitor-based chopper, most of the time, it will still be functional, albeit at a reduced efficiency. However, in a conventional chopper circuit, a device failure will result in a complete shutdown of the chopper operation. This can be analyzed from Fig. 1(b) that, supposing S_{C1} fails, this will block the energy transfer from the overcharged C_{d1} to L_1. This, in effect, will result in complete unbalanced capacitor voltages. Let us now consider the three-level chopper circuit of Fig. 2(a). It is first assumed that S_{f2} fails. This, however, will not completely block the energy transfer possibility from C_{d1} to L_1 as another energy transfer path is available through C_{f1} and S_{f3}, which is evident from Table II. Next, it is supposed that S_{f1} fails. Then, it will not be possible to transfer the energy from C_{d1} to L_1 as both the energy transfer paths from C_{d1} to L_1 involve S_{f1} (Table II). However, since C_{f1} normally holds a voltage similar to those of the dc-link capacitors $(C_{d1}-C_{d4})$, the energy-transfer possibility still remains from C_{f1} to C_{d2}, as is evident from Table II. Therefore, although, in this case, v_{Cd1} will continue to increase, v_{Cd2} may be momentarily controlled by C_{f1}. For the lower chopper switches S_{f3} and S_{f4}, a similar situation can be observed. Similarly, the lower chopper set will experience the same situation. Therefore, it can be concluded that, when there is a fault on one of the chopper's semiconductor switching devices, the proposed flying-capacitor-based chopper circuit may still function, although at a reduced efficiency. The chopper efficiency under a fault case will improve for a higher level flying-capacitor-based chopper, like the one shown in Fig. 2(b), as it possesses more redundant switch combinations for the corresponding energy transfers for balancing the capacitor voltages.

It is evident from Tables III and V that there are multiple switch combinations available for the different energy transfer actions for dc capacitor voltage balancing. This feature can be utilized to operate the chopper with lower individual switching frequencies, resulting in lower losses. The reduction of semiconductor losses will reduce the average temperature at the components and thus decrease the failure rate. The redundancy in switching combination can be utilized to reduce the chopper inductor volume as well.

Apart from the aforementioned advantages, since the flying-capacitor-based chopper has a multilevel configuration, it is expected to have more advantages like reduced electromagnetic compatibility problems and lower acoustic noise due to reduced dv/dt, limited voltage transients, etc. [1]–[5].

Even though the proposed flying-capacitor-based chopper circuit has several advantages as described previously, its structure and control are more complex compared with those of a conventional chopper. The overall cost of this configuration may not be higher because it can have lower losses, reduced inductor size, and lower rated devices as described earlier.

IV. Simulation Results

To exemplify the functioning and control of the flying-capacitor-based chopper circuits in Fig. 2, simulation studies are performed on a single-phase five-level DCMLI. The phase disposition modulation strategy (described in [1]–[3] and [42]–[44]) is considered with an amplitude modulation index $(m_a) = 0.8$ and a frequency modulation index $(m_f) = 21$. The inverter is supplying an RL load of $R = 35\ \Omega$ and $L = 30$ mH. The dc-link voltage is 80 V, and the inverter devices are assumed to be nearly ideal. The chopper inductors are taken as $L_1 = L_2 = 15$ mH and $\Delta = 2$ V (Δ is the hysteresis band set across $V_{\mathrm{Cdr}} = 20$ V). The flying capacitors are taken as $C_{f1} = C_{f2} = 5000\ \mu$F for the three-level chopper [Fig. 2(a)]. For the four-level chopper [Fig. 2(b)], the capacitors are $C_{f1} = C_{f3} = 3750\ \mu$F and $C_{f2} = C_{f4} = 7500\ \mu$F. After first selecting the capacitance values for the three-level chopper, the four-level chopper capacitance values are accordingly taken in proportion to their corresponding reference voltage values. The flying capacitors are purposely taken to be larger than those of dc-link capacitors $(C_{d1} - C_{d4} = 500\ \mu\mathrm{F})$ so that their voltage variations remain small. This allows the selection of a smaller band size for their voltage regulation as compared with those for the dc-link capacitors. Another important advantage of using large flying capacitors is that they hold larger energy as compared with those in the dc-link capacitors, which makes it possible to transfer energy from the flying capacitor to the dc-link capacitors. As discussed earlier, ΔV_{Cf} should be taken at most half of ΔV_C. Therefore, ΔV_{Cf} is taken to be 1% of the reference value of the corresponding flying-capacitor voltage as compared with $\Delta V_C = 10\%$ of the reference value of the dc-link capacitor voltage.

With the inverter and chopper parameters given previously, a simulation study is performed, first, using the three-level chopper [Fig. 2(a)]. The flying capacitors are kept uncharged initially, which is an abnormal operating condition since the flying capacitors would normally be precharged to their nominal values to prevent destruction of the switching devices. Thus, the investigation of this type of transient response is the "worst" case unbalanced condition. This situation is purposely considered so as to show the flying capacitors charging using the state sequence (4a, 3) under region (A) of chopper operation (Table III). The controller is designed to continuously check the capacitor voltages and apply state sequence (4a, 3) whenever v_{Cd1} (v_{Cd4}) crosses the upper defined limit during the charging process of C_{f1} (C_{f2}). State sequence (4a, 3) is applied until v_{Cd1} reaches near $V_{\mathrm{dc}/4}$. This action is repeated until the complete charging of flying capacitors is achieved, and when their voltages reach within their limits of $V_{\mathrm{dc}}/4 \pm \Delta V_{\mathrm{Cf}}$, region (B)

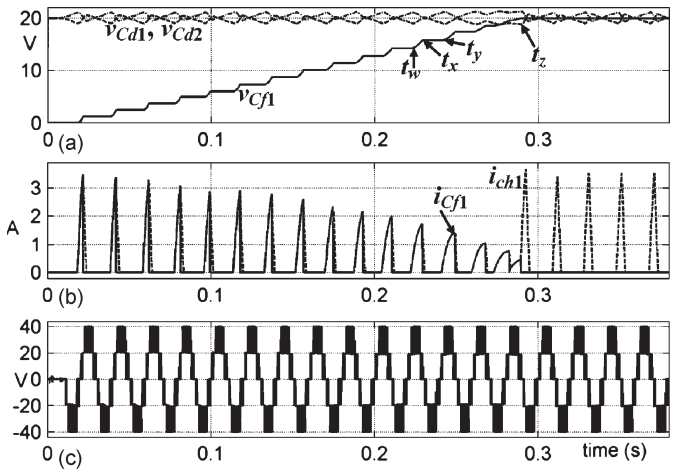

Fig. 4. Charging of flying capacitor in the three-level chopper. (a) DC-link and flying-capacitor voltage, (b) inductor current, and (c) inverter output voltage.

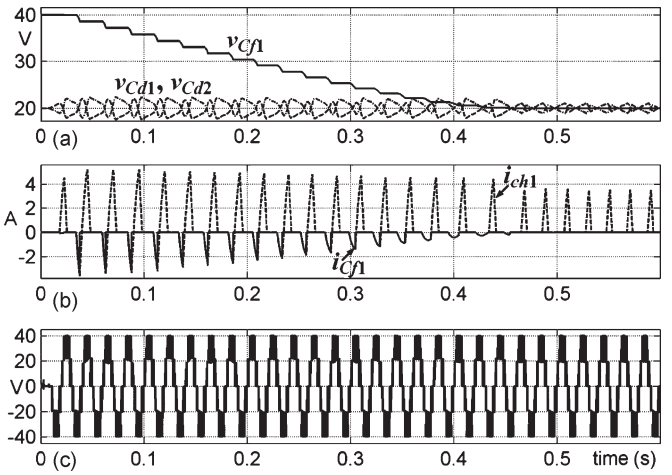

Fig. 5. Discharging of flying capacitor in the three-level chopper. (a) DC-link and flying-capacitor voltage, (b) inductor current, and (c) inverter output voltage.

switch states are applied while $C_{d1}-C_{d4}$ are controlled using the single-pulse control as described earlier.

The simulation results are shown in Fig. 4. The charging of C_{f1} to its desired value is evident from Fig. 4(a). The dc-link capacitor voltages are also equalized in this process. In Fig. 4(a), at t_w, $v_{\rm Cd1}$ crosses its upper boundary, and therefore, the controller selects state number 4a so that C_{d1} discharges to C_{f1} and L_1. This can be observed during t_w and t_x as $v_{\rm Cf1}$ and $i_{\rm ch1}$ (same as $i_{\rm Cf1}$ until t_x) build. Once $v_{\rm Cd1}$ reaches near $V_{\rm dc}/4$ (at t_x) (state number 3), S_{f1} and S_{f3} are turned off so that the energy stored in L_1 charges C_{d2} through D_{f3} and D_{f4} (until t_y). It can be seen that, between time instants t_x and t_y, $v_{\rm Cf1}$ remains constant as no current is flowing through it. This is also evident from Fig. 4(b) as $i_{\rm Cf1}$ dies out quickly (e.g., at t_y) while $i_{\rm ch1}$ takes a while to die out as it flows through D_{f3} and D_{f4} following t_y. The energy required by C_{f1} in charging it by, for example, $\Delta_{\rm Cf}$ from V_1 during the charging process t_w to t_x is given by

$$\Delta E_{\rm Cf1} = \frac{1}{2}C_f(V_1+\Delta_{\rm Cf})^2 - \frac{1}{2}C_f V_1^2. \tag{1}$$

By neglecting the term $(1/2)C_f\Delta_{\rm Cf}^2$ in (1) for a sufficiently small $\Delta_{\rm Cf}$ compared with V_1, the resulting equation becomes

$$\Delta E_{\rm Cf1} = C_f V_1 \Delta_{\rm Cf}. \tag{2}$$

It is evident from (2) that, as V_1 increases, the energy required by C_{f1} increases as well. As a result, for larger values of V_1, the resulting energy transferred to L_1 from C_{d1} may not be sufficient to raise $v_{\rm Cd2}$ to its reference. This can also be observed from Fig. 4(a) and (b) where, for large flying-capacitor voltages during the charging process, the dc-link capacitor voltage equalization is not that good, and also, the inductor current is reduced. Once $v_{\rm Cf1}$ reaches within $V_{\rm dc}/4 \pm \Delta V_{\rm Cf}$ [at t_z, Fig. 4(a)], region (B) state sequences start operating while dc-link capacitor voltages are equalized using the single-pulse control. It can be seen that, following t_z, $i_{\rm Cf1}$ is negligible as compared with $i_{\rm ch1}$, and therefore, $v_{\rm Cd1}$ and $v_{\rm Cd2}$ are very well equalized. The corresponding five-level inverter output voltage is shown in Fig. 4(c), which is undisturbed and has the expected waveform. This simulation result confirms that the three-level chopper is able to equalize dc-link capacitor voltages as well as to charge up and regulate the flying-capacitor voltage around its reference.

The afore-presented simulation study illustrates the charging of a flying capacitor from an initial value to its target reference. As discussed in the previous section, the flying capacitor can be discharged as well using the states 4b and 5b (Table II). It is evident from Table III that C_{f1} can transfer its energy to one of C_{d1} or C_{d2} only in region (B). To illustrate the discharging of C_{f1}, another simulation study is performed with the system conditions remaining the same except the initial value of $v_{\rm Cf1}$ which is set at 40 V. The resulting curves are shown in Fig. 5. As C_{f1} exchanges energy with either C_{d1} or C_{d2} only in region (B) when both $v_{\rm Cd1}$ and $v_{\rm Cd2}$ are within limits, the large exchange of energy does not take place. This results in slower discharging of C_{f1}, which can also be observed by comparing the charging of C_{f1} in Fig. 4(a) and the discharging of C_{f1} in Fig. 5(a). It is evident from these figures that it takes almost 0.11 s more to force $v_{\rm Cf1}$ to its reference in Fig. 5(a) as compared with that in Fig. 4(a), when the initial imbalance extent was the same in both cases. However, it is clear from Fig. 5 that the proposed chopper with its control scheme is able to regulate $v_{\rm Cf1}$ even under large disturbances. Furthermore, from Fig. 5, under region (A) while using the state sequence (1, 3), $v_{\rm Cf1}$ remains constant and discharges to either C_{d1} or C_{d2} following state number 3. The corresponding inductor and flying-capacitor currents and inverter output voltages are shown in Fig. 5(b) and (c), respectively. These waveforms can be analyzed in a manner similar to that of the previously presented simulation results.

In a similar manner as aforementioned, the four-level chopper in Fig. 2(b) is also controlled, and the corresponding simulation results are shown in Fig. 6. It is evident from Fig. 6(a) that the dc-link capacitor and flying-capacitor voltages are effectively regulated around their references in steady state and that, also, the chopper charges up the flying capacitors close to their references in a manner detailed as aforementioned. During the charging process, as both the flying capacitors [C_{f1} and C_{f2} in the upper chopper set in Fig. 2(b)] are uncharged at the

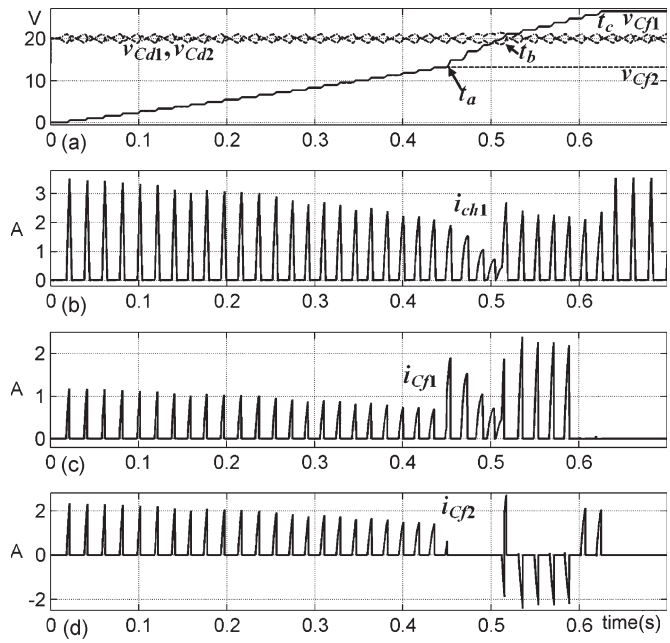

Fig. 6. Four-level chopper simulation results. (a) DC-link and flying-capacitor voltage, (b) inductor current, (c) current in C_{f1}, and (d) current in C_{f2}.

beginning, state number 4a (Table V) is applied to first charge C_{f2}. In this state, S_{f1} and S_{f2} are switched on, which forward biases D_{f4} as $v_{\rm Cf2}$ is less than $v_{\rm Cd1}$. However, since $v_{\rm Cf1}$ is also less than $v_{\rm Cd1}$ at the beginning, another current loop forms, which charges C_{f1} through S_{f1} and forward-biased diodes D_{f4} and D_{f5}. Therefore, both C_{f1} and C_{f2} get charged in parallel in the beginning from C_{d1} until $v_{\rm Cf2}$ reaches its reference. It is also evident from Fig. 6(c) and (d) where positive values of $i_{\rm Cf1}$ and $i_{\rm Cf2}$ (currents through C_{f1} and C_{f2}, respectively) represent the charging of the respective capacitors. It is to be noted that state number 5a could have also been used to charge up C_{f1} first with no change in C_{f2}. However, the building of voltage in only C_{f1} may result in higher stresses on few devices. Therefore, the state number 4a is purposely chosen in the beginning to simultaneously charge C_{f1} and C_{f2}. Following t_a when $v_{\rm Cf2}$ has reached within $V_{\rm dc}/6 \pm \Delta V_{\rm Cf2}$, only C_{f1} is required to be charged further. Since $v_{\rm Cf1}$ is still less than $v_{\rm Cd1}$ and $v_{\rm Cd2}$, state 5a or 7a is used to charge it up. Since these states charge only C_{f1}, as opposed to state 4a in which both C_{f1} and C_{f2} were charged simultaneously, the rapid charging of C_{f1} is expected.

It is clear from Fig. 6(a) that, following t_a, the charging of C_{f1} is rapid. Furthermore, between t_a and t_b, $i_{\rm Cf2}$ is zero, causing no change in $v_{\rm Cf2}$, and $i_{\rm Cf1}$ is positive, representing the charging of C_{f1}. At t_b, $v_{\rm Cf1}$ reaches a value where it becomes more than both $v_{\rm Cd1}$ and $v_{\rm Cd2}$ and therefore cannot be charged further using state 5a or 7a. As detailed earlier, state 8b or 9b is used to charge C_{f1} once its voltage becomes greater than those of C_{d1} and C_{d2}. These states, however, cause undesirable discharging of C_{f2}. Therefore, the state 4a or 6a is again selected to force C_{f2} back to within its voltage limits. It is charged repeatedly using state 4a or 6a until it is again within the allotted limits, and then, state 8b or 9b is again applied to charge C_{f1}. These actions are repeated until both $v_{\rm Cf1}$ and $v_{\rm Cf2}$ are within their respective allotted bands. Since the value of C_{f2} is taken larger than C_{f1}, it always remains possible to charge C_{f1} near its reference voltage value by applying both states 8b and 9b. This chopper action is also evident from Fig. 6 where, following t_b, the positive value of $i_{\rm Cf2}$ indicates charging while the negative value indicates discharging of C_{f2}. At t_b, $v_{\rm Cf1}$ also reaches within its allotted band of $V_{\rm dc}/3 \pm \Delta V_{\rm Cf1}$, and following this instant, the steady-state operation of the chopper is activated by applying region (B) state sequences. In steady state, the dc-link capacitor voltages are equalized, and flying-capacitor voltages are balanced by exchanging very insignificant energy between them. Similar to that in the three-level case, the capacitors C_{f1} and C_{f2} of the four-level chopper can be discharged as well from a given initial value to their corresponding target voltages. To do this, the states listed in Table IV are used in the same manner as these are used for the charging of C_{f1} and C_{f2} in Fig. 6. The corresponding simulation results are, however, not presented here.

It is observed from the simulation studies that, for higher chopper levels, the flying-capacitor voltage regulation becomes slower as observed in Fig. 6, where C_{f2} is required to be discharged undesirably so that C_{f1} could get charged, and then, C_{f2} is again charged to reach its reference. As the number of flying capacitors increases with the chopper levels, more undesirable charging or discharging of flying capacitors will be required, followed by other charging or discharging processes which will slow the process. However, it can be seen from Fig. 6(a) that, even with the undesired discharging of C_{f2}, $v_{\rm Cf2}$ is well balanced and will remain so as a very small value of $\Delta V_{\rm Cf}$ is chosen and only region (B) state sequences are used in the steady state. It is to be noted that the time response of the proposed choppers depends on the size of capacitors and inductors involved.

V. Experimental Results

In order to validate the flying-capacitor-based-chopper proposal and the control schemes presented earlier, a five-level diode-clamped inverter system is implemented in the laboratory. The overall structure of the experimental setup is shown in Fig. 7. The main power circuits consist of a single-phase five-level voltage source DCMLI, load, and dc-link circuit. The inverter dc bus is supported by a separately controllable dc supply obtained from a single-phase transformer and diode rectifier circuit. In this figure, HV denotes the Hall effect voltage transducers. For example, HV6 represents the voltage sensor connected across C_{f1} which senses $v_{\rm Cf1}$. Similarly, HC1 and HC2 represent the Hall effect current transducers sensing the chopper currents. The inverter loads consist of RL components with the parameters the same as considered earlier in Section IV. Each switch S_1 to S_{41} consists of an insulated-gate bipolar transistor (IGBT) with an antiparallel diode. The IGBT module used is a Mitsubishi CM75DY-24H [45]. This is a 1200-V/75-A IGBT with two IGBTs/diodes in each module. For simplicity, the same IGBT modules are also used as clamping diodes with a shorted gate in the inverter, as shown in Fig. 7. The dc-link capacitors are $C_{d1} = C_{d2} = C_{d3} = C_{d4} = 220$ μF, and the chopper circuit parameters are $R_1 = R_2 = 2.0$ Ω, $L_1 = L_2 = 20$ mH, and

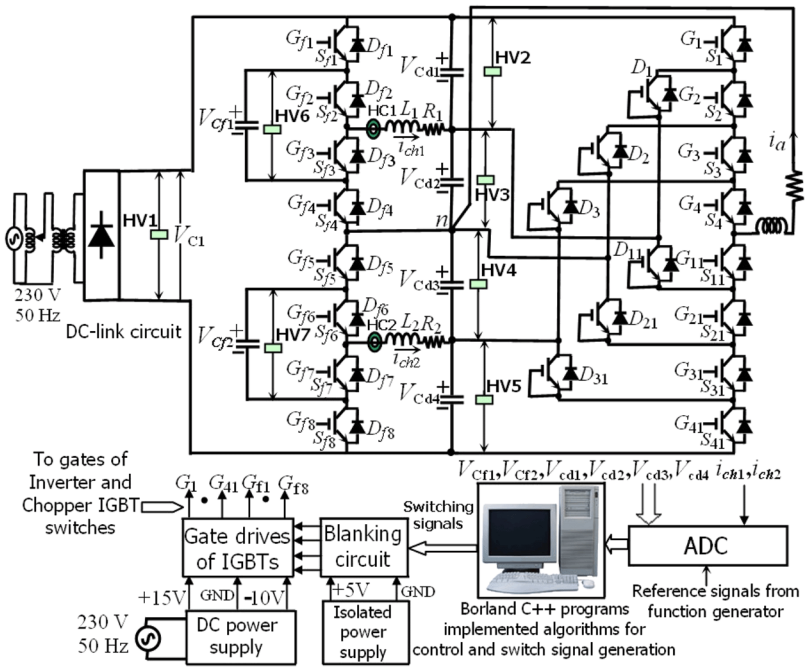

Fig. 7. Overall structure of the experimental setup.

$C_{f1} = C_{f2} = 2200\ \mu$F [Fig. 2(a)]. The dc-link voltage $V_{\rm dc}$ is kept fixed at 80 V, and ΔV_C and $\Delta V_{\rm Cf}$ (Fig. 3) are taken the same as in the simulation studies presented earlier.

In Fig. 7, the block diagram for PC interfacing and other controllers are also shown. The low-voltage signals from the transducers connected to the power circuits are used as inputs to various controllers. For multilevel modulation, an external modulating signal and four carrier signals of the same characteristics as considered in the previous section are used. These are acquired by a PC (P-1V, 2.4 GHz, 256-MB RAM, 40-GB hard disk drive) through analog-to-digital converter channels of a standard data acquisition card (NI DAQmx PCI-6259) [46]. Based on these quantities, a program written in Borland C++ is implemented for the control tasks. The corresponding switching decision signals are generated at the digital-output port of the DAQ and are passed to the IGBT driver circuits after introducing a lockout delay of 7.5 μs using blanking circuits. The blanking circuit is designed using monostable 74LS123 and AND gate 7408. The blanking circuit is required to avoid the short circuit of a dc-link voltage due to the finite turn-off and turn-on times of IGBT switches. IGBTs require a gate voltage signal in order to establish collector-to-emitter conduction or nonconduction. A single-phase five-level inverter topology associated with the chopper circuit in Fig. 2(a) needs 16 gate drivers. Mitsubishi M57959L hybrid IGBT driver modules are chosen to perform this task. This is a high-speed component that is endowed with a voltage logic level input and insulated by a high-speed optocoupler that protects against the event of a short circuit [47].

The inverter system in Fig. 7 is made to run first with the chopper inactivated. The corresponding results are shown in Fig. 8. As discussed earlier in Section II, it is evident from Fig. 8 that C_{d1} and C_{d4} are charged while C_{d2} and C_{d3} are discharged. These charging and discharging lead to $V_{\rm Cd2} \approx V_{\rm Cd3} \approx 0$ and $V_{\rm Cd1} \approx V_{\rm Cd4} \approx V_{\rm dc}/2$ as the capacitors

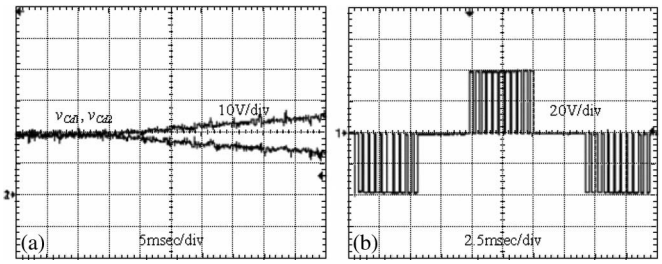

Fig. 8. Experimental results without chopper-supported dc link. (a) Unbalanced dc capacitor voltages and (b) inverter output voltage with completely discharged inner dc capacitors.

are completely charged or discharged. This results in the loss of the five-level waveform of the inverter output voltage, and it resembles a three-level output, which can also be seen from Fig. 8(b).

Following the complete charging/discharging of dc capacitors, corresponding to Fig. 8(b), the three-level chopper is then turned on and operated using the control scheme presented earlier (Fig. 3). The corresponding experimental results are shown in Figs. 9 and 10. In Fig. 9, the chopper is enabled at t_e, and before this instant, the dc-link capacitors were completely charged/discharged, and their voltages were unequal. As soon as the chopper is activated, a large chopper current $(i_{\rm ch1})$ builds up to reduce $v_{\rm Cd1}$ and subsequently increase $v_{\rm Cd2}$. This large value of $i_{\rm ch1}$ is due to the large value of $\Delta V_{\rm Cd1}$. Following this, the chopper equalizes the capacitor voltages with reduced chopper current, depending on the system and control parameters, as shown in Fig. 10. The flying-capacitor voltage $(v_{\rm Cf1})$ shown in Fig. 10(a) is tightly regulated around its reference value of 20 V in the steady state. The steady-state dc-link capacitor voltages shown in Fig. 10(b) can be seen to be equalized. Similar results are also obtained for the lower chopper set [Fig. 2(a)], which, however, are not shown here.

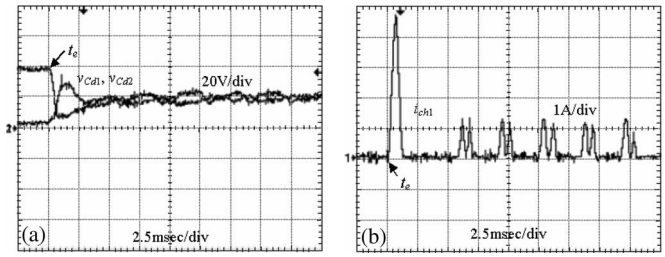

Fig. 9. Experimental results of the three-level chopper. (a) DC capacitor voltages achieving equalization as the chopper is activated. (b) Chopper current.

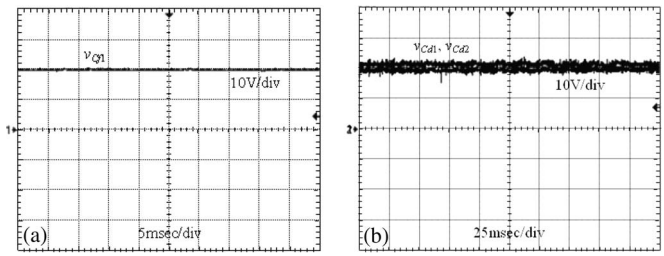

Fig. 10. Experimental results of the three-level chopper. (a) Flying-capacitor voltage in steady state and (b) equalized dc capacitor voltages in steady state.

With balanced capacitor voltages, the inverter output phase voltage is of a symmetric five-level shape. It is also evident that the theoretical and experimental results agreed with each other with acceptable errors. It is therefore concluded from the simulation and experimental results that the flying-capacitor-based chopper is able to meet the objectives set for it.

VI. Conclusion

A flying-capacitor-based chopper has been proposed for dc capacitor voltage equalization in a DCMLI. It requires additional power semiconductor devices and capacitors but of reduced voltage rating compared with the conventional chopper. Two configurations of this topology, named as three-level and four-level choppers, are analyzed for generalization purposes. These are different in capacitor and semiconductor device count and correspondingly reduce the device voltage stresses by half and one-third, respectively. The working principles and control schemes for these circuits have been presented. It has been shown that, by preferentially selecting the available redundant chopper switch states, the dc-link capacitor voltages can be efficiently equalized in addition to having tightly regulated flying-capacitor voltages around their references. The various operating modes of the chopper are described along with their preferential selection logic to achieve the desired performances. Simulation and experimental results obtained have verified the viability and effectiveness of the voltage-balancing circuit and control, even in transient states. This proposed topology is expected to be more reliable, loss efficient, and able to enhance the ride-through capability of the inverter system, and these features need to be investigated further.

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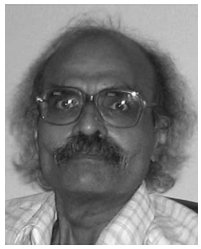

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