Modeling and control of renewable energy systems

Hybrid Cascade Converter Topology with series Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells

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Abstract- A novel H-bridge multilevel PWM converter topology based on a series connection of a high voltage (HV) diode-clamped inverter and a low voltage (LV) conventional inverter is proposed. A DC link voltage arrangement for the new hybrid and asymmetric solution is presented to have a maximum number of output voltage levels by preserving the adjacent switching vectors between voltage levels. Hence, a fifteen-level hybrid converter can be attained with a minimum number of power components. A comparative study has been carried out to present high performance of the proposed configuration to approach a very low THD of voltage and current, which leads to the possible elimination of output filter. Regarding the proposed configuration, a new cascade inverter is verified by cascading an asymmetrical diode-clamped inverter, in which nineteen levels can be synthesized in output voltage with the same number of components. To balance the DC link capacitor voltages for the maximum output voltage resolution as well as synthesise asymmetrical DC link combination, a new Multi-output Boost (MOB) converter is utilised at the DC link voltage of a seven-level H-bridge diode-clamped inverter. Simulation and hardware results based on different modulations are presented to confirm the validity of the proposed approach to achieve a high quality output voltage.

I. INTRODUCTION

Multilevel power conversion has achieved wide acceptance for its capability of high voltage, and high efficiency operation. The most popular advantages of the multilevel inverter compared with the traditional voltage source inverter, are high power quality waveforms with lower distortion, and a low blocking voltage by switching devices. As the number of levels increases the above advantages will be enhanced, however, it can impose a significant expense of the increase in circuit complexity which reduces the reliability and efficiency in such a converter. Three prominent five-level inverter topologies; diode-clamped [1], flying capacitor [2], and cascade [3] are shown in Fig.1. An extensive comparison between the multilevel topologies have been performed in [4] in terms of their applications, circuit modeling, modulation techniques and technical issues. Among these topologies, cascade configuration has been attracted for medium and high voltage renewable energy systems such as photovoltaic due to its modular and simple structure. Application of the cascade inverter for renewable energy systems is reviewed in [5, 6]. Higher-level can easily be implemented by adding classical H-bridge cells to this configuration. However, it needs additional DC voltage sources and switching devices. Proposition of a cascade converter using a single DC source and capacitors is proposed in [7] which can save the extra DC sources for higher-level converters, however, a capacitor voltage balancing algorithm is required [8]. Typically, different types of multilevel converters are utilised with the same rating of the DC link voltages and power devices due to modularity and simplicity of the control strategy. Recently, asymmetrical multilevel inverters with unequal DC source voltages have been addressed in literature [9-30]. Therefore, based on different switching states it is possible to achieve more voltage levels on output voltage by adding and subtracting DC link voltages compared with conventional multilevel inverters with the same number of components [9]. By doing so, output voltage with superior quality can be obtained with less circuit and control complexity and also, increasing the harmonic characteristic of the output voltage can decrease the size of the filter. The hybrid converters have been the main focus of the literature with regard to asymmetrical configuration of multilevel inverters as they have shown their abilities and strengths in medium and high power applications [9, 12]. Diverse topologies have been studied based on a variety of H-bridge cascaded cells and DC voltage ratio to enhance the output voltage resolution compared with the same DC voltage ratio of the cells [12-30]. However, due to the different voltage rate of switching devices in hybrid configuration, it loses its modularity compared with symmetrical cascade inverters. Various PWM strategies for symmetrical cascade inverters with high and fundamental switching frequency have been presented [14-16]. To reduce switching losses and improve the converter efficiency, hybrid modulations for cascade converters with unequal DC sources is proposed which allows use of the slow switching device in the higher voltage cells and fast switching devices in lower voltage cells [17-19].

Since more voltage levels correspond to the increasing number of components, recent research in this area has focused on a series of connected multilevel converters in cascaded H-bridge structure [28-30]. The structure of the cascaded multilevel

inverter is demonstrated in Fig.2. Therein, configuration consists of *m*-level multilevel H-bridge cells (either diode-clamped or flying capacitor inverter) each with an isolated DC source.

The number of cells depends on the desired output voltage level which is synthesised by adding up all the H-bridge cells output voltage as $v_{out}(t)= v_{out1}(t)+v_{out2}(t)+v_{out3}(t)+\ldots+v_{outN}(t)$. In a system which utilises equal sets of DC sources ($V_{dc1}=V_{dc2}=V_{dc3}=\ldots=V_{dcN}$), the number of output voltage levels is $N\times (m-1) +1$ where; N is the number of cascaded cells, and *m* is the number of output voltage levels in each multilevel H-bridge cells. The main advantage of this arrangement is the simplicity to cascade several H-bridge cells for improvement of the output voltage resolution with reduced number of components. However, capacitor voltage imbalance and complexity of system can cause a critical problem which should be taken into account in this configuration either using diode-clamped or flying capacitor topology [31, 35]. To address this limitation, isolated DC sources or alternatively, auxiliary converters, can be used for capacitor voltage balancing. Utilization of unequal DC sources on each series diode-clamped or flying capacitor cells can increase the number of output voltage for a given power circuit in Fig.2, with the equivalent number of components. A different DC voltage ratio for H-bridge cells is proposed to achieve the maximum number of output voltage levels. However, along with possible maximisation of obtainable output voltage levels based on the voltage ratio of DC sources, the existence of adjacent switching vectors to move from one possible voltage level to another with only one switch change should be considered. Simultaneous switching of different switches is not an immense problem when there are just a few of them happening over one cycle, however, when switching between the nonadjacent switching vectors occurs frequently in modulation between adjacent levels, it becomes a critical issue to increase the switching losses.

In this paper, a general idea of cascading multilevel H-bridge cells is used to propose different configurations using a seven-level symmetrical and asymmetrical diode-clamped H-bridge converter supplied with a MOB converter, cascaded with classical three-level inverters. The MOB converter can solve the capacitor voltage imbalance problem as well as boost the low output voltage of renewable energy systems such as solar cells to the desired value of the diode-clamped DC link voltage. DC voltage ratio of cells will be presented to obtain maximum voltage levels on output voltage with adjacent switching vectors between all possible voltage levels, which can minimize the switching losses. Using a triple-output DC-DC converter offers asymmetrical DC link capacitor voltage arrangement for the seven-level H-bridge diode-clamped converter, in which nine voltage levels can be obtained with the same number of components. Using an asymmetrical diode-clamped converter in the proposed cascaded H-bridge cells achieves four more voltage levels in output compared with symmetrical configuration. Performance of the proposed asymmetrical H-bridge diode-clamped inverter has been verified by simulation and hardware results. Finally, two different PWM methods based on predictive current control have been presented to validate the proposed approach.

II. Symmetrical and Asymmetrical Diode-Clamped Converter (SDCC and ADCC) Using MOB Converter

A new DC-DC boost converter with multiple outputs, which can be used as a front-end converter to boost the inverter's DC link voltage for grid connection systems based on diode-clamped converter, is analysed in [35]. Using this MOB converter, the DC voltage across each capacitor can be adjusted to a desired voltage level, thereby solving the main problem associated with balancing the capacitors' voltages in such converters. Authors in [11] presented a new modulation technique for a diode-clamped inverter when voltages across capacitors are unequal. Fig.3 shows a configuration for an H-bridge seven-level diode-clamped inverter joint with the front-end MOB converter. An unequal DC link arrangement is applied instead of identical DC link capacitor voltages. The bottom capacitor's voltage is kept at twice the level of other capacitors during operation, so that configuration has asymmetrical behaviour with respect to the neutral point ($V_{c1}=2V_{c2}=2V_{c3}$). As shown in Fig.3, it is supposed that the low input voltage (E) is boosted to V_{dc} at the DC link of seven-level diode-clamped H-bridge inverter (V_{NM}). Therefore, in the SDCC configuration, DC link capacitors voltage ratio are $V_{c1}=V_{c2}=V_{c3}=V_{dc}/3$, however, in ADCC configuration, capacitors' voltages are maintained at $V_{c1}=V_{dc}/2$, and $V_{c3}=V_{c2}=V_{dc}/4$ (with respect to the neutral point).

According to the structure of the seven-level diode-clamped converter, there are four possible switching states in each leg of the inverter that can be derived from four switch combinations to obtain different DC link voltage levels. The "on" and "off" switching states of each switch are defined as "1" and "0", respectively. Four switching states in one leg of the diode-clamped H-bridge inverter are distinguished by four switching function states which are summarised in Table 1. For example, (011) means that S_1=0 (off), S_2=1 (on), and S_3=1 (on), which is defined as switching function state "2".

All possible switching states associated with different output voltage levels in SDCC and ADCC converters are shown in Table 2. Exploring the output voltage levels, nine different voltage levels can be generated in asymmetrical DC link arrangement based on different switching states, in which two more voltage levels can be synthesised in output voltage compared with the symmetrical arrangement with the same number of switching devices.

From the possible switching function states defined in Table 1, Fig.4 shows the adjacency diagram of SDCC and ADCC configurations. As shown, the adjacent vectors are available between all voltage levels in both configurations, so that all voltage levels can be achieved with one switch change. However, non-adjacent switching transitions are required between the following switching transitions in the ADCC configuration which are depicted by dashed lines in Fig.4:

- (20) and (31)
- (02) and (13)

This transition requires two switch changes in the ADCC. To remove non-adjacent voltage vector in positive voltage levels, when the controller increases the voltage level from $V_{dc}/2$ to $3V_{dc}/4$, transition occurs from switching function states (31) to (20). Then the controller uses switching function state (10) for modulation between $V_{dc}/2$ and $3V_{dc}/4$. Also, after the occurrence of the transition from $3V_{dc}/4$ (20) to $V_{dc}/2$ (31), the controller uses state (21) for the modulation between $V_{dc}/2$ and $V_{dc}/4$. The same situation happens when the output voltage is negative. Therefore, these non-adjacent switching transitions occur only four times during one cycle. It is apparent that by aassuming that switching losses is proportional to the number of switching per cycle**,** the switching loss associated with the extra switching is negligible in the high switching frequency. As a result, improved voltage waveforms can be obtained using ADCC topology compared with SDCC topology with the same number of components and almost same number of switching.

Although the output voltage of the asymmetrical DC link arrangement benefits from two more voltage levels with the same number of components compared with symmetrical DC link arrangement, extra voltage rates should be paid for two switches in each leg of the inverter. Maximum voltage across switching components during different switching states is derived in Table 3 to have a comparison between the voltage rating in the symmetrical and asymmetrical DC link arrangements. In the asymmetrical configuration, the maximum voltage rating of switches (S_3 and S_6) in each leg is $V_{dc}/6$ more than the switches in the symmetrical configuration for the same DC link voltage. By investigating the voltage ratings, maximum voltage rating of diodes (D_{c1} and D_{c3}) decreased by $V_{dc}/12$ and $V_{dc}/6$; however, the maximum voltage tolerated by another two diodes (D_{c2} and D_{C4}) increased by $V_{dc}/12$ and $V_{dc}/6$, which shows that the maximum voltage across diodes has not been changed in both configurations.

The output voltage of the symmetrical and asymmetrical single-phase diode-clamped inverters for the same circuit parameters is shown in Fig.5. Herein, in the DC-DC side, input voltage (*E)* is assumed as 100V; switching frequency of the DC-DC converter (f_{sw}) is 10 kHz, L=2mH, and C_1=C_2=C_3=1mF, while in the inverter side fundamental and switching frequencies are f=50Hz, f_{sw}=4 KHz, and the DC link of seven-level diode-clamped inverter (V_{NM}) is boosted to 300 V using a triple-output boost converter. Mid point voltage regulation for symmetrical and asymmetrical configurations for m_a=1and PF=1 has been shown in Fig.5 (a). It is clear that the MOB converter is able to boost the low input voltage for DC link capacitors as well as balance the capacitors voltage to the desired level for m_a=1 and pure resistive load which is impossible in more than five-level single-phase diode-clamped topology without an active front-end converter. In order to generate output voltage, based on the duty cycle of switches, the controller chooses the next suitable switching function state using the adjacent vectors in Fig.4. To show the performance of the proposed structure for inductive load, Fig.5 (b) illustrates the DC link capacitor voltage control and output voltage for m_a=1 and PF=0.5. In order to synthesising an equal DC link capacitor voltage arrangement in the conventional configuration, while the total voltage of an inverter DC link is boosted at

300V, mid point voltages (V_{c1} and $V_{c1}+V_{c2}$) are controlled at 100V and 200V. However, to have an asymmetrical DC link configuration, mid point voltages are controlled at 150 V and 225 V, respectively

A laboratory prototype of a symmetrical and asymmetrical seven-level H-bridge inverter has been implemented to practically verify the proposed configuration. The laboratory prototype has been tested for the following specifications: V_{dc}=90 V, $I_{out\text{-}peak}$=5 A, f=160Hz and f_{sw}=6 kHz under pure inductive load L=16mH. A predictive current control has been developed in a V850E/IG3 microcontroller to force the load current to follow the reference for the H-bridge seven-level diode-clamped inverter with symmetrical and asymmetrical DC link arrangements. Switching states to generate the desired voltage level based on the amount of current reference is chosen by the microcontroller according to adjacent switching vectors. Output voltage and current of the symmetrical and asymmetrical seven-level diode-clamped inverter is demonstrated in Fig.6. Regarding simulation and hardware results, two more voltage levels can be synthesised in output voltage of ADCC configuration compared with SDCC configuration with using the same number of components and structure. Therefore, the seven-level H-bridge inverter performs in the same way as a nine-level inverter. To examine the performance of the asymmetrical configuration, harmonic spectrums associated with the output voltage of the both SDCC and ADCC configurations are exposed in Fig.6. Comparing harmonic spectrums, better harmonic performance is obtainable using the asymmetrical DC link arrangement for the diode-clamped converter. This achievement allows on one hand, an improvement in output voltage harmonic characteristics with a same number of components compared with symmetrical seven-level H-bridge configuration, and on the other hand, a decrease in cost and complexity of inverter hardware layout structure with the same output waveforms quality compared with the symmetrical nine-level H-bridge inverter.

III. Proposed Multilevel Hybrid Cascade Converters

One of the aspects of this paper is to select DC input voltages for a topology based on a series connection of a symmetrical and asymmetrical diode-clamped H-bridge cell with three-level H-bridge inverters to achieve a maximum number of output levels by preserving the minimum switching losses. Simultaneous switching of different switches is not a real problem when there are just few of them happening over one cycle, however, repeatedly switching between the nonadjacent switching vectors is not acceptable, due to an increase in switching losses and commutation noise. The state of art in this topology can improve the resolution of the output voltage with minimum power components, while keeping the adjacent switching vectors between all modulation voltage levels. Fig.7 presents the schematic of this configuration for a two-cell hybrid cascade converter. The MOB converter is utilised to supply DC input voltage of diode-clamped multilevel H-bridge cell to regulate capacitors voltages and provide the desired voltage rate for the DC link capacitors.

To achieve maximum resolution in output voltage of the N-cell proposed topology, DC voltage arrangement should be considered as follows:

$$V_{dcN} = \frac{Minimum\ voltage\ \ level\ of\ multilevel\ \ inverter}{2^{N-1}} \quad (1)$$

where, for proposed two-cell inverter in Fig.7, we have:

$$V_{dc2} = \frac{Minimum\ voltage\ \ level\ \ of\ multilevel\ \ inverter}{2} \quad (2)$$

Based on this arrangement, the number of output voltage levels can be derived from Eq.1:

$$number\ \ of\ \ output\ \ levels = 2^{N-1} \times (m+1) - 1 \quad (3)$$

where, m is the number of output voltage levels of multilevel H-bridge inverters and N is the number of cells. Regarding Eq.3, there are two possibilities to increase the obtainable voltage levels in the proposed configuration. One solution is by adding a classical three-level H-bridge inverter in which the number of voltage levels will be doubled. This imposes four extra switches and one isolated DC source in regular configuration of the system. Although implementation of a three-level inverter by a DC capacitor saves the isolated DC source, it still requires four extra switching devices, extra DC link capacitor and further effort on capacitor voltage balancing [7, 8, 19]. Alternatively, the number of output voltage levels increases by raising the diode-clamped output voltage levels, in which four extra switches, four clamped diodes and one DC link capacitor are needed.

According to the ADCC configuration, using asymmetrical configuration in diode-clamped DC link voltage leads to an increase in the output voltage levels without increasing the number of components in a diode-clamped H-bridge structure. Here, the realisation of the asymmetrical configuration for H-bridge diode-clamped inverters in the proposed hybrid cascaded topology results in an increase in the number of output voltage levels with the same number of components. This issue will be comparatively discussed for two cells H-bridge cascade connection with seven-level SDCC and ADCC configurations in the following sections.

A. Two-cell Cascaded H-bridge Converter with Seven-level H-bridge SDCC

Fig.8 illustrates a fifteen-level cascade inverters assembled from one module of a HV symmetrical H-bridge seven-level diode-clamped inverter and LV classical three-level H-bridge inverter. Herein, the DC link voltage of a diode-clamped inverter is boosted and regulated for the equal rate by MOB converter. To meet the Eq.2 where the DC link voltage of the classical inverter is half of the lower level of the diode clamped inverter, the DC link voltage of the diode-clamped inverter is regulated to $V_{dc1}=6V_{dc2}$ using the MOB converter. Referring to Eq.3, fifteen different voltage levels can be achieved on output voltage.

Possible switching states for both the seven-level H-bridge SDCC and three-level inverter with relevant output voltage levels have been shown in Table 4. The adjacent switching vectors of the different voltage levels for the proposed topology

associated to switching states of H-bridge cells are depicted in Fig.9. The first two digits of each switching function states are allocated to the diode-clamped inverter in terms of Table 1 and the other two digits belong to the three-level H-bridge inverter switching function state which is "1" when S_{13}=0 and S_{14}=1 and "2" when S_{13}=1 and S_{14}=1.

According to the adjacent switching vector diagram, switching transitions employ switches of only the LV cell for modulation between adjacent levels, so that it is possible to achieve different levels with just one switch change, except for in movement from a pair of modulated levels to another. Therefore, three extra switching transitions take place in each half cycle between non-adjacent voltage vectors. For a positive half a cycle, extra switching occurs when the voltage level is changed from $V_{dc}/6$ (0021, 1121, 2221, 3321) to $V_{dc}/3$ (1011, 1022, 2111, 2122, 3211, 3222), $V_{dc}/2$ (1021, 2121, 3221) to $2V_{dc}/3$ (2011, 2022, 3111, 3122), and $5V_{dc}/6$ (2021, 3121) to V_{dc} (3011, 3022). Although these extra switching losses will be negligible in high switching frequency, using a proper PWM method can avoid any extra switching losses in this configuration.

B. Two-cell Cascaded H-bridge Converters with Seven-level H-bridge ADCC

A higher number of levels can be easily obtained using an asymmetrical diode-clamped inverter in the HV cell as the MOB converter can constrain capacitors' voltage to different voltage rates. Fig.10 presents a proposed hybrid cascade converter where the bottom capacitor voltage in the diode-clamped inverter is twice the other capacitors, so that the minimum voltage level in this configuration is $V_{c2}=V_{c3}=V_{dc}/4$. To meet the requirement of the Eq.2 to have maximum output voltage levels with adjacent switching vectors, the DC link of the diode-clamped inverter is controlled at $V_{dc1}=8V_{dc2}$ using MOB converter, in which the DC link voltage of the three-level inverter is half that of the lower voltage of the diode-clamped inverter. According to the Eq.3, nineteen voltage levels can be achieved using ADCC in multilevel H-bridge cell. Furthermore, there is no need for a control strategy to balance the capacitors' voltage as MOB regulates the capacitors voltage which reduces the complexity of the control system in a higher number of levels. Table 5 presents the output voltage level corresponding to the possible switching states for both the seven-level ADCC H-bridge converter and three-level inverters. As shown, using the asymmetrical configuration for diode-clamped topology in the HV cell, the output voltage has nineteen levels which is four levels more than the proposed cascade configuration with SDCC configuration. Therefore, increasing voltage levels of cascaded H-bridge inverter can lead to a better output voltage quality and reduction or elimination of the output filter.

The adjacency of switching function states with regard to switching states in Table 5 is shown in Fig.11 for all output voltage levels of the proposed topology. As shown, adjacency is available between all voltage levels and all the transitions between adjacent voltage levels employs switches of only the LV cell, except for moving from a pair of modulated levels to another. Since these transitions do not occur repeatedly, four extra switching take place in each half cycle between non-

adjacent vectors compared with a symmetrical configuration when the voltage level is changed from $V_{dc}/8$ (0021, 1121, 2221, 3321) to $2V_{dc}/8$ (2111, 2122, 3211, 3222), $3V_{dc}/8$ (2121, 3221) to $V_{dc}/2$ (1011 1022, 3111 3122), $5V_{dc}/8$ (1021, 3121) to $6V_{dc}/8$ (2011, 2022), and $7V_{dc}/8$ (2021) to V_{dc} (3023,3011). Utilisation of proper PWM strategy is necessary to achieve high performance output voltage with respect to adjacent switching vectors to minimise extra switching losses in this configuration.

IV. Performance Comparison of Proposed Hybrid Converters under Modulation Schemes

To study the operation of the proposed cascaded H-bridge converters, the PWM converter scheme has been simulated using Matlab software. The main electric components of the power circuit are given in Table 6. To confirm the validity of the system, a comparison study has been carried out for H-bridge cascaded converters with symmetrical and asymmetrical diode-clamped inverters. In order to achieve identical comparison, equal parameters are considered for both topologies. Total DC link voltage of two cells is assumed at 270V, where the DC link voltage of the classical three-level inverter is 39V for the fifteen-level converter and 30V in a nineteen-level converter. To verify the fifteen-level and the nineteen-level hybrid converters based on the Eq.2, the DC link voltage of the symmetrical and asymmetrical diode-clamped converters should be controlled at 231V and 240V respectively. Therefore, DC like capacitor voltage should be regulated to have an equal ($Vc1=V_{c2}=V_{c3}$) or unequal ($V_{c1}=2V_{c2}=2V_{c3}$) DC link arrangement.

Different PWM techniques have been proposed for single-phase and three-phase hybrid converters in order to have a high quality load voltage and low switching losses [36-39]. A simple and generalized time-domain duty cycle computation technique for the single-phase multilevel inverters has been extended for the hybrid converters in [37], where the reference voltage is achieved as the averaged value between two nearest output voltage levels of the converter. However, the performance of the proposed method for hybrid converters decreases compared with the cascade inverter as the calculations increase. In addition, adjacent switching vectors have not been considered for hybrid configuration which can increase the losses. Current control is an essential part of the overall control system which allows instantaneous current waveform control with high accuracy, as well as peak current protection and overload rejection [38, 39]. A novel predictive current control based on adjacent voltage vectors has been proposed [38] for three-phase multilevel converters which can easily be applied for the multilevel with different voltage levels without significant changes in the control system. In this paper a general idea of predictive current control is utilised to generate the desired current for asymmetrical and symmetrical H-bridge cascaded configurations based on adjacent switching vectors. According to Fig.8 or Fig.10, the phase output voltage can be defined in terms of the *RL* load component as follows:

$$v_{out} = Ri_{out} + L\frac{di_{out}}{dt} + e \quad (4)$$

i_{out}= load current
v_{out}=phase voltage
R=load resistance
L=load inductance
e=back emf voltage

Since the aim of this PWM is to justify the performance of proposed cascade converters to synthesise all voltage levels, pure inductive load has been studied as a load (R=0, e=0). Thus, Eq.4 can be rewritten as follows in each switching period:

$$v_{out} = L\frac{i_{out,n+1} - i_{out,n}}{T_{sw}} \quad (5)$$

where, $i_{out,n+1}$ is the amount of current in the next switching cycle , $i_{out,n}$ is the present current, and T_{sw} is the switching period. Therefore, form the Eq.5, duty cycle to force the load current to track the reference current in the next switching period can be predicted by:

$$d = L\frac{I_{ref} - i_{out,n}}{V_{dc}T_{sw}} \quad (6)$$

According Eq.6, the duty cycle can easily be calculated by measuring the load current. Once the duty cycle of all switches has been calculated to generate the desired currents at the end of each switching cycle, the duty cycle of switches can be defined based on the amount of total duty cycle from Eq.7.

Defined voltage levels based on duty cycle for the fifteen-level and the nineteen-level proposed hybrid converters are shown in Table 7.

- $0 < \sum_{1}^{n-1} d_j < \frac{1}{(n-1)}$
- $\frac{1}{(n-1)} < \sum_{1}^{n-1} d_j < \frac{2}{(n-1)}$. (7)

⋮

- $\frac{(n-2)}{(n-1)} < \sum_{1}^{n-1} d_j < 1$

where, n is the number of non-negative voltage levels per leg and $\sum_{1}^{n-1} d_j$ is a sum of duty cycles of all switches per leg.

Based on the defined voltage levels in each switching cycle, the controller identifies relevant switching states of the particular voltage level regarding adjacent switching vectors to minimise switching losses. However, according to the adjacent switching vectors graph for the fifteen-level and nineteen-level converters (Fig.9 and Fig11), there are some non-adjacent switching states that occur in some voltage levels, in which extra switching losses applies to achieve desired voltage levels. Based on the controller's decisions at these points to change the voltage levels, two different methods have been proposed to achieve the proper switching states.

A. With Extra Switching

In the first method, switching states are chosen to achieve different voltage levels regardless of adjacency between switching transitions. As is depicted for one non-adjacent point in Fig.12, to increase the voltage from $V_{dc1}/6$ to $V_{dc1}/3$ in the fifteen-level or from $V_{dc1}/8$ to $V_{dc1}/4$ in the nineteen-level converter, the switching function states should be changed from (3321) to (3222). Then the controller uses (3222) and (3212) for modulation between those voltage levels. Therefore, one extra switching transition happens due to non-adjacent vectors. The same situation happens for the other non-adjacent transitions which happen twelve times in the fifteen-level converter and sixteen times in the nineteen-level converter in each fundamental cycle.

Although it is possible to achieve sequenced voltage level by locating the duty cycles in the middle of each switching cycle, extra losses should be paid. Extra switching can be determined by following equation:

$$Extra\ \ switching\% = \frac{Extra\ \ switching\ \ \ transition \times Fundamental\ \ \ frequency}{Switching\ \ \ frequency} \tag{8}$$

Fig.13 shows the extra switching in terms of switching frequency. As shown, total extra losses will be negligible in higher switching frequencies. Fig.14 illustrate output voltage for the fifteen-level and the nineteen-level hybrid converters with extra losses method at f_{sw}=5 KHz, respectively. Output waveforms are nearly sinusoidal and current tracks the reference current accurately. THD of output voltage has been calculated as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} (V_n)^2}}{V_1} \tag{9}$$

However, to have a harmonic current distortion factor, weighted total harmonic distortion (WTHD) of output voltage has been compared for symmetrical and asymmetrical hybrid converters based on Eq.10.

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty} (\frac{V_n}{n})^2}}{V_1} \tag{10}$$

THD of output voltage and current waveforms for one switching frequency sideband of the proposed hybrid cascade converter with the symmetrical and asymmetrical diode-clamped converter in terms of different switching frequencies are depicted in Fig.15. Corresponding to Fig.13 and Fig15, as the trend of THD and extra losses is decreasing in higher switching frequencies; the THD of the hybrid converter with ADCC is almost 1.7% less than the symmetrical one. As shown in Fig.15, once the switching losses are negligible in high switching frequencies, the WTHD of the proposed configuration decreases either for the fifteen-level and nineteen-level. However, configuration with the asymmetrical diode-clamped H-bridge shows better harmonic characteristics compared with the configuration with symmetrical H-bridge converter. Based on proposed cascaded configuration, switches in the high voltage multilevel cell work at the fundamental

frequency, while switches of low voltage cell work with the switching frequency. Enhanced harmonic characteristics are expected for asymmetric configuration as the number of output voltage in configuration with symmetrical diode-clamped is lower than asymmetrical configuration.

B. Without Extra Switching

In order to avoid any extra switching a second method to select the proper switching states is proposed which is shown as a non-adjacent voltage vector in Fig.16. Thus, to change voltage level from $V_{dc1}/6$ to $V_{dc1}/3$ in the fifteen-level and from $V_{dc1}/8$ to $V_{dc1}/4$ in the nineteen-level converter switching transitions occur from (3322) to (3222). Then the controller uses (3222) and (3212) for modulation between those voltage levels. By doing so, no extra switching happens to increase the voltage levels. However, the voltage will jump two levels by choosing these switching function states. Therefore, twelve jumps of these voltage levels occurs in the output voltage of the fifteen-level inverter as it has twelve non-adjacent switching transitions in each fundamental frequency. The same scenario happens for the nineteen-level hybrid inverter as it has sixteen non-adjacent switching vectors in each cycle. Setting the pulse width based on defined duty cycle in the middle of the switching cycle gives an opportunity to obtain upper voltage levels with a jump and without any extra switching losses. However, a number of asymmetrical pulse patterns occur in each fundamental frequency (twelve times in fifteen-level and sixteen times in nineteen-level inverter), and worse THD is expected for this PWM method compared with previous one. Fig.17 demonstrates the output voltage waveforms at f_{sw}=5 KHz in the proposed hybrid cascade converter with SDCC and ADCC configurations, respectively.

To compare the quality of the waveforms of hybrid cascade converter with symmetrical (fifteen-level) and asymmetrical (nineteen-level) diode-clamped inverters, THD and WTHD for one side band of the switching frequency of the output voltage according to Eq.9 and Eq.10 are illustrated in Fig.18. Although, the quality of output waveforms is less than PWM strategy with extra switching due to the number of voltage jump, configuration with ADCC H-bridge provides better quality waveforms. In higher switching frequencies, as the number of voltage jumps is negligible, harmonic characteristics of output waveforms are improved.

The diversity of two methods either in the case of THD of voltage and current or extra switching losses is negligible in higher switching frequency (more than 8 KHz), which shows the high performance of this proposed method to achieve more voltage levels with minimum power components and losses. Nevertheless, in low switching frequency based on different application proper PWM method can be chosen in order to have a better quality or minimum losses respectively.

To study the effect of the DC link variation on performance of the proposed converters, two different ripples, 5% and 10% of the DC link voltage, have been taken into account in both modulation techniques for the inductive load at the switching frequency of 10 KHz. In the fifteen-level converter with the extra switching, the THD rose to 7.2% and 9.8% at 5% and

10% ripples, respectively. However, in the nineteen-level converter it is increased to 5.82% and 8.37%, respectively. Also, in the modulation without the extra switching, the THD of the output voltage for the fifteen-level converter at 5% and 10% ripples reached to 7.91% and 8.22%, respectively while in the nineteen-level converter were at 6.8% and 8%, respectively. It can be concluded that, even by considering DC link ripple, the THD of the output voltage in the proposed hybrid converter with ADCC is still less than the converter with SDCC configuration either with or without the extra switching modulation techniques.

According to simulation results,

- Using ADCC instead of SDCC in the proposed hybrid cascade converter can generate four more voltage levels in output voltage which leads to better harmonic characteristics with the same number of components and switching.
- By means of the first method of PWM (with extra switching) although better total harmonic distortion can be achieved compared with the second PWM method (without extra switching), extra losses should be paid.
- The effect of extra losses or THD between the first and second method in higher switching frequency is negligible so that it shows the high performance of proposed topology in this switching of such frequencies. However, in low switching frequencies the first or second method of switching could be selected based on different applications.

V. Conclusion

This paper has presented the diode-clamped multilevel H-bridge cell cascaded with three-level conventional inverters to increase efficiency of converters with high output voltage resolution. A novel DC link voltage rating is proposed for the multilevel diode-clamped and three-level H-bridge inverters to improve the output voltage and current quality by preserving the adjacent switching vectors between all voltage levels. The MOB converter has been applied as a DC link supplier of a diode-clamped inverter to boost and regulate the capacitors' voltage to the desired DC link rates. Using the MOB converter, a new cascade inverter is verified by cascading asymmetrical seven-level H-bridge diode-clamped inverter. Nineteen-level performance was achieved, which has more voltage levels as well as lower voltage, and current THD rather than using a symmetrical diode-clamped inverter with the same configuration and equivalent number of power components. Predictive current control was conducted to show the performance of the proposed method. In this case, two different methods for the switching states selection are proposed to minimise either losses or THD of voltage in hybrid converters. Novel H-bridge cascaded cells can decrease the complexity of control and cost of the system as well as diminish or remove the output filters when the configuration will be extended for more H-bridge cells.

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VI. REFERENCES

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