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A Hybrid Discontinuous Voltage Controller for DSTATCOM Applications

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Abstract – This paper proposes a hybrid discontinuous control methodology for a voltage source converter (VSC) based distribution static compensator (DSTATCOM) connected to a 3-phase distribution system. It is assumed that the DSTATCOM controls the point of common coupling (PCC) voltage. An LC output filter is connected at the output of the VSC. With the help of both filter inductor current and filter capacitor voltage control, the voltage across the filter capacitor is controlled. Based on the voltage error, the control is switched between voltage and current control mode. In this scheme, an extra diode state is used that makes the VSC output current discontinuous. This diode state reduces the switching losses because half of the total switching occurs at nearly zero converter current. The effects of different source conditions on voltage at PCC are studied. Voltage angle at PCC is controlled using a PI controller. Simulation studies are performed using PSCAD to validate the efficacy of the proposed controller.

Index Terms – DSTATCOM, discontinuous current, hybrid control, LC output filter.

I. INTRODUCTION

POWER QUALITY is a concern for sensitive loads (consumers) like semiconductor manufacturing plants, hospitals, financial institutes or food processing plants as a voltage dip for even short duration can cost them a substantial amount of money. Most of the power quality problems originate in distribution system. Installation of a distribution static compensator (DSTATCOM) at consumer premises is an effective solution of these problems [1]-[2]. A DSTATCOM is a voltage source converter (VSC) based shunt device, usually supported by short-time energy stored in the dc capacitor(s). Various kinds of structure and control methods are used for compensators [3]. In this paper, voltage at point of common coupling (PCC) is controlled and made balanced so that source current can be balanced, even when the load is unbalanced and nonlinear. To prohibit the switching frequency components of the VSC to the PCC voltage, an LC filter is connected at the output of VSC. A simple hysteresis current control (HCC) will fail to track the capacitor voltage reference. Hence a hybrid discontinuous feedback control law is proposed for the combined VSC-LC filter system.

In this paper, the discussion is based on the structure and control of a DSTATCOM that is suitable to compensate the load at the time of sag or swell in source voltage. Also it can compensate the load at the time of feeder change. To control the power flow from source, voltage angle at PCC is controlled using a PI controller. This angle control gives a jump in voltage angle when compensator is connected to the grid. A solution to avoid this jump is proposed in this paper.

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The control strategy described in this paper uses both voltage and current controls. In voltage control mode modified concept of 3-level HCC is used [4]-[5]. Generally in a 3-level HCC, the output of the inverter is either $+V_{dc}$, 0 or $-V_{dc}$. In the zero state, a short circuit path is provided through inverter. In this paper the zero state is modified by a diode state. In the diode state, all four switches of single phase inverter are turned off. Filter inductor current is made zero with the help of diodes.

II. VOLTAGE CONTROL STRUCTURE

The scheme of DSTATCOM is shown in Fig. 1. In this system, a load that can be active, passive, unbalanced or nonlinear is connected with a balance voltage source (V_s) through a feeder. Resistance and inductance of feeder are R and L . A DSTATCOM that contains a VSC and an LC filter at the output of VSC is used to compensate the load. The VSC is supplied by the dc storage capacitor C_{dc} . The LC filter inductance and capacitance are denoted by L_f and C_f respectively and the resistance R_f indicates the circuit losses. It can be seen from Fig. 1 that the voltage across the filter capacitor C_f is the PCC voltage v_t . The aim of this scheme is to balance the three phase PCC voltages.

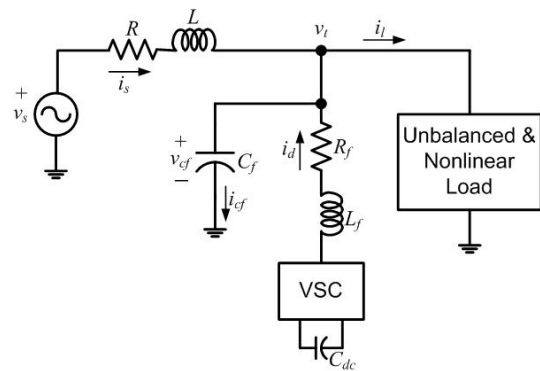


Fig. 1. Single-line diagram of shunt compensation of a load through a feeder.

A. The DSTATCOM model

Fig. 2 shows the structure of DSTATCOM. It contains three H-Bridge VSCs. All three VSCs are connected to common DC storage capacitor C_{dc} . Each VSC is connected to grid through single phase transformer and a capacitor. The three single phase transformers are used to provide isolation [2]. Leakage inductance of transformer L_f and the filter capacitor C_f constitute the LC filter for each phase. All three transformers are connected in star and neutral point is connected to the neutral of the load or it may be grounded if neutral point of load is not available.

As far as structure of single phase converter is concern, it has four switches with anti-parallel freewheeling diode. In the

later part of this paper, we shall see that output current of the converter, i.e., filter inductor current may be discontinuous. So the diodes' rating must be same as the IGBTs' rating.

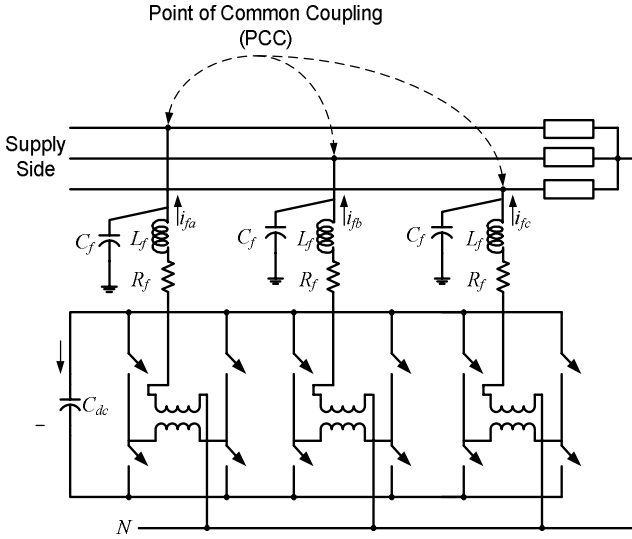


Fig. 2. Compensator structure used in which three separate VSCs are supplied from a common dc storage capacitor.

B. The Reference generation

The aim the scheme is to balance the PCC voltages. Note that the compensator (DSTATCOM) is supplied by a dc storage capacitor, which can only provide temporary ride through during transients. Hence the power demanded by the load and the losses in the compensation circuit must be supplied by the source. The voltage angle at PCC – δ is set in such a manner that the source supplies the total power and loss requirements.

Let us define

$$V_s = V_1 \angle 0^\circ \text{ and } V_l = V_2 \angle -\delta \quad (1)$$

Then from Fig. 1, we get the following expression for the power entering the PCC from the source

$$P = \frac{V_2}{R^2 + X^2} [R(V_1 \cos \delta - V_2) + XV_1 \sin \delta] \quad (2)$$

where $X = \omega L$. If $V_1 \approx V_2$, the first term inside the bracket on the right hand side of (2) is negative. However, its influence on the positive valued second term is negligible as $R \ll X$. Now suppose a voltage sags occurs causing V_1 to drop. If the DSTATCOM holds V_2 constant, the first term becomes more negative. Let us stipulate that the power to the load must remain unchanged. Hence δ must increase not only to offset the first term, but also to maintain the power flow constant. Similarly during a voltage swell in V_1 , the angle δ must reduce in order to hold the power constant.

For example, let us assume that $V_1 = V_2 = 11$ kV (L-L), $R = 6.05 \Omega$, $X = 36.2854 \Omega$ and $\delta = 20^\circ$. Then the three-phase power, calculated from (2) is 1.077 MW. Now suppose a symmetrical sag in supply voltage reduces V_1 to 9 kV (L-L). Then in order to maintain the power flow constant, δ must be equal to 27.5° . Similarly if V_1 becomes 12 kV (L-L), δ should be around 17.3° to hold the power constant.

Therefore in order to keep the power constant, δ must be controlled. If the power flow is constant, the dc capacitor voltage V_{dc} remains constant since it is absorbing the required amount of power to replenish the losses. A drop in the capacitor voltage indicates as voltage sag as it tries to supply power to the load. The capacitor voltage increases during a voltage swell as the increased power from the source is drawn by the DSTATCOM. Therefore the power drawn from the source can be controlled by regulating the capacitor voltage around its reference value. This gives the following capacitor voltage control loop

$$\delta = K_p e + K_I \int e dt \quad (3)$$

where $e = V_{cref} - V_{dc}$, V_{cref} being reference voltage for the dc capacitor. Using this δ and reference peak voltage at PCC (V_{2m}), three phase reference voltages are generated for voltage controller. These references are

$$\left. \begin{aligned} v_{aref} &= V_{2m} \sin(\omega t - \delta) \\ v_{bref} &= V_{2m} \sin(\omega t - \delta - 120^\circ) \\ v_{cref} &= V_{2m} \sin(\omega t - \delta + 120^\circ) \end{aligned} \right\} \quad (4)$$

With the help of voltage controller, the voltage at the PCC is kept balanced.

III. STRATEGY FOR HYBRID DISCONTINUOUS CONTROL

If our source voltages are balanced sinusoids and we make PCC voltage also balance then source current will also be balance. The harmonic and unbalanced components of the load currents will be supplied by compensator. However any unbalance or distortion in the source voltages will be reflected in the source currents since the PCC voltages will remain balanced sinusoidal. In this section, we shall introduce a new control methodology to track the PCC voltage references (4). This control requires fewer of switching events, thereby incurring lower switching losses compared to hysteretic control.

This control is a combination of voltage and current control in which all the three states (+ 1, - 1 and 0) of inverter are used. In + 1 and - 1 states, the output voltages of inverter are $+ V_{dc}$ and $- V_{dc}$ respectively and the 0-state is the diode state where all four switches are turned off. In the diode state, with the help of diode, the inductor current is forced to zero. This state introduces discontinuity in the converter output current.

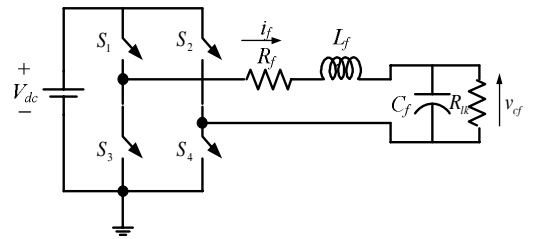


Fig. 3. VSC scheme to control capacitor voltage.

Let us consider a single phase H-bridge converter with an LC filter as shown in Fig. 3. The leakage in the capacitor is denoted by a high resistance R_{lk} . It is desired that the VSC

tracks a reference capacitor voltage with the help of current and voltage control. For this, two zones are defined as shown in Fig. 4. If capacitor voltage is in Zone 1, the VSC is operated in current control mode and if the voltage is in Zone 2 then it is operated in voltage control mode. Both these variables are controlled in hysteresis bands. In Zone 1, a hysteresis band limit is set for the inductor current (i_f) and in Zone 2, hysteresis band is set for the capacitor voltage (v_{cf}).

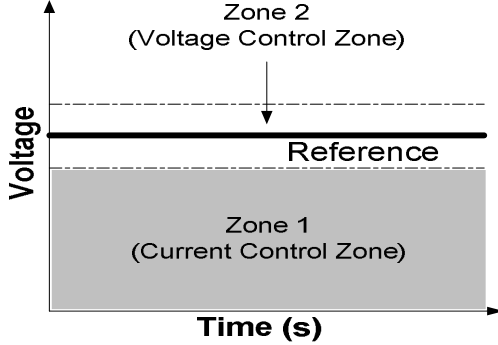


Fig. 4. Two zones for voltage control.

DC Voltage Tracking: If the reference of the capacitor voltage is positive, then switching in Zone 1 will be defined as

$$\text{If } i_f \geq h_i \text{ then } S_{1-4} = 0 \quad (5)$$

where h_i is the current hysteresis band. This implies that if the current i_f is greater than or equal to h_i , turn all the switches off. However, if this current is less than zero, apply positive voltage at the VSC output, i.e.,

$$\text{If } i_f < 0 \text{ then } S_{1,4} = +1 \text{ and } S_{2,3} = 0 \quad (6)$$

Let the upper and lower voltage hysteresis bands be denoted by h_{uv} and h_{lv} respectively. Then for Zone 2, we have the following switching logic

$$\text{If } v_{cf} \geq v_{ref} + h_{uv} \text{ then } S_{1-4} = 0 \quad (7)$$

$$\text{If } v_{cf} \leq v_{ref} - h_{lv} \text{ then } S_{1,4} = +1 \text{ and } S_{2,3} = 0 \quad (8)$$

For example, let assume $v_{ref} = 8$ kV (dc), $h_i = 0.4$ kA, $h_{uv} = 0.02$ kV and $h_{lv} = 0.1$ kV. Value of h_{uv} should be less than h_{lv} because even if all four switches are turned off, the capacitor voltage increase until i_f becomes zero and the capacitor voltage becomes more than $v_{ref} + h_{uv}$. If h_{uv} and h_{lv} are same, a steady state error will always be there. To eliminate this error h_{uv} should be less than h_{lv} . Fig. 5 shows the tracking of capacitor voltage when v_{ref} is positive. It can be seen that that when the voltage rises to its reference, the control is in Zone 1, where the current is switched rapidly. Once the voltage reaches the reference value, the control is switched to zone 2 to maintain the output voltage. During this time, the current switching will be dependent on the leakage resistance of the capacitor. If the resistance is small, the leakage will be more, resulting in higher current switching. The same scheme can also be applied when v_{ref} is negative. This is not shown here.

AC Voltage Tracking: To track a sinusoidal capacitor voltage reference, one cycle is divided in four parts as shown in

Fig. 6. Regions 1 and 3 can be tracked using the switching schemes explained above. However for Regions 2 and 4 separate switching scheme needs to be implemented because the capacitor discharges in these regions.

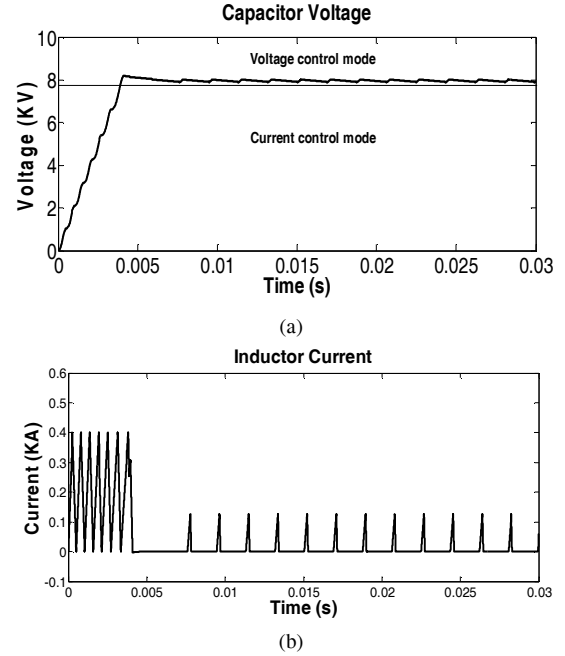


Fig. 5. (a) Capacitor voltage and (b) Inductor current during DC tracking.

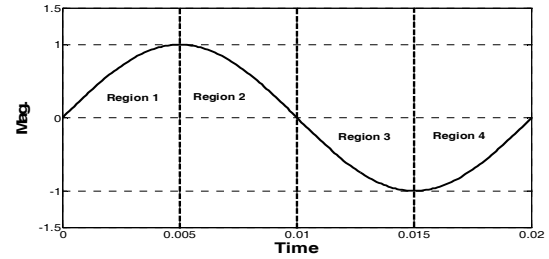


Fig. 6. Four regions of one cycle of a sinusoidal wave.

Two zones are also defined for Regions 2 and 4 – one for current control and the other for voltage control. For Region 2, switching in Zone 1 is

$$\text{If } i_f \geq 0 \text{ then } S_{2,3} = +1 \text{ and } S_{1,4} = 0 \quad (9)$$

$$\text{If } i_f \leq h_i \text{ then } S_{1-4} = 0 \quad (10)$$

The switching for Zone 2 are

$$\text{If } v_{cf} \geq v_{ref} + h_{lv} \text{ then } S_{2,3} = 1 \text{ and } S_{1,4} = 0 \quad (11)$$

$$\text{If } v_{cf} \leq v_{ref} - h_{uv} \text{ then } S_{1-4} = 0 \quad (12)$$

Fig. 7 shows the sinusoidal tracking of capacitor voltage and inductor current. The tracking is discontinuous in nature.

Example 1: In this example, a passive load is connected to the VSC through an LC filter. For a passive load, a diode state is required for all the regions shown in Fig. 6. In Regions 1 and 4, only $+V_{dc}$ is required, while in Regions 2 and 3, only $-V_{dc}$ is required. Note that there is no need to utilize $-V_{dc}$ in Regions 1 and 4 and $+V_{dc}$ in Regions 2 and 3 (load should not provide rapid discharging path to capacitor). Hence the

scheme described above produces very accurate tracking. However when the load is active or when a passive load provide a rapid discharging path for the capacitor, the $-V_{dc}$ state may also be required in Regions 1 and 4 while the $+V_{dc}$ state may be required in Regions 2 and 3 depending on the relative phase difference between the VSC output voltage and the system internal emf. This may increase the switching frequency of the VSC and lead to continuous conduction mode of the inductor current. Fig. 8 shows the load voltage and inductor current for a passive load.

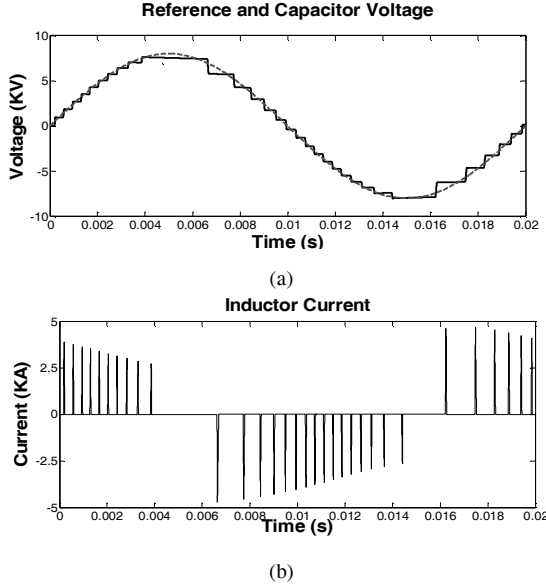


Fig. 7. (a)Capacitor voltage and (b) Inductor current for AC voltage tracking.

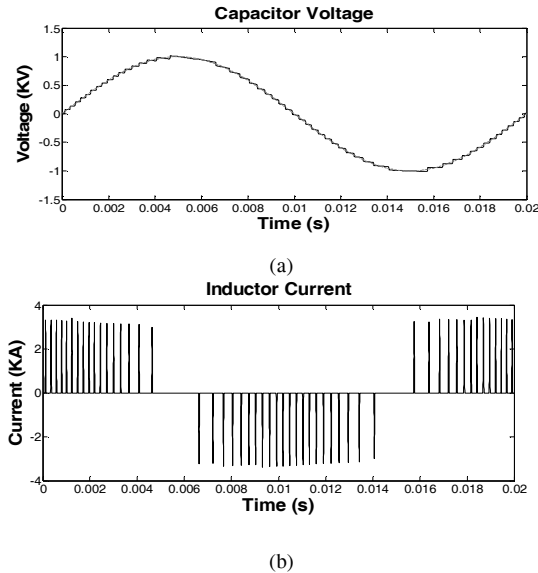


Fig. 8. (a) Capacitor voltage and (b) Inductor current for Example 1

For tracking in Region 1 with an active load, the switching control is defined as follows. If capacitor voltage is in Zone 1, then

$$\text{If } v_{cf} \geq h_i \text{ then } S_{1-4} = 0 \quad (13)$$

$$\text{If } i_f < 0 \text{ then } S_{1,4} = 1 \text{ and } S_{2,3} = 0 \quad (14)$$

But if the capacitor voltage is in Zone 2, then

$$\text{If } v_{cf} \leq v_{ref} - h_{lv} \text{ then } S_{1,4} = 1 \text{ and } S_{2,3} = 0 \quad (15)$$

$$\text{If } v_{cf} > v_{ref} - h_{lv} \text{ and } v_{cf} < v_{ref} + h_{uv} \text{ then } S_{1-4} = 0 \quad (16)$$

$$\text{If } v_{cf} \geq v_{ref} + h_{uv} \text{ then } S_{1,4} = 0 \text{ and } S_{2,3} = 1 \quad (17)$$

The switching for Region 3 will be the same as above except that $-V_{dc}$ state will be chosen instead of $+V_{dc}$ state.

The switching for Region 2 is defined as follows. Switching in Zone 1 is

$$\text{If } i_f \geq 0 \text{ then } S_{2,3} = 1 \text{ and } S_{1,4} = 0 \quad (18)$$

$$\text{If } i_f \leq h_i \text{ then } S_{1-4} = 0 \quad (19)$$

For Zone 2,

$$\text{If } v_{cf} \geq v_{ref} + h_{lv} \text{ then } S_{2,3} = 1 \text{ and } S_{1,4} = 0 \quad (20)$$

$$\text{If } v_{cf} < v_{ref} + h_{lv} \text{ and } v_{cf} > v_{ref} - h_{uv} \text{ then } S_{1-4} = 0 \quad (21)$$

$$\text{If } v_{cf} \leq v_{ref} - h_{uv} \text{ then } S_{2,3} = 0 \text{ and } S_{1,4} = 1 \quad (22)$$

Switching for Region 4 can be obtain in the same way as in Region 2, the only difference being the capacitor discharges from negative to zero instead of positive to zero.

IV. COMPENSATOR PERFORMANCE

Once the reference for PCC voltage is computed from (4), the PCC voltage can be tracked using the controller described in Section III. This is illustrated with the help of the following example.

Example 2: Consider the system shown in Fig. 1. The system and DSTATCOM parameters chosen are given in Table I. It is assumed that the source voltage is balanced. The load is both unbalanced (passive RL) and nonlinear (three-phase rectifier supplying an RL). The compensator is connected to grid at time $t = 0$.

TABLE I. SYSTEM PARAMETERS

System Quantities	Values
Systems Frequency (ω)	100π rad/s (50 Hz)
Source voltage (V_s)	11 kV rms (L-L)
Feeder impedance ($R_f + jX_f$)	$6.05 + j36.26 \Omega$
Unbalanced Load	
The subscripts a , b and c denote the three phases.	$Z_{la} = 48.2 + j94.2 \Omega$ $Z_{lb} = 12.2 + j31.4 \Omega$ $Z_{lc} = 24.2 + j60.47 \Omega$
Nonlinear Load	
Contains a three-phase rectifier that supplies	$100 + j31.4 \Omega$
DSTATCOM	
Loss (R_f)	3Ω
Filter capacitor (C_f)	$50 \mu\text{F}$
Three single-phase transformers are rated at	1 MVA, 3 kV/11 kV, leakage inductance (L_f) of 2.5%
Capacitor Control Loop	
DC capacitor	$10000 \mu\text{F}$
Reference voltage (v_{cref})	3.5 kV
Proportional gain (K_p)	-0.7
Integral gain (K_I)	0.1

The source currents, load currents, PCC voltages and the angle of the PCC voltage are shown in Figs. 9 (a-d) respectively. The initial transient lasts about 0.1 s. During this time, the dc capacitor charges. Once the dc capacitor voltage

reaches its desired level, the angle of the PCC voltage settles to its steady state level and the initial transient dies out. This is evident from all the plots of Fig. 9.

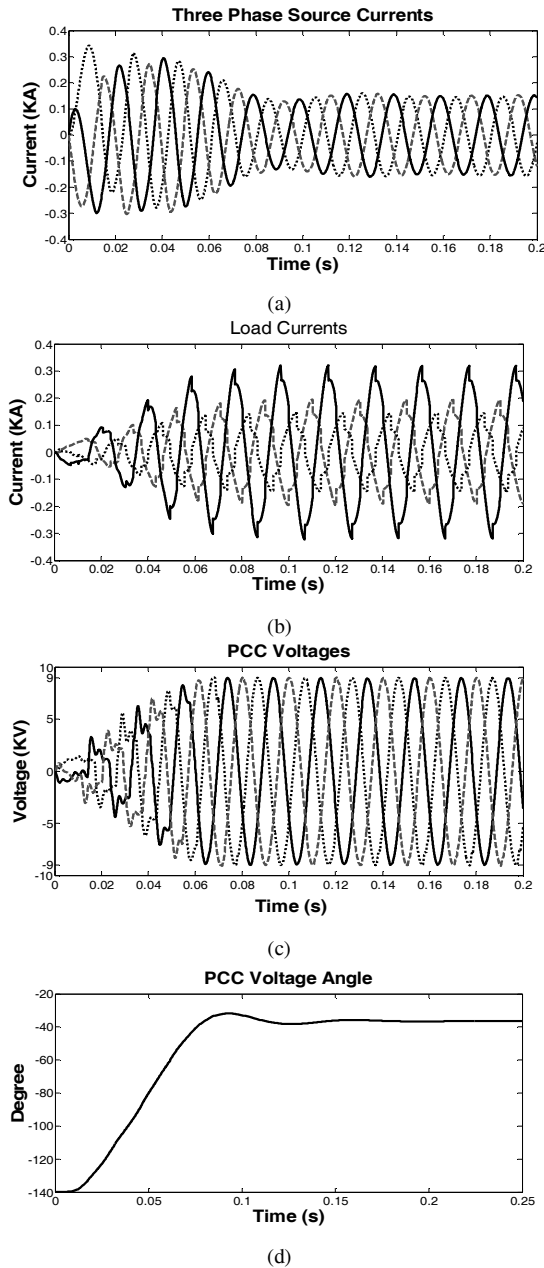


Fig. 9. Compensation of the unbalanced nonlinear load without precharged capacitor.

Once the load and the compensator are connected to the grid at time $t = 0$, the PCC voltage angle starts changing as shown in Fig. 9 (d). This angle changes significantly in the transient period. Such a rapid change in angle may not be desirable to some loads. To overcome this problem, the dc capacitor should be pre-charged before connecting the DSTATCOM to the grid. To charge the dc capacitor, the same VSC that is used as the compensator is used. At the time of pre-charging, the controller is switched off and anti-parallel diodes of the VSC are used as an un-controlled rectifier. This pre-charging scheme is shown in Fig. 10, which contains two circuit breakers. The load is connected to the grid through the circuit breakers CB1 and filter capacitor is connected to the

rest of the DSTATCOM through CB2. Initially controller is switched off to charge the dc capacitor. During this time, CB1 and CB2 are kept open. To limit the charging current of dc capacitor a resistance is connected in series with dc capacitor. Once the capacitor voltage reaches the desired value, the series resistance is bypassed (short-circuited) with the help of switch SC1 and CB1 and CB2 are closed subsequently.

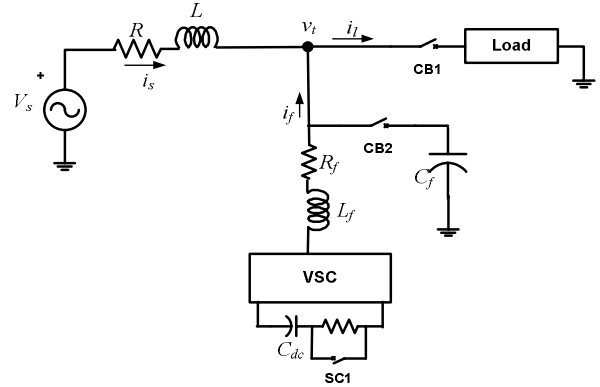
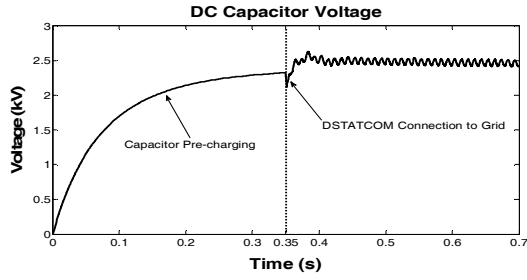


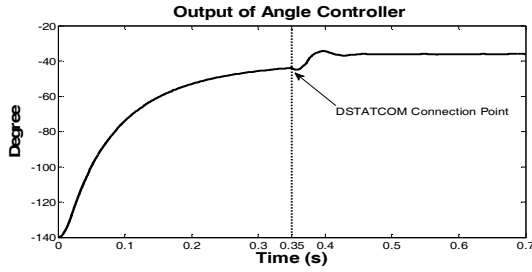
Fig. 10. Schematic diagram of the compensation scheme to pre-charge the dc capacitor.

Using the above pre-charging scheme, capacitor is charged for initial 0.35 s and during this time CB1, CB2 and switch SC1 is kept open. It can be seen from the dc capacitor voltage of Fig. 11 (a) that the capacitor voltage attains a near steady state value at $t = 0.35$ s and hence further pre-charging is not possible. However once CB1, CB2 and SC1 are closed, the capacitor voltage and PCC voltage angle settle quickly without deviating much from their pre-charged values as evident from Fig. 11 (a) and (b). During the charging, phase-a of the PCC voltage is shown in Fig. 11 (c). It can be seen that this voltage does not collapse during this period. Hence, the loads that may be connected upstream from the PCC will not get affected much. Also note that the output of the angle controller (3) changes rapidly from -140° towards its steady state value due to the controlled charging of the dc capacitor. However since the PCC voltage is not controlled by the DSTATCOM during the pre-charging time, the angle change does not have any effect on the load or the PCC voltage. Once the breakers CB1 and CB2 are closed, the load currents start flowing (Fig. 11 d) and the PCC voltages quickly attain its steady state magnitude (Fig. 11 c). The advantage of this pre-charging method is that it does not require any extra hardware other than the switch SC1 and the resistor connected in series with the dc capacitor. The presence of the resistor will increase losses. However it will not have much consequence since the charging time is very small.

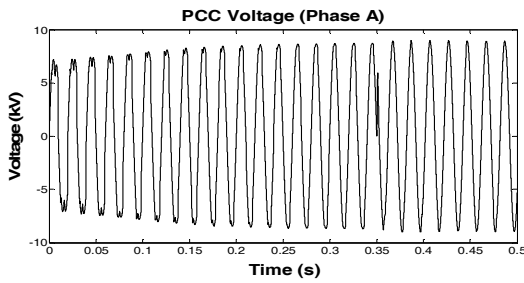
Example 3: To investigate the behavior of the controller at the time of a voltage sag in the source voltage, let us consider the same system as given in Table I. A voltage sag occurs at $t = 0.25$ sec in which the source voltage drops to 7 kV (L-N, peak) from the nominal value of 9 kV. The sag is removed at $t = 0.45$ sec. It is desired that the PCC voltage is maintained at 8 kV (L-N, peak). The three-phase PCC voltage is shown in Fig. 12 (a). It can be seen from this figure that there is no appreciable change in the magnitude of the PCC voltage during the sag or its removal. From (2), it is clear that if source voltage



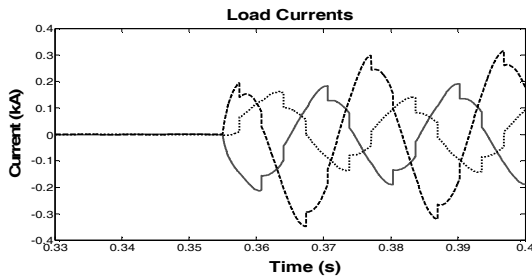
(a)



(b)



(c)

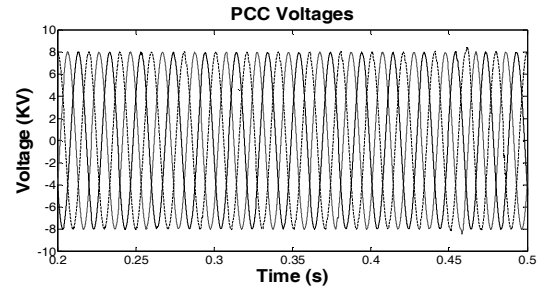


(d)

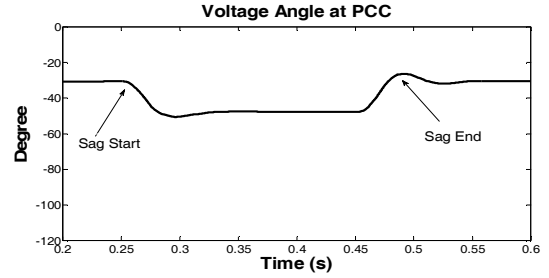
Fig. 11. (a) DC capacitor voltage, (b) voltage angle at PCC, (c) PCC voltage and (d) load currents when the dc capacitor is pre-charged.

reduces then δ should increase to maintain the same level of power flow. Fig. 12 (b) shows the PCC voltage angle. It starts decreasing at $t = 0.25$ s, resulting in increase in δ . The angle returns to its original value once the sag is removed. The three-phase source currents are shown in Fig. 12 (c). It can be seen these currents increase during the voltage sag to maintain the constant amount of power flow.

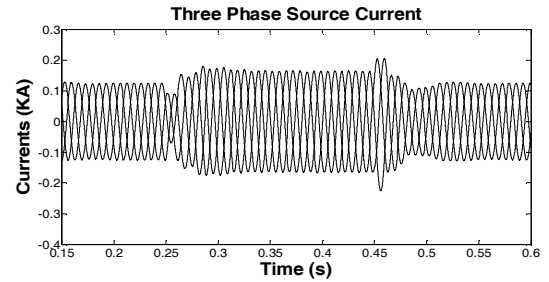
Example 4: The behavior of the system is investigated for a swell in the source voltage, which occurs at $t = 0.25$ s. The swell is removed at $t = 0.45$ s. The same system as given in Table I is considered here also. During the swell, the source voltage rises to 11 kV (L-N, peak). It can be seen from Fig 13 that magnitude of PCC voltage remains constant while its angle increases to maintain constant power flow.



(a)

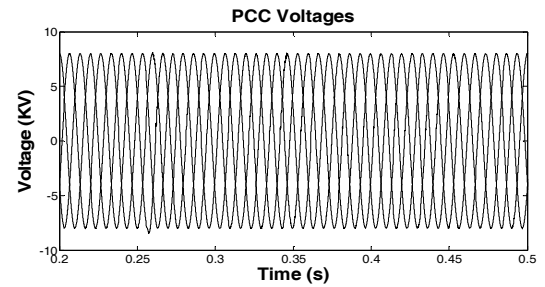


(b)

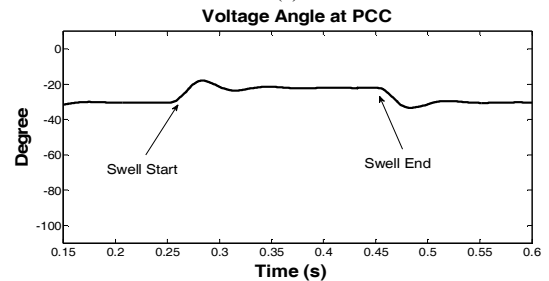


(c)

Fig. 12. (a) PCC voltages, (b) voltage angle and (c) source currents for Example 3.



(a)



(b)

Fig. 13. (a) PCC voltages and (b) voltage angle for Example 4.

Example 5: Unsymmetrical sag/swell is a common occurrence in power systems. In this example, we shall investigate the system behavior during such an occurrence. Let us consider the same system as given in Table I. However the peak

of the instantaneous source voltages are changed as 10kV, 9kV and 8kV (L-N, peak) for the phases a, b and c respectively at $t = 0.3$ s and 8kV, 9kV and 10kV (L-N, peak) for the phases a, b and c respectively at $t = 0.5$ sec. It is desired that the DSTATCOM maintains the peak of the PCC voltage at 9 kV. These voltages are shown in Fig. 14 (a). The PCC voltage angle is shown in Fig. 14 (b). It can be seen that it almost remains unchanged. Since the PCC voltages are held constant, the power requirement of the load remains unchanged. Also since the changes in the source voltages are symmetrical (the dip in one phase is equal to the rise in the other), the angle must remain constant for constant power. The source currents are shown in Fig. 14 (c). It can be seen that they are unbalanced in sympathy with the source voltages.

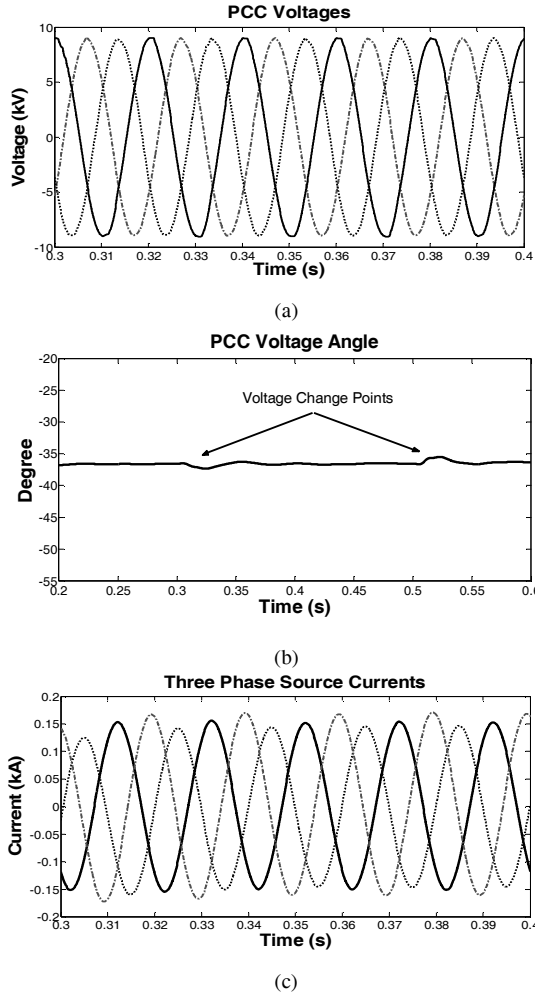


Fig. 14. (a) PCC voltages (b) voltage angle (c) and source currents for Example 5.

Example 6: Let us now consider the case when there is a change in the feeder impedance. To investigate this case, the system in Table I is altered by introducing a 3-phase phase rectifier that is connected half between the source and the PCC as shown in Fig. 15. This load is connected to the feeder through a circuit breaker (CB1), which is closed at time $t = 0.3$ s. The results are shown in Fig. 16. With the introduction of the rectifier load, some amount of power is supplied by the source to it. However since the load power has to remain constant, the PCC voltage angle must recede to maintain the power flow to the load. This is evident from Fig. 16 (a). The

magnitude of the PCC voltage remains constant as evident from Fig. 16 (b). However the currents (i_s) supplied by the source are now distorted, but balanced due to the rectifier load as shown in Fig. 16 (c).

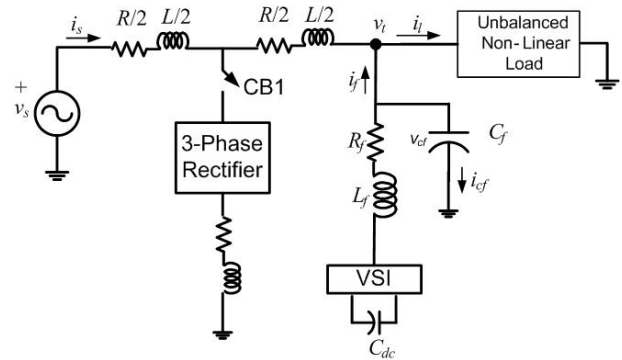


Fig. 15 PCC Feeder switching scheme for Example 6

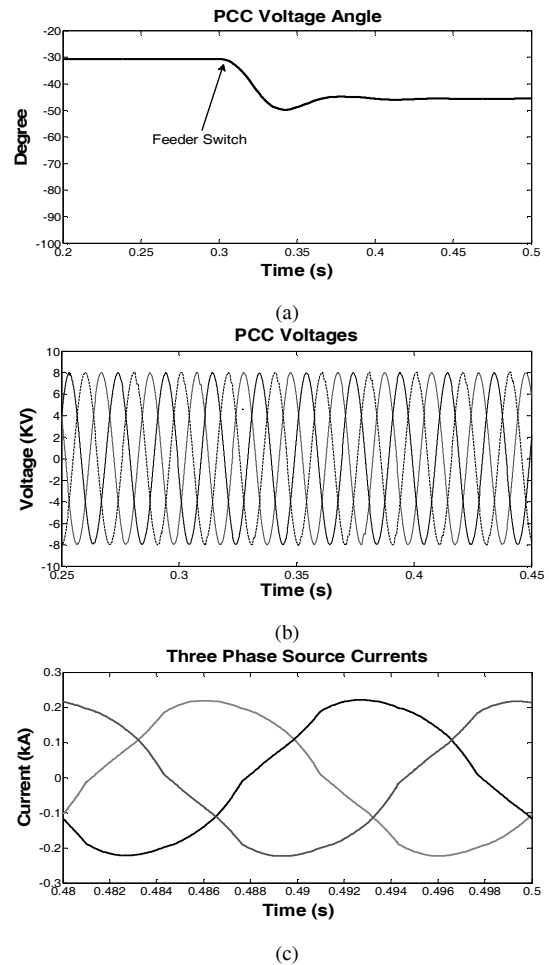


Fig. 16 (a) PCC voltage angle, (b) PCC voltages and (c) source currents for Example 6.

V. CONCLUSIONS

This paper presents a new switching control strategy for voltage control in the presence of an LC filter. The use of the LC filter removes the effects of switching frequency components on the output voltage better than the traditional L filter. However a simple hysteric band control is not suitable in this situation as it will lead to instability. To overcome this

situation, a discontinuous hybrid control strategy is proposed here which reduces the switching losses. Due to the use of the diode state, half of the switching events occur when the inverter current is zero or nearly zero, which makes half of the switching lossless. Because of this advantage, a higher switching frequency can be chosen, which will result in better tracking of higher frequency waveforms. Alternatively, the size of the inverter can be reduced.

This improved control strategy has been applied to a DSTATCOM operating in a voltage control mode. The advantage of the proposed control method is that it is robust to LC parameter variations and does not need a redesign for the changes in the remainder of the power system, DSTATCOM parameters and operating conditions. It has been shown that the DSTATCOM is able to hold the PCC voltage constant in the face of various system disturbances and load changes. A simple angle control has been used for the DSTATCOM and a pre-charging scheme to avoid a phase jump has been designed.

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