State Feedback Control of Multilevel Inverters for DSTATCOM Applications

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***Abstract*—In this paper, load compensation using multilevel inverter-based distribution static compensator (DSTATCOM) is presented. The DSTATCOM is connected to a three-phase four-wire (3p4w) distribution system. Two different multilevel inverter topologies are used to realize the DSTATCOM. They are diode-clamped multilevel inverter (DCMLI) and flying capacitor multilevel inverter (FCMLI). A compensating technique has been derived, which uses the state feedback control to the multilevel inverters-based DSTATCOMs. A switching strategy for the multilevel inverters that ensures utilization of all output voltage states of the inverter for efficient tracking of references has been proposed. The schemes of dc-link capacitor voltage control for DCMLI and flying capacitor voltage control for FCMLI have been discussed. Comparative studies of performances of the two DSTATCOM topologies are performed. The simulation studies are performed using PSCAD/EMTDC to validate the efficacy of the proposed control scheme.**

***Index Terms*—Diode-clamped multilevel inverter (DCMLI), distribution static compensator (DSTATCOM), flying capacitor multilevel inverter (FCMLI), switching control.**

I. Introduction

A DISTRIBUTION static compensator (DSTATCOM) is a voltage-source converter (VSC)-based shunt device, usually supported by short-time energy stored in the dc capacitor(s) [1]. The task of the DSTATCOM is to filter out the unbalances and distortions in the source currents caused by the loads and at the same time forcing the source to work at a desired power factor. For these tasks, it is preferable to perform faster switching actions (such as the hysteresis current control) to have a fast dynamic response, improved robustness, simplicity and a continuously spread harmonic spectrum [1]–[3]. For medium to high voltage applications and to meet the current and voltage harmonic distortion standards imposed on the line side, recent trends are to use multilevel inverters to realize the DSTATCOM [3]–[10]. The advantages of multilevel inverters are smaller filter size, lower switching losses, lower electromagnetic interference, lower voltage stress of power semiconductors and lower acoustic noise. These can eliminate the need of interconnecting transformer [4]. Besides, a multilevel compensator, in comparison with its two level counterparts, makes more exact formation of the compensating currents possible. It also has better properties under sudden changes of load making these topologies attractive for continuous control of system dynamic behavior and to reduce power quality problems [3]–[14]. Multilevel inverters are generally classified as diode-clamped multilevel inverter (DCMLI), cascade H-bridge inverter and flying capacitor multilevel inverter (FCMLI). Their applications in shunt compensations of distribution systems have been reported in [3]–[10]. All of these carry an implicit assumption that the source is stiff (i.e., the voltage at the point of common coupling (PCC) is tightly regulated and cannot be influenced by the currents injected by the shunt device). This, however, is not a valid assumption and the compensator performance degrades considerably with high impedance ac supplies (i.e., with non-stiff sources) if the same shunt algorithms used in these are applied [1]. The cascade topology is traditionally used and recommended for slow switching frequency applications (switching at the fundamental frequency of the power system). As the number of levels increases and at high switching frequencies, it faces difficulty in controlling dc-link voltages and is not very well suited as a DSTATCOM [4]–[8]. The dc-link voltage controls of FCMLI and DCMLI at high switching frequencies are relatively simpler and have been reported in [3] and [9]–[13].

This paper proposes the design of a state feedback switching controller for a five-level inverter-based DSTATCOM. The state feedback switching controller uses linear quadratic regulator (LQR) design that tracks the reference state trajectories. It is assumed that the DSTATCOM is connected to a system having balanced source supplying an unbalanced and nonlinear load through a long feeder. In this paper, two different DSTATCOM structures are considered—one based on FCMLI and the other based on DCMLI. A comparative study of their performances has been presented when the DSTATCOMs, in conjunction with a feeder side filter capacitor, are used for improving the power quality of the distribution system. The other aspects of the proposal are having balanced dc-link voltages for the DCMLI and balanced flying capacitor voltages for the FCMLI, while ensuring the desired tracking using the proposed switching control scheme.

II. Multilevel VSCs Circuit Configurations

For the transformerless DSTATCOMs considered in this paper, higher-level inverter structure may be required to meet the desired voltage profile at the PCC and to have good quality outputs. Unfortunately, the number of achievable voltage levels is limited due to circuit layout, cost and packaging constraints [4]. In this paper, the five-level inverter configurations have been considered.

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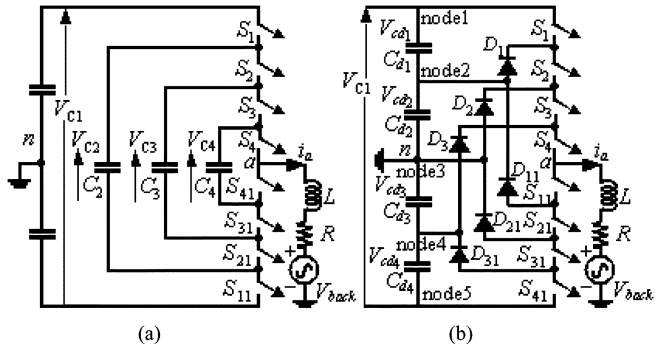

Fig. 1. Five-level inverter leg. (a) FCMLI. (b) DCMLI.

TABLE I
SWITCHING SCHEME FOR ONE PHASE LEG OF A FIVE-LEVEL FCMLI

S_1	S_2	S_3	S_4	S_{41}	S_{31}	S_{21}	S_{11}	C_2	C_3	C_4	V_{an}
1	1	1	1	0	0	0	0	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	1	0	0	0	NC	NC	+	$+V_{dc}/4$
1	1	0	1	0	1	0	0	NC	+	−	
1	0	1	1	0	0	1	0	+	−	NC	
0	1	1	1	0	0	0	1	−	NC	NC	
0	0	1	1	0	0	1	1	NC	−	NC	0
0	1	0	1	0	1	0	1	−	+	−	
0	1	1	0	1	0	0	1	−	NC	+	
1	0	0	1	0	1	1	0	+	NC	−	
1	0	1	0	1	0	1	0	+	−	+	
1	1	0	0	1	1	0	0	NC	+	NC	
1	0	0	0	1	1	1	0	+	NC	NC	$-V_{dc}/4$
0	1	0	0	1	1	0	1	−	+	NC	
0	0	1	0	1	0	1	1	NC	−	+	
0	0	0	1	0	1	1	1	NC	NC	−	
0	0	0	0	1	1	1	1	NC	NC	NC	$-V_{dc}/2$

A. Flying Capacitor Multilevel Inverter

Fig. 1(a) shows the schematic of one leg of a three-phase five-level FCMLI. Here, each switch consists of a power semiconductor switching device with an antiparallel diode. The switches S_{11} to S_{41} are complementary of S_1 to S_4, respectively. V_{C1} is the dc-link voltage and V_{C2}, V_{C3}, and V_{C4} are flying capacitor voltages, regulated using a control scheme at $3V_{C1}/4$, $V_{C1}/2$, and $V_{C1}/4$, respectively, to clamp each device voltage stress at $V_{C1}/4$. Table I lists the switch combinations used to synthesize five output voltage levels (V_{an}) and the corresponding states of the flying capacitors for $V_{C1} = V_{dc}$. Charging a capacitor is indicated by $+$, the discharging by $-$, while "NC" indicates neither charging nor discharging. The given switch states are for the outgoing direction of the current waveform (i_a in Fig. 1). The states ($+$ and $-$) will reverse for the incoming current. It can be seen from Table I that the structure offers multiple switch combinations for $V_{an} = V_{dc}/4$, 0 and $-V_{dc}/4$. As such redundancies are available, one can choose a preferential switching state for these output voltage levels that will help to maintain the capacitor voltages constant. The operation and structure details of FCMLI can be found in [3] and [9]–[11].

B. Diode-Clamped Multilevel Inverter

Fig. 1(b) shows the schematic of one leg of a three-phase five-level DCMLI. In this structure, the complementary switch pairs (S_1, S_{11}), (S_2, S_{21}), (S_3, S_{31}), and (S_4, S_{41}) are placed differently as compared to that in FCMLI. V_{C1} is the dc-link voltage and D_1 to D_{31} are diodes used for clamping each device voltage stress at $V_{C1}/4$. An n-level DCMLI requires $(n-1)$ capacitors on the dc bus, as is evident from the figure. Table II lists the switch states of the five output voltage levels. The DCMLI structure has an inherent unbalancing problem among its dc-link capacitors. This is because, net mean nonzero currents flow from nodes 2 and 4 in Fig. 1(b) for a five-level DCMLI, resulting in the asymmetry between the charging and discharging time of dc capacitors. The detailed description of this phenomenon and other structural and operational details of DCMLI can be found in [4] and [12]–[14]. With the advent of a number of dc capacitor voltage control schemes, the use of DCMLI is not behind that of other multilevel inverters in most of the applications. This is because it has some of the desirable features such as: 1) its dc capacitors can be easily precharged as a group, 2) its switching control is easiest, and 3) the protection circuit required in DCMLI is least complex compared to that in other multilevel inverters, etc. [4], [14].

TABLE II
SWITCHING SCHEME FOR ONE PHASE LEG OF A FIVE-LEVEL DCMLI

S_1	S_2	S_3	S_4	S_{41}	S_{31}	S_{21}	S_{11}	V_{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	0	0	0	1	$+V_{dc}/4$
0	0	1	1	0	0	1	1	0
0	0	0	1	0	1	1	1	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

III. DSTATCOM FOR NONSTIFF SOURCES

A. Compensated Distribution System Structure

The single line diagram of the 3p4w distribution system under study is shown in Fig. 2. In this system, an unbalanced and nonlinear load is supplied by a balanced voltage source (v_s) through a feeder of impedance $R_S + j\omega L_S$. The load is compensated by a DSTATCOM based on one of the two inverters shown in Fig. 1 and its neutral point (n, Fig. 1) is clamped to the neutral of the distribution system. The neutral-clamped configuration has been considered in this paper as it allows three independent current injections. Further, if the inverter output is able to meet the voltage profile at the PCC, the neutral-clamped inverter can be connected without a transformer [16]. However, the configuration used in [1], necessarily requires transformer(s). In Fig. 2, L_f is an additional external inductance that serves as a voltage harmonic attenuator to attenuate the high-frequency voltage harmonics that the DSTATCOM generates [6] and R_f is its resistance. The inductor L_f is mandatory for supporting a difference in instantaneous voltage between the PCC and the ac terminals of the inverter to allow a finite power exchange between the inverter and the distribution system. Here, it is assumed that the inverter provides sufficient voltage level to eliminate the need of connecting transformers. A filter capacitor (C_f) is connected to the PCC to provide a path for the harmonic currents generated due to switchings, the design considerations of which can be found in [16]. The DSTATCOM is operated to balance the

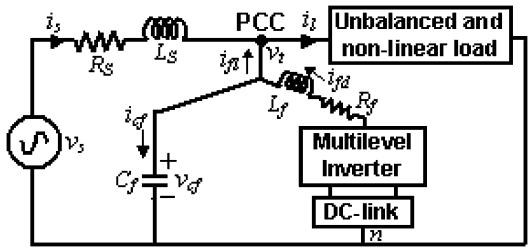

Fig. 2. Single line diagram of a DSTATCOM compensated distribution system.

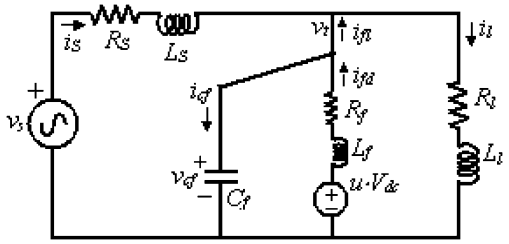

Fig. 3. Equivalent circuit of a DSTATCOM compensated distributed system.

source current i_s by injecting i_{fl} to cancel the harmonic component in i_l.

B. State Feedback Control

In this subsection, the control design is presented for the compensated system shown in Fig. 2, the equivalent circuit of which is shown in Fig. 3. Here, the nonlinear load is neglected and the load is represented by R_l and L_l. V_{dc} is the dc-link voltage and u is a switching function generated through feedback control. For a five-level inverter, u can attain five values (i.e., $-1/2$, $-1/4$, 0, $+1/4$, and $+1/2$, corresponding to the five output voltage levels of the inverter ($-V_{dc}/2$, $-V_{dc}/4$, 0, $+V_{dc}/4$, and $+V_{dc}/2$). Defining a state vector as

$$x^T = [\, i_{fl} \quad i_{cf} \quad v_{cf} \quad i_l \,] \tag{1}$$

the system can be written as [1]

$$\dot{x} = Ax + Bv_s + Cu_c \tag{2}$$

where u_c is the continuous time control law from which the switching control u is generated. Assuming that we have full control over u_c, an infinite time linear quadratic regulator (LQR) is designed with its control law defined as

$$u_c = -K(x - x_{ref}) \tag{3}$$

where x_{ref} is the desired state vector. In an LQR problem, a performance index J is chosen as

$$J = \int_0^\infty \{(x - x_{ref})^T Q(x - x_{ref}) + u_c^T r u_c\} dt \tag{4}$$

where Q and r are the weighting matrices that serve as design parameters [17]. J is then minimized to obtain the optimal control law u_c. This problem is then reduced to solve the steady state matrix Riccati equation [17] of

$$A^T P + PA - PBr^{-1}B^T P = Q. \tag{5}$$

This equation is solved for constant real symmetric matrix P. Once P is known, the gain is computed as follows:

$$K = r^{-1}B^T P. \tag{6}$$

With this gain K, the control law is implemented as in (3).

C. Generation of Reference States

To implement the control law (3), we would require references for the four elements of the state vector. However, since the load can change any time, generating the reference for the load current is difficult. Hence the fourth element of the gain matrix (as computed in (6)) is chosen as zero. As has been shown in [1], this does not significantly alter the system performance. A block diagram for the computation of reference states is shown in Fig. 4. The PCC voltages v_{ta}, v_{tb}, and v_{tc} are measured and their positive sequence components are extracted [1]. These are the reference filter capacitor voltages and are denoted by v^*_{cfa}, v^*_{cfb}, and v^*_{cfc}. From these reference voltages, the reference filter capacitor (C_f) currents are computed and are denoted by i^*_{cfa}, i^*_{cfb}, and i^*_{cfc}. The reference compensator currents i^*_{fla}, i^*_{flb}, and i^*_{flc} are generated from the positive sequence terminal voltages, as indicated in (7) and [18]

$$\left.\begin{aligned} i^*_{fla} &= i_{la} - \frac{v_{ta} - v_0}{\Delta}(plav + ploss) \\ i^*_{flb} &= i_{lb} - \frac{v_{tb} - v_0}{\Delta}(plav + ploss) \\ i^*_{flc} &= i_{lc} - \frac{v_{tc} - v_0}{\Delta}(plav + ploss) \end{aligned}\right\} \tag{7}$$

where $v_0 = (1/3)\,\Sigma_{\gamma=a,b,c} v_{t\gamma}$ ($v_0 = 0$ when the terminal voltages are balanced) and $\Delta = \left[\Sigma_{\gamma=a,b,c} v^2_{t\gamma}\right] - v_0^2$. The use of this reference generation ensures that the source currents are balanced, distortion free, and in phase with the terminal voltage [18]. The zero sequence current of the load flows from the load neutral and the DSTATCOM dc bus neutral (n in Fig. 1) and does not appear in the source neutral. The term plav is the average power consumed by the load and is obtained by a moving average filter that gives a continuous measurement of the average power by averaging it over the immediate previous half cycle. The term ploss is the additional power drawn from the ac system to hold the dc bus voltage constant against the losses in the inverter. It is generated through a suitable feedback control and is defined by (8). In (8), $e = V_{ref} - V_{dc}^{\text{cyc}}$, where V_{dc}^{cyc} is the cycle-by-cycle average of the dc-link voltage and V_{ref} is its reference value. In the simplest form of feedback, a PI controller is used to compute the ploss

$$ploss = K_p e + K_I \int e dt. \tag{8}$$

Once these reference quantities are obtained, the reference vector for each phase is obtained as follows:

$$x_{refp} = [\, i^*_{flp} \quad i^*_{cfp} \quad v^*_{cfp} \quad 0 \,]^T_{p=a,b,c}.$$

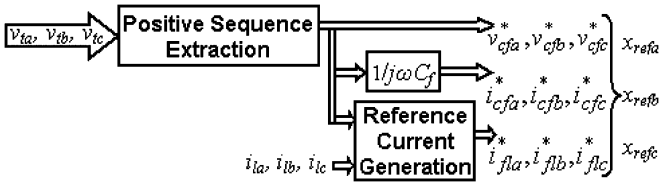

Fig. 4. Block diagram of reference quantities generation.

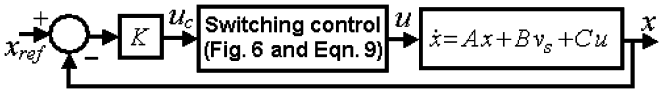

Fig. 5. State feedback control with a nonlinear element in the forward path.

The actual state vectors x_a, x_b, and x_c are obtained from the measurements. The control signal for each phase is then computed using the reference and actual state vectors in the respective phases as given in (3).

D. Switching Control of the Five-Level Inverter

The control signal u_c as defined by (3) is a continuous signal. The switching decision u of the VSC is constrained to be either of $-1/2$, $-1/4$, 0, $+1/4$, and $+1/2$ for a five-level inverter. This decision is obtained from u_c as shown in Fig. 5.

Fig. 6 shows the proposed switching scheme of the five-level inverter. As is evident from (3), u_c is the error (weighted by K) between the reference and actual state variables to be controlled. Since K is a 4×1 matrix, its multiplication with $(x - x_{ref})$ results in a single element. This value of u_c is the summation of the errors of the controlled quantities multiplied by their corresponding gains (elements of K). An arbitrary control signal (corresponding to u_c in Fig. 5) is taken and compared with four switching bands, marked as B_1, B_2, B_3, and B_4 in Fig. 6. A total number of $(n-1)$ bands will be similarly required for an n-level inverter. The switching decisions are taken during the band crossing of the control signal at its positive slope when u_c is positive and at negative slope when u_c is negative. The switching decisions are made each time to change the voltage level by one step (e.g., from 0 to $+V_{dc}/4$, or to $-V_{dc}/4$, etc.) at the previously defined boundaries of B_1, B_2, and B_3. However, at the boundaries of B_4, extreme output voltage levels (i.e., $+V_{dc}/2$ at the upper boundary and $-V_{dc}/2$ at the lower boundary) are applied for the purpose detailed in the next paragraph. In the upper boundary regions, the output voltage state changes from lower to higher (i.e., $-V_{dc}/2$ to $-V_{dc}/4$, $-V_{dc}/4$ to 0, 0 to $+V_{dc}/4$, and $+V_{dc}/4$ to $+V_{dc}/2$) and in the lower boundary regions, from higher to lower (i.e., $V_{dc}/2$ to $V_{dc}/4$, $V_{dc}/4$ to 0, 0 to $-V_{dc}/4$, and $-V_{dc}/4$ to $-V_{dc}/2$). These voltage level transitions ensure that the corresponding discrete values of u (i.e., $-1/2$, $-1/4$, 0, $+1/4$, and $+1/2$) can be obtained from a continuous signal u_c (Fig. 5). The switching strategy can be understood from Fig. 6. At point A, the control signal crosses the lower boundary of B_1 with negative slope. Before this point, the output voltage state was $+V_{dc}/2$. Therefore, the next lower voltage level $(+V_{dc}/4)$ is applied at A. The control signal then follows the path as shown and at the crossing points shown in the figure (i.e., C, D, E, etc.), voltage state transition takes place as mentioned earlier. Now, let us consider point "H" in Fig. 6, at

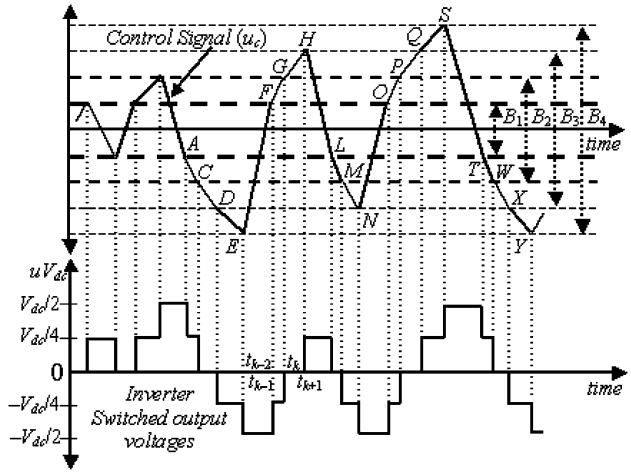

Fig. 6. Switching control of a five level inverter.

which voltage transition takes place from 0 to $V_{dc}/4$. This transition will increase i_{fl}, v_t, and i_{cf} in accordance with their corresponding gains (defined by the elements of K). This, in turn, reduces the error between the reference and actual state variables as per (3). If $V_{dc}/4$ is sufficient enough to force u_c in the opposite direction, no further voltage level transition will take place until u_c reaches the negative boundary regions. However, if $V_{dc}/4$ is not sufficient enough to force u_c in the opposite direction, another higher voltage level transition will take place once u_c crosses a higher positive boundary limit. In Fig. 6, $V_{dc}/4$ has been able to force u_c in the opposite direction. In this way, the waveform of u_c will be mostly periodic and will vary across zero-line.

In a hysteresis current control scheme discussed in [3], two bands were considered for a five-level inverter and fixed voltage levels were applied in different boundary regions. However, by using this approach, unnecessary switching occurs at the band limits, which increases the losses in the system [2]. This can be further justified from [3], where the switching frequency is much higher than that in the present case (as observed in Section IV). In another method discussed in [15] for a three-level inverter, it was said that the current error could be controlled in a single band in general (for higher level inverters also), by selecting the output voltage levels one after another. An outer hysteresis band was introduced optionally to allow switching to the extreme voltage levels for rapid current error reduction during transient conditions. However, this method of taking only two bands will fail for higher level inverters considered in this paper. Suppose we consider the case of only one main band B_1 and an extra band B_2 (to apply the extreme voltage levels, Fig. 6), as discussed in [15]. Then at C in Fig. 6, the output voltage should be $-V_{dc}/2$, irrespective of the previous output voltage state (i.e., at A). Hence, this type of output voltage state transition may result in skipping of the intermediate voltage states. For example, if the voltage state transition is from 0 to $-V_{dc}/2$, the voltage state $-V_{dc}/4$ is skipped. This results in under utilization of the output voltage states and over stress on the switching devices at the time of switching, resulting in increased losses. This phenomenon is particularly more severe for FCMLI as will be discussed in Section IV. For

a five-level inverter, three bands will also be insufficient. From Fig. 6, in the case of only three bands (B_1, B_2, B_3), the output voltage state at Q will be $+V_{dc}/2$ and hence the voltage state $V_{dc}/4$ will be skipped. This will again lead to under utilization of the output voltage states, over stress on the switching devices at the time of switching resulting in increased losses and bad quality outputs. Therefore, in this paper, four bands have been considered for a five-level inverter.

As will be described in Section IV, u_c is mainly influenced by the DSTATCOM injected current error due to the largest weight allotted to it. Therefore, for determining the approximate widths of the bands $B_1 - B_4$, we neglect the errors of the terminal voltage and the filter capacitor current. In that case, the control signal u_c will be expressed as

$$u_c = -K\left(i_{fl} - i_{fl}^*\right). \tag{9}$$

Then, under this condition, the size of the band B_4 is largely determined by the maximum permitted level of current distortion (sets the maximum limits of B_4). In that case, the bands $B_1 - B_3$ can be simply defined as

$$B_i = \frac{i}{(n-1)} B_4 \quad i = 1, 2, 3. \tag{10}$$

Similarly, the minimum possible width of the bands is mainly determined by the maximum allowable switching frequency of the power devices. For that case, we assume that u_c is contained within the band B_1 with whatever voltage levels appearing at the boundaries of B_1 when u_c crosses these boundaries with a certain sign of its slope. At any point of time, the rate of change of the injected current is given by

$$\frac{di_{fl}}{dt} \cong \frac{\Delta i_{fl}}{\Delta t} = \frac{V_i - V_t}{L_f} \Rightarrow \Delta i_{fl} = \frac{V_i - V_t}{L_f} \Delta t \tag{11}$$

where V_i is the inverter output voltage. In (11), R_f has been neglected by considering that the voltage across R_f is often small. For a certain L_f and $f_s = 1/\Delta t$ (maximum allowable switching frequency), the smallest width of $B_1 = K \times \Delta i_{fl}$ can be set by assuming that V_i is having its maximum value (i.e., $V_i = V_{dc}/2$). Then, the minimum possible width of B_1 can be defined as

$$B_{1\min} = K \left| \frac{\frac{V_{dc}}{2} - V_t}{L_f} \right|_{\max} \frac{1}{f_s}. \tag{12}$$

Based on the earlier analysis, the widths of the bands $B_2 - B_4$ can be similarly defined. In general, for an n-level inverter, $(n-1)$ bands are required with their widths defined by

$$B_i = (2 \times i - 1) B_{1\min} \quad i = 1, 2, \ldots, (n-1). \tag{13}$$

Therefore, the maximum and minimum possible widths of the bands can be defined by (10) and (13), respectively. In a practical circuit, Δt in (11) is the total time delay from the point of the ac current measurement to the switching of the power device. This path includes the deadtime of the inverter switches, the current measurement transducer delay and delays through the controller and gate driver logic boards. It can be stated from the mentioned analysis that the set of switching bands has different zones in order to provide a reliable and robust control for an n-level inverter and are also responsible for the desired switching frequency. This gives good convergence to the tracking band as well as good stability of tracking.

Based on the previous observations, the switching decision u_c can be defined for an n-level inverter as

$$\begin{aligned} &\text{if} \left\{ u_c \geq 0 \text{ and } \frac{du_c}{dt} > 0 \right\} \text{then}, u(t_k) \\ &\quad = u(t_{k-1}) + \frac{1}{n-1} \\ &\text{else if} \left\{ u_c < 0 \text{ and } \frac{du_c}{dt} < 0 \right\} \text{then}, u(t_k) \\ &\quad = u(t_{k-1}) - \frac{1}{n-1}. \end{aligned} \tag{14}$$

In (14), $u(t_k)$ is the current value of the switching decision, while $u(t_{k-1})$ is its immediate past value. This can be justified from Fig. 6 in which t_{k-1}, t_k, etc., shown on the horizontal axis are the time instants at which the crossing of u_c and the previously defined boundaries of the bands take place. It can be seen that depending on the sign of u_c and du_c/dt, the output voltage level is either increased or decreased by $V_{dc}/4$, at the crossing points. Note that the inverter holds its output voltage level until t_k, which it attained at t_{k-1}. It is also to be noted that with $u_c > 0$ $du_c/dt < 0$ and with $u_c < 0$, $du_c/dt > 0$, no voltage transition takes place at the crossing points. This is because, in these regions, the control signal is heading towards zero line, which implies that the error between the controlled state vector and its reference value is reducing with the present output voltage level. Hence no voltage transition is required for this. Another point to be noted is that, no exact evaluation is needed for du_c/dt, as only the sign of the slope of u_c is needed at the crossing points of u_c and the band limits. At each sampling instant in the measurement process, the current value of u_c is compared with its previous value. A positive value of this difference indicates a positive du_c/dt, while the negative value indicates a negative du_c/dt.

For a well known environment, such as tracking sinewaves, the range of errors is easily bounded beforehand. Therefore, a gain matrix K can be found that will keep the control value in the desired range [17].

IV. FCMLI-Based DSTATCOM

In this section, the operation and simulation results of a five-level FCMLI-based DSTATCOM are presented. The distribution system of Fig. 2, with a fundamental frequency of 50 Hz has been considered. A balanced three-phase source with a line-to-line rms voltage of 11 kV supplies unbalanced RL loads of (24.2 + j60.5)Ω, (12.2 + j31.4) Ω, and (48.2 + j94.2) Ω in phase $-a$, b and c respectively. A three-phase uncontrolled rectifier load (as nonlinear load) is also connected to the load bus through a smoothing reactor of 0.5 mH in each phase and having a load of (100 + j31.4) Ω. The feeder impedance is (6.05 + j36.26) Ω in each phase. The unbalanced and distorted load currents and terminal (PCC) voltages of the system without any compensation are plotted in Fig. 7.

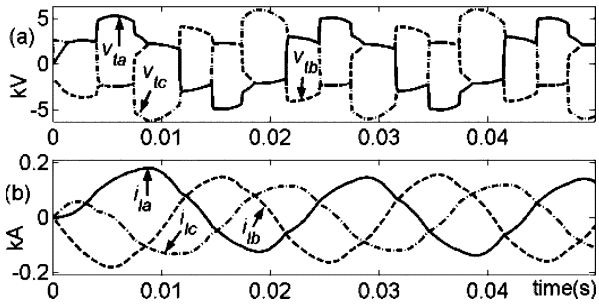

Fig. 7. (a) PCC voltages. (b) Source currents in the uncompensated case.

TABLE III
FIVE-LEVEL INVERTER PARAMETERS

Device ON resistance	0.01 Ω
Device OFF resistance	1.0E6 Ω
Forward voltage drop	0.0 kV
Forward breakover voltage	7.5 kV
Reverse withstand voltage	7.5 kV
Snubber resistance	500.0 Ω
Snubber capacitance	25 μF

The dc-link of the FCMLI-based DSTATCOM contains two capacitors of 500 μF each (Fig. 1). A flying capacitor voltage balancing scheme proposed in [3] has been applied here. Each time the control signal u_c crosses the previously defined band boundaries, the following quantities are sensed:

- the direction of the current i_{fd} flowing through the inverter;
- the desired output voltage level of the inverter (Fig. 6);
- the voltage state of the flying capacitors (i.e., whether they are overcharged, undercharged, or within limits).

Based on these observations, a most favorable switch combination is chosen from Table I. This produces balanced flying capacitor voltages as well as the desired voltage levels. For the switching control scheme shown in Fig. 6, less bands results in skipping of the intermediate voltage levels, as discussed earlier. This phenomenon may result in flying capacitor voltage unbalance, as a few switch combinations (corresponding to the skipped voltage level, Table I) will not take part in controlling the capacitor voltages. This will further deteriorate the system performance. Therefore, $(n-1)$ bands are necessarily required for an n-level inverter.

The size of the flying capacitors can be chosen depending on the maximum voltage stress across them, permissible voltage variations across these capacitors and the maximum current flowing through each of them [4], [9], [11]. Here, for simplicity, equal size of the capacitors are taken as $C_4 = C_3 = C_2 = 500\ \mu$F, for each phase. The other parameters of the inverter are listed in Table III. With reference to Fig. 2, $L_f = 0.03854$ H, $R_f = 3.0\ \Omega$ and $C_f = 50\ \mu$F are chosen for each phase. The reference dc-link voltage (V_{ref}) is taken 24 kV. The widths of the switching bands (Fig. 6) are taken $B_4 = 0.01$, $B_3 = 0.0075$, $B_2 = 0.005$, $B_1 = 0.0025$ p.u [as defined in (10)]. The PI-controller parameters (8) are $Kp = 0.4$ and $K_I = 10$.

The compensated system is started from rest (i.e., the initial conditions are zero). The DSTATCOM is connected at the end

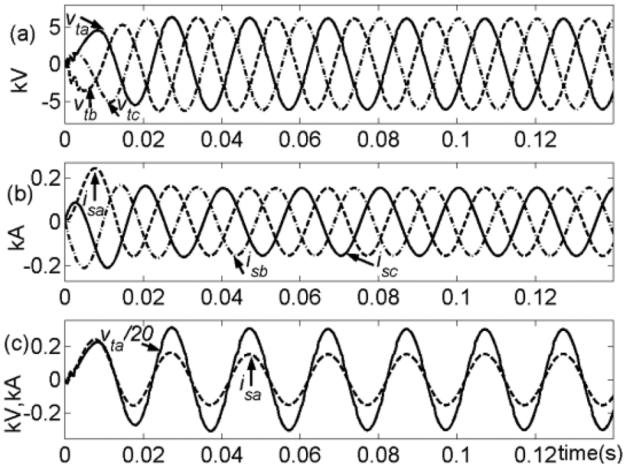

Fig. 8. (a) PCC voltages. (b) Source currents. (c) UPF operation of the FCMLI-based DSTATCOM compensated system.

of the first half cycle when the average power measurement becomes available. For the system considered here, the LQR performance index is minimized with

$$Q = \mathrm{diag}([200 \quad 0 \quad 10 \quad 0]) \quad r = 0.001$$

where diag is a diagonal matrix. The two variables that are most the important to be controlled are the current i_{fl} and the voltage v_t. The weighting matrix Q reflects the importance of these states. Based on the system just discussed and the LQR parameters, the gain matrix is given by $K = [220.3\ 2.5\ 100\ -65.8]$. Using this feedback, the oscillatory closed-loop eigenvalues are to the left of the line $s = -1298$. To avoid the complexity of forming a reference for the load current, the gain matrix is restricted to $K = [220.3\ 2.5\ 100\ 0]$. This reduced state feedback results in a minimal shift in the closed-loop eigenvalues to the left of $s = -1171$. It can be seen from the response shown in Fig. 8 that both source currents and terminal voltages become balanced and free from harmonics once the compensator action settles. Unity power factor (UPF) operation is also achieved and hence the DSTATCOM fulfills the objectives set earlier. The voltage in Fig. 8(c) has been scaled down to 0.05 times. The voltages and currents shown in Fig. 8(a) and (b) is analyzed using Fourier series analysis. The resulting total harmonic distortion (THD) of v_{ta} is 1.43% and of i_{sa} is 0.17%, which are well within the limits of IEEE Std. 519–1992 [19].

Fig. 9(a) shows the dc-link and phase-a flying capacitor voltages of the inverter. The capacitors are assumed to be precharged to their corresponding reference values stated above. It can be seen that V_{C1} and flying capacitor voltages are balanced at their corresponding set values of 24 kV, 18 kV, 12 kV and 6 kV respectively, justifying the flying capacitor voltage balancing scheme adopted from [3]. Once the DSTATCOM is operational, the term ploss [as in (8)] settles within a cycle to a small oscillating value, which is the real power required by the inverter to keep V_{C1} balanced [Fig. 9(c)]. The source power p_s and the load power p_{lav} are also shown in Fig. 9(c). p_{loss} has an average value of 0.032 MW and maximum and minimum

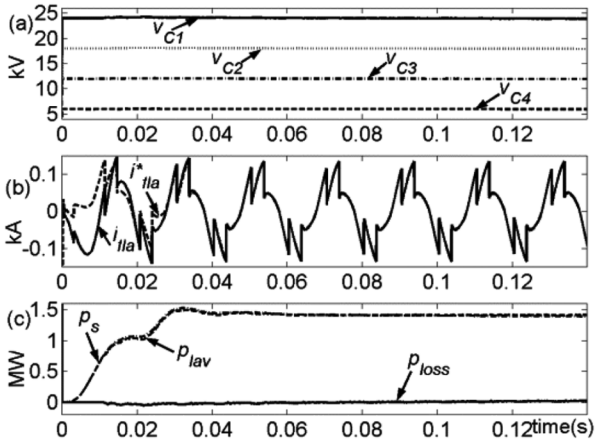

Fig. 9. (a) DC capacitor voltages. (b) Reference current tracking. (c) Instantaneous powers of the FCMLI-based DSTATCOM.

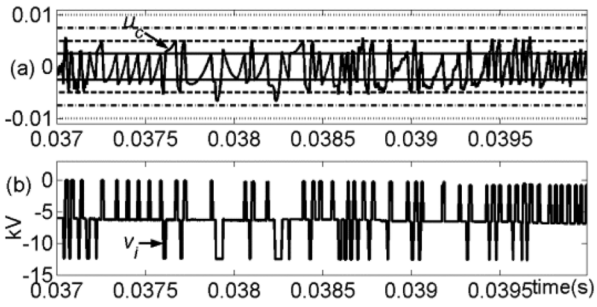

Fig. 10. (a) Control signal with four bands. (b) Inverter switched output voltage.

values of 0.044 MW and 0.02 MW, respectively, whose differences from the average value correspond to the charging and discharging of the capacitors. These values indicate that the average power consumed by the inverter is only 2.28% of the load power ($\approx$ 1.4 MW). Fig. 9(b) illustrates that the injected current tracks the reference within a half-cycle, which confirms the robust tracking performance of the state feedback control strategy proposed before.

Fig. 10 shows the variation of the phase-a control signal $u_c(3)$ across the allotted bands and phase-a output voltage of the inverter. As can be seen, whenever u_c crosses the positive boundaries with positive slope or negative boundaries with a negative slope, a new output voltage level is generated [different from its previous one, Fig. 10(b)]. Following a change in the reference, u_c accordingly changes. The controller then outputs the desired voltage required to follow the reference as close as possible. It should again be noted that u_c mainly depends on the DSTATCOM injected current error, as maximum weight has been allotted to it. The fast recovery and good accuracy can be appreciated. Due to the nature of the control and the inverter, the switching frequency is not constant and varies for all the switches of the FCMLI [1], [4]. Here, the minimum and maximum switching frequencies are found to be around 0.41 kHz and 0.98 kHz, respectively. The switching frequency can be further reduced by increasing the widths of the bands (Fig. 6).

It is to be noted that the gain matrix is designed with the parameters of phase-a of the system and is subsequently used for

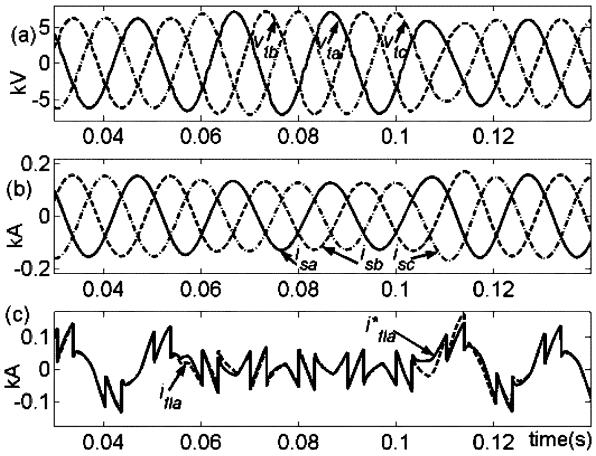

Fig. 11. (a) PCC voltages. (b) Source currents. (c) Reference current tracking with load change.

the other two phases. Since the load parameters are different for the different phases, the algorithm can be claimed to be robust to the variations in the load parameters. To further investigate the effect of load change on the compensator system, the RL component of the load is disconnected at 0.05 s in the simulation run when the system is operating in the steady state. Therefore, after 0.05 s, the source supplies only the rectifier. At 0.1 s, the original loading condition is restored. The system responses are shown in Fig. 11. It can be seen that the tracking is satisfactory and smooth with new references apart from the half cycle delay in formulation of correct references, as is evident from Fig. 11(c). This confirms that the controller performance is independent of the load changes. As the tracking is good, balanced and sinusoidal terminal voltages and source currents are achieved also in the changed load condition, without any significant delay or transient [Fig. 11(a) and (b)]. It should be noted that here that the aim of the DSTATCOM operation is not to regulate the PCC voltage, but to make the source current balanced and distortion free. Since the source voltage v_s is also balanced and sinusoidal, the fulfillment of the above aim ensures a balanced and sinusoidal PCC voltage. In addition, the unity power factor operation at the PCC minimizes the feeder drop. Therefore the PCC voltage varies as the load changes in accordance with feeder drop caused by change in the source current (Fig. 11).

For the same system conditions, a DSTATCOM is designed and simulated with the two-level inverter structure such as that used in [1], with three H-bridge VSCs connected to a common dc storage capacitor. The dc capacitor is sized equivalently and three equivalent single phase transformers are used to connect the inverter to the PCC. The leakage inductance and losses of the transformers are equivalently same as the interface inductance and resistance used for the FCMLI-based DSTATCOM. The same control strategy as discussed before is applied for this case as well. The ac filter capacitors are also taken as same. A single switching band is taken and is equal to B_4 (Fig. 6). The voltage $V_{dc}/2$ is applied at the upper boundary and $-V_{dc}/2$ at the lower boundary of the band, as u_c crosses these boundaries. The THDs of v_{ta} and i_{sa} of this modified system is found to be 4.6% and 1.3%, respectively. The switching frequency is about 4.5 kHz and ploss has an

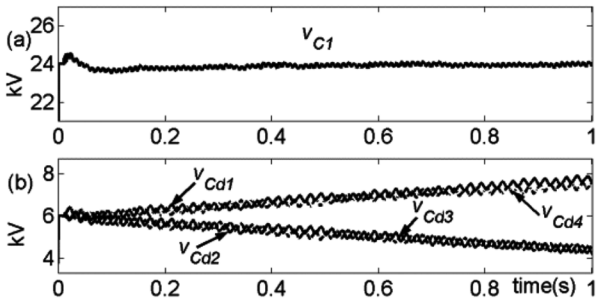

Fig. 12. (a) Total dc-link voltage. (b) Individual dc capacitor voltages.

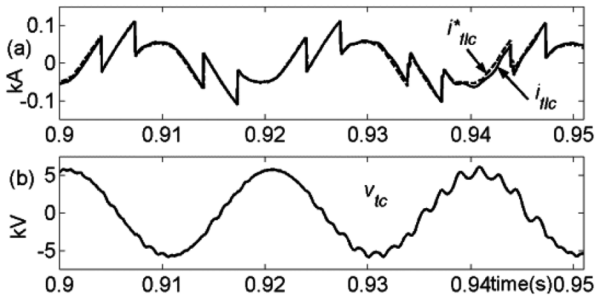

Fig. 13. (a) Reference current tracking. (b) Terminal voltage of phase-c.

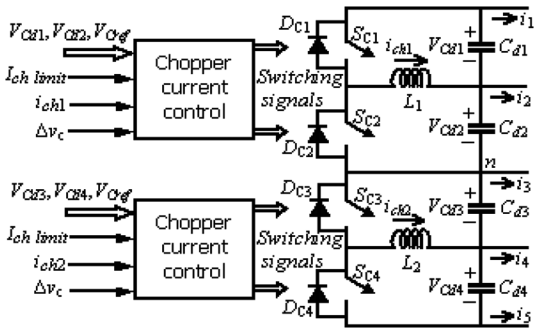

Fig. 14. Control block diagram and equivalent circuit of the chopper.

average value of 0.03 MW. By comparing these data with those found in the proposed FCMLI-based DSTATCOM system, we find that the switching frequency is considerably lesser and also the compensator performance is much improved for the proposed DSTATCOM. In addition, it offers less THD in both voltages and currents for almost the same losses and therefore, the filter size requirements are less. Therefore, for high voltage distribution systems, an FCMLI-based DSTATCOM with the proposed control strategy is better suited as compared to the other existing two-level structures. Its superiority is also due to few other factors as mentioned in Section I.

V. DCMLI-Based DSTATCOM

In this Section, the operation and simulation results of a five-level DCMLI-based DSTATCOM are presented. The operating conditions and the device parameters are the same as in the case of FCMLI-based DSTATCOM. However, here, the dc-link contains four capacitors of 1000 μF each [Fig. 1(b)] and the blocking diodes [D_1, D_{11}, etc., in Fig. 1(b)] are correspondingly considered of higher ratings. As discussed earlier, a DCMLI requires an extra control over its dc-link because of the voltage unbalance occurring across its individual dc-link capacitors. This phenomena is evident from Figs. 12 and 13, in which, the operational performances of a DCMLI-based DSTATCOM (without any extra control over its dc-link) is shown for the operating conditions already mentioned. It is evident from Fig. 12 that despite a balanced total dc-link voltage (V_{C1}, controlled using (8)), the four dc- link capacitor voltages drift from their reference values. The inner two capacitor voltages (V_{cd2}, V_{cd3}) collapse while the outer capacitor voltages (V_{cd1}, V_{cd4}) increase and may go beyond the safe limits of operation. The implication of this phenomena is the loss of tracking, affecting the control performance and malfunctioning of the inverter. This is further evident from Fig. 13, where loss of tracking of the phase-c reference and injected current are shown along with the affected phase-c terminal voltage.

To prevent the capacitor voltage imbalance, chopper circuits as shown in Fig. 14, are preferentially used as it is more reliable and robust against line faults, transients, and disturbances [4], [12]. The capacitor voltages are controlled within a band by transferring the extra energy from the overcharged capacitor to an inductor and then transferring it back from the inductor to the undercharged capacitor. In Fig. 14, L_1 is used to exchange the energy between C_{d1} and C_{d2} using the switches S_{C1}, S_{C2} and antiparallel diodes D_{C1} and D_{C2}, while L_2 exchanges the energy between C_{d3} and C_{d4} using S_{C3}, S_{C4}, D_{C3}, and D_{C4} [12]. However, using this control, the chopper current rating may be large, which can be adjudged from the following discussion. It is assumed that the rate of monotonic change in capacitor voltages due to i_1, i_2, i_3, i_4 and i_5 is small. The chopper is assumed to restore the voltages close to V_{cref} at a fast rate. Therefore, i_1 to i_5 in Fig. 14 are neglected. Suppose that at a certain instant, V_{cd1} is more than its reference value (V_{cref}) by Δv_C, which is the band beyond which the chopper is activated and assume $C_{d1} = C_{d2} = C_{d3} = C_{d4} = C$. Then, the extra energy stored in C_{d1} is given as

$$E_{c1} = \frac{1}{2} C v_{cd1}^2 - \frac{1}{2} C v_{cref}^2. \tag{15}$$

Now, S_{C1} is closed until i_{ch1} builds up, so that all of the extra energy stored in C_{d1} is transferred to L_1. Therefore, the maximum chopper current $i_{ch\,\max}$ has the following relations:

$$\frac{1}{2} L_1 i_{ch\,\max}^2 = \frac{1}{2} C \left\{ v_{cd1}^2 - v_{cref}^2 \right\} \tag{16}$$

$$i_{ch\,\max} = \sqrt{\frac{C}{L_1}} \left\{ v_{cd1}^2 - v_{cref}^2 \right\}^{1/2}. \tag{17}$$

It is evident from (17) that the chopper current rating may be large for high value of $i_{ch\,\max}$. To reduce the current rating, a scheme has been proposed in this paper in which the chopper is operated with a current limit, $I_{ch\ \mathrm{limit}}$, which is a fraction of $i_{ch\,\max}$. The corresponding control block diagram is shown in Fig. 14. In this scheme, in each of the chopper circuits, a switch (such as S_{C1} or S_{C2} in the upper chopper circuit) is closed depending upon the result of comparison of the larger of the corresponding capacitor voltages (such as v_{cd1} and v_{cd2} in the

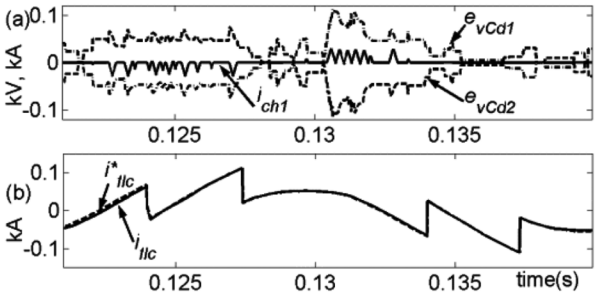

Fig. 15. (a) Chopper current control. (b) DSTATCOM tracking performance.

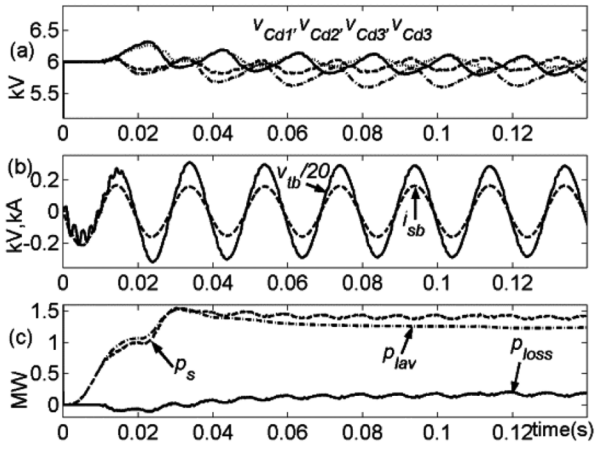

Fig. 16. (a) Controlled dc capacitor voltages. (b) UPF operation. (c) Instantaneous powers of the DCMLI-based DSTATCOM.

upper chopper circuit) with the voltage limit ($V_{cref} + \Delta v_C$). The switch is kept closed till the chopper current (i_{ch1} in the upper and i_{ch2} in the lower circuit) reaches the predefined current limit, $I_{ch\ \mathrm{limit}}$. At this point, the switch is opened and is kept open till the chopper current reduces to zero by transferring the energy to the undercharged capacitor through an anti-parallel diode (such as D_{C1} or D_{C2} in the upper circuit). If the capacitor voltage under consideration is larger than V_{cref}, the cycle is repeated and continued till the capacitor voltage is close to V_{cref}. In this method, the chopper current is limited to $I_{ch\ \mathrm{limit}}$, which can be set at the designing stage of the chopper circuit.

Using this chopper control scheme, the DCMLI-based DSTATCOM is simulated for $\Delta v_C = 50$ V, $I_{ch\ \mathrm{limit}} = 30$ A, $L_1 = L_2 = 0.2$ H and $V_{cref} = 6$ kV (as $V_{ref} = 24$ kV). Fig. 15(a) shows the voltage errors of C_{d1} and $C_{d2}(e_{vcd1} = v_{cd1} - v_{cref}, e_{vcd2} = v_{cd2} - v_{cref})$ and i_{ch1}. It can be seen that as one of the voltage errors moves out of band, the corresponding switch is opened and closed repeatedly with a current limit of 30 A in the corresponding direction, until voltages of the capacitors are close to V_{cref}. Thereafter, the chopper is turned off and it remains off till voltage of one of the capacitors again crosses the band. The reference and actual injected current waveforms of phase-c plotted in Fig. 15(b) show the perfect tracking performance as the dc-link capacitor voltages are balanced now. Fig. 16(a) shows the four balanced dc-link capacitor voltages controlled using the developed chopper control scheme. Fig. 16(b) shows the balanced and distortion free PCC voltage and source current with UPF operation. Fig. 16(c) shows the instantaneous powers. In this case, ploss has an average value of 0.08 MW, which is significantly higher than that observed for FCMLI-based DSTATCOM of the previous section. This means that the losses occurring in the DCMLI-based DSTAT COM are much higher. The switching frequency of the main semiconductor devices [S_1, S_2, etc., in Fig. 1(b)] in this case is same as that observed for FCMLI, which can be justified from Tables I and II. It can be seen that for any voltage level output, equal number of switches are conducting for both the inverters. Also, as the levels change from one to another [as in Fig. 6], only two switching states change. However, extra losses occur in DCMLI because of the switching losses in the chopper circuits and also in the snubber parameters of the blocking diodes [e.g., D_1, D_2, etc. in Fig. 1(b)]. These extra losses add up to increased ploss for the DCMLI-based DSTATCOM. The other implication of the chopper circuit is that due to transfer of energy from one capacitor to another via an inductor, the response of the dc-link capacitor voltage control is slow. Further, as the capacitor voltages are controlled within a band, their variations are large for a given capacitance of the dc link. These result in relatively poorer quality of the output controlled quantities (THDs of v_{ta} is 1.99% and of i_{sa} is 0.23%) as compared to those in the FCMLI-based DSTATCOM.

The simulation results confirm that the proposed DSTATCOMs based on a FCMLI and a DCMLI show satisfactory results. Time response in all cases is about or less than one cycle, which is adequate for the distribution systems.

VI. Conclusion

In this paper, proposals have been made for the DSTATCOMs based on multilevel inverters for systems with non-stiff source. Two multilevel inverters, namely, FCMLI and DCMLI have been considered. A state feedback control-based compensating technique has been derived for the DSTATCOM. It results in balanced and distortion free source currents and terminal voltages. A switching strategy has been proposed for the multilevel inverter, which ensures an efficient utilization of all output voltage states of the inverter for tracking the reference. A flying capacitor voltage control scheme for the FCMLI-based DSTATCOM has been used, which results in balanced flying capacitor voltages and at the same time ensures that the desired output voltage level is generated. A control scheme has been proposed for the chopper connected to the dc link of the DCMLI-based DSTATCOM. It equalizes the dc-link capacitor voltages while limiting the maximum current of the chopper switches and inductors. Performance of the DSTATCOMs has been tested through simulation of a distribution network having unbalanced and nonlinear loads. The simulation results confirm that the proposed DSTATCOMs offer satisfactory performances. However, performance of the FCMLI-based compensator is slightly better.

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