A flexible DSTATCOM operating in voltage or current control mode

G. Ledwich and A. Ghosh

Abstract: The topology and control are discussed of a distribution static compensator (DSTATCOM) that can be operated flexibly in the voltage or current control mode. In the voltage control mode, the DSTATCOM can force the voltage of a distribution bus to be balanced sinusoids. In the current control mode, it can cancel distortion caused by the load, such that current drawn by the compensated load is pure balanced sinusoid. Both these objectives are achieved, irrespective of unbalance and harmonic distortions in load currents or source voltages. The chosen DSTATCOM topology includes three single-phase voltage source inverters connected in parallel to a filter-capacitor, which allows the high-frequency component of the current to pass. A switching control scheme is proposed, and its suitability is proved for this problem. The proposed scheme is verified using computer simulation studies.

1 Introduction

Power quality issues are gaining significant attention due to the increase in the number of sensitive loads. Many of these loads use equipment that is sensitive to distortions or dips in supply voltages. Almost all power quality problems originate from disturbances in the distribution networks. Regulations apply in many places, which limit the distortion and unbalance that a customer can inject to a distribution system [1]. These regulations may require the installation of compensators (filters) on customer premises. It is also expected that a utility will supply a low distortion balanced voltage to its customers, especially those with sensitive loads.

A distribution static compensator (DSTATCOM) is a voltage source inverter (VSI)-based power electronic device. Usually, this device is supported by short-term energy stored in a DC capacitor. When a DSTATCOM is associated with a particular load, it can inject compensating current so that the total demand meets the specifications for utility connection. Alternatively, it can also clean up the voltage of a utility bus from any unbalance and harmonic distortion. The aim of this paper is to investigate a DSTATCOM that can perform both these tasks.

For load compensation using a DSTATCOM, one of the major considerations is the generation of the reference compensator currents. There are several methods that have been developed for the use of the compensator when it tracks these reference currents, thereby injecting three-phase currents in the AC system to cancel out disturbances caused by the load [2–5]. Most of these methods carry an implicit assumption that the voltage at the point of common coupling is tightly regulated and cannot be influenced by the currents injected by the shunt device. This, however, is not a valid assumption for most applications, and the performance of the compensator will degrade considerably at high-impedance AC connection points.

We propose a DSTATCOM topology that can work in either the voltage or current control mode. In a voltage control mode, the DSTATCOM is connected at a utility bus to maintain a balanced voltage at that bus, irrespective of unbalance or distortion in either side of the bus. In this mode, the operation and maintenance of the DSTATCOM is the responsibility of the utility. Alternatively, in the current control mode, the DSTATCOM compensates for any unbalance or distortion in the load. Ideally, it should draw a balanced current from the system, irrespective of any unbalance or harmonics in either the source or load. It is also assumed that the DSTATCOM is placed at a utility bus or on customer premises. Therefore, the source is not assumed to be stiff.

We propose a compensator structure that is capable of both these tasks. The compensator used for this study consists of three single-phase H-bridge voltage source inverters (VSIs), driven by a single DC storage capacitor. We also have a shunt passive filter-capacitor to provide a path for the high-frequency components of the current. The DSTATCOM current and voltage references are generated based on Fourier series extraction of fundamental sequence components, using half-cycle running (moving) averaging. We also propose a linear quadratic regulator (LQR)-based design of the switching controller scheme, which tracks the reference using the proposed compensator-filter structure.

2 DSTATCOM in power distribution systems

A DSTATCOM is capable of compensating either bus voltage or line current. If it operates in a voltage control mode, it can make the voltage of the bus to which it is connected a balanced sinusoid, irrespective of the unbalance and distortion in voltage in the supply side or line current. Similarly when operated in a current control mode, it can force the source side currents to become balanced sinusoids.

Consider a typical radial distribution system, as shown in Fig. 1. It consists of a stiff source connected at bus 1 and

IEE Proceedings online no. 20020009

DOI: 10.1049/ip-gtd:20020009

Paper first received 25th April 2000 and in revised from 21st June 2001

G. Ledwich is with the School of Electrical & Electronic Systems Engineering, Queensland University of Technology, Brisbane, Queensland, Australia

A. Ghosh is with the Indian Institute of Technology, Kanpur, India

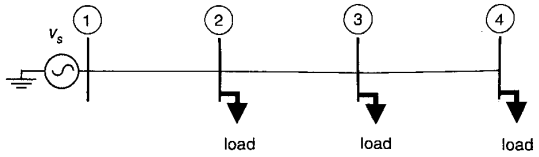

Fig. 1 *Typical radial distribution system*

three load buses. It is assumed that consumers are supplied from these buses. A DSTATCOM can be connected in any of these buses, depending on whether it belongs to the utility or a particular customer. For example, if the voltage at bus 3 is distorted, it affects customers both at buses 3 and 4. The utility may then install a DSTATCOM at this bus to clean up its voltage. On the other hand, suppose that the consumer at bus 4 has loads that draw unbalanced and distorted current from the supply. In order to avoid a penalty, one option for the consumer is to install a DSTATCOM on its premises, so that the current drawn from bus 4 is a balanced sinusoid.

A DSTATCOM can be realised using a VSI and a DC storage capacitor. One of the requirements of a DSTATCOM in a three-phase four-wire distribution system is that it is capable of injecting three unbalanced and distorted currents into the AC system, to cancel voltage or current unbalance or distortions. We therefore need a DSTATCOM that is able to force three independent currents through three phases. The problem of using an ordinary three-phase bridge inverter as the power circuit of the DSTATCOM is that the sum of three currents must be equal to zero. This prevents its use as a four-wire DSTATCOM power circuit. The DSTATCOM structure considered in this paper is shown in Fig. 2. It contains three H-bridge VSIs connected to a common DC storage capacitor [5]. This topology allows three independent current injections, as this contains three separate H-bridge inverters.

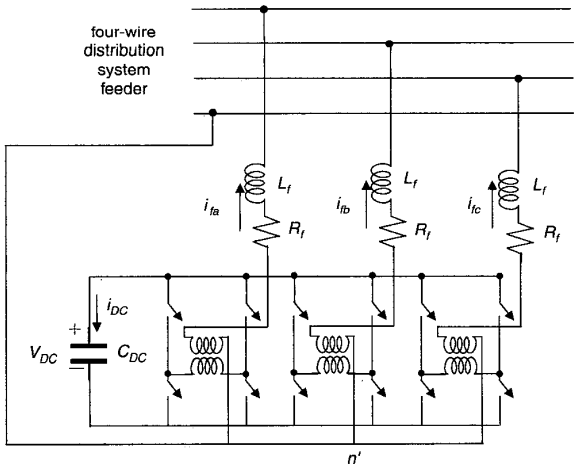

Fig. 2 *Compensator structure used where three separate VSIs are supplied from common DC storage capacitor*

In the circuit shown in Fig. 2, each switch represents a power semiconductor device and an anti-parallel diode combination. Each VSI is connected to the network though a transformer. Six output terminals of the transformer are connected in star. The purpose of including the transformers is to provide isolation between the inverters. This prevents the DC storage capacitor from being short-circulated through switches in different inverters. The inductance L_f in Fig. 2 represents the leakage inductance of each transformer and additional external inductance, if any. The switching losses of an inverter and the copper loss of the connecting transformer are represented by a resistance R_f. The iron losses of the transformer are neglected. For a star-connected load, the neutral point of the three transformers is connected to the load neutral. There are alternative power electronic options [6, 7] that achieve a similar performance.

The equivalent circuit of the system under study is shown in Fig. 3. In Fig. 3 the point of common coupling (PCC) is the bus to which the DSTATCOM is connected. The voltage source (v_s) is the Thevenin equivalent voltage looking to the left of this bus. The Thevenin equivalent impedance is represented by the resistance R and inductance L. The source current is denoted by i_s and the load current by i_l. We further define the voltage at the point of common coupling as the terminal voltage v_t. The DSTATCOM contains a VSI, a DC capacitor (C_{dc}), a resistance (R_f) and an inductance (L_f). In addition, a filter-capacitor (C_{filt}) is added to the circuit, to provide a path for the harmonic current. Note that the terminal voltage is the voltage across the filter-capacitor C_{filt}, i.e. v_t=v_{filt}. We denote the three-phase quantities by $_a$, $_b$ and $_c$. For example, the source voltages are represented as v_{sa}, v_{sb} and v_{sc} and the load currents as i_{la}, i_{lb} and i_{lc}.

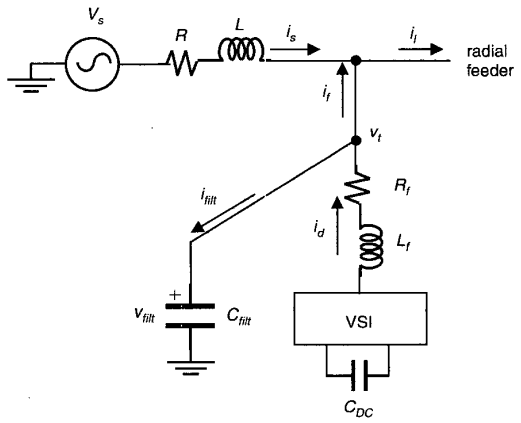

Fig. 3 *Equivalent circuit of shunt-compensated distribution system*

3 DSTATCOM control

In this Section, we present the control design for the system shown in Fig. 3. The equivalent circuit of the compensated system is shown in Fig. 4, where the feeders and the loads on the radial feeder to the right of the point of common coupling are represented by R_l and L_l. Let us define the following state vector: $\mathbf{x}^T = [\mathbf{i}_1, \mathbf{i}_2, \mathbf{i}_3, \mathbf{v}_t]$.

The state-space equation of the circuit can then be written as

$$\dot{x} = \begin{bmatrix} -R/L & 0 & 0 & -1/L \\ 0 & -R_f/L_f & 0 & 1/L_f \\ 0 & 0 & -R_l/L_l & 1/L_l \\ 1/C_{filt} & -1/C_{filt} & -1/C_{filt} & 0 \end{bmatrix} x$$

$$+\begin{bmatrix}1/L\\0\\0\\0\end{bmatrix}v_s+\begin{bmatrix}0\\-V_{dc}/L_f\\0\\0\end{bmatrix}u$$
$$=Ax+B_1v_s+B_2u \quad (1)$$

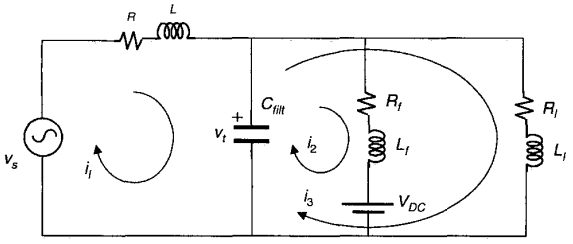

Fig. 4 *Equivalent circuit of DSTATCOM*

The state eqn. 1 contains the feeder and load impedances; although the former is measurable, the latter may change at any time. Moreover, any feedback controller must rely on the locally measured variables. From Fig. 3 it can be seen that the local variables for the DSTATCOM are terminal voltage, source current, filter current and the filter capacitor current. Based on the above observation, we make the following state transformation to more conveniently represent the local measurements shown in Fig. 3:

$$z=\begin{bmatrix}i_f\\i_{filt}\\v_t\\i_l\end{bmatrix}=\begin{bmatrix}-1&0&1&0\\1&-1&-1&0\\0&0&0&1\\0&0&1&0\end{bmatrix}x=Px \quad (2)$$

The state eqn. 1 can then be transformed into

$$\dot{z}=PAP^{-1}z+PB_1v_s+PB_2uV_{DC}=\Lambda z+\Gamma_1v_s+\Gamma_2u \quad (3)$$

3.1 Proportional control

Assuming we have full control over u, an infinite time LQR can be designed for this problem. The control is of the form

$$u=-K(z-z_{ref}) \quad (4)$$

where z_{ref} is the desired state vector. In an LQR problem, a performance index is chosen in the form

$$J=\int_0^\infty\left\{(z-z_{ref})^TQ(z-z_{ref})+u^TRu\right\}dt \quad (5)$$

and u is chosen to minimise J through the solution of the steady-state Ricaati eqn. [8].

3.2 Switching control

The control signal computed so far using the LQR is a continuous signal. In practice, the control signal u is the switching decision of the VSI of the DSTATCOM, and thus is constrained to be either $+1$, 0, -1 in each phase. One important property of the LQR is that it is tolerant of input nonlinearities, as shown in Fig. 5. LQR design is stable, provided that the effective gain of the input nonlinearity is constrained in the sector between 1/2 and 2 [6]. When the errors are large, and the control is bounded between $+1$ and -1, the gains of K must be small. The switching control is $+1$ when the LQR value is positive and -1 when it is negative. For a set of decreasing values of R, we obtain a corresponding set of increasing values of K. Thus, there will always exist a value of R such that Kz is bounded appropriately. Finite time convergence of the regulator problem can be shown, provided Q is chosen such that as $R\rightarrow 0$, $K\rightarrow\infty$. This gives a better performance than the exponential convergence of proportional control [9].

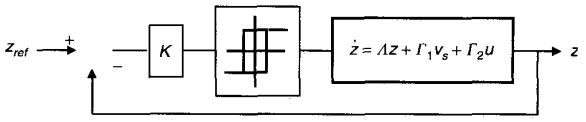

Fig. 5 *State feedback control with nonlinear element in forward path*

After the initial transient is over, the control for each phase, based only on the sign of the LQR value, will chatter at a rate limited by the switches. To avoid this, the switching, for each phase, is based on

$$u=-hys(K\{z-z_{ref}\}) \quad (6)$$

where the *hys* function is defined by

$$\begin{aligned}&\text{if } w>\lim \text{ then } hys(w)=1\\&\text{else if } w<-\lim \text{ then } hys(w)=-1\end{aligned} \quad (7)$$

The selection of lim determines the switching frequency while tracking the reference. This application of LQR design to switching control gives good convergence to the tracking band, as well as good stability of tracking. In this control law, the switching decision is based on a linear combination of multiple states. Hence, we call this switching band tracking control.

For a well known environment, such as tracking sine waves, the range of errors is easily bounded beforehand. Therefore, a gain matrix **K** can be found that will keep the control value in the desired range.

4 DSTATCOM as a voltage regulator

In this Section, we present the use of DSTATCOM as a voltage regulator to correct the voltage of a specified bus. As seen from eqn. 6, a key aspect of the functioning of a DSTATCOM is the generation of the reference waveforms. For the operation of the DSTATCOM as a voltage regulator, we need to specify the following references: terminal voltage (v_t), injected current (i_f), current through the filter capacitor (i_{filt}) and load current (i_l). Of these, the load current is load dependent and may change at any time. It is thus desirable to eliminate it from the feedback signal, such that knowledge of the load in eqn. 1 becomes redundant in designing the feedback signal. The implication of this reduced feedback is shown in Example 1 below.

We can choose an arbitrary magnitude for the reference signal of v_t. In this paper, a reference magnitude of 1.0 p.u. is chosen when the DSTATCOM operates in the voltage control mode. However, the phase of the reference signal must be chosen such that the real power drawn by the DSTATCOM is zero in the steady state. To facilitate this, we use the following feedback signal:

$$\phi_a(k+1)=\phi_a(k)+C_Pp_{f-av} \quad (8)$$

where ϕ_a is the angle of the phase a of the reference voltage: C_p is a gain: p_{f-av} is the average of the shunt power: and k is the discrete-time index. Once ϕ_a is obtained, the reference angles for the other two phases are obtained through 120° phase shift. The instantaneous three-phase reference

voltages for the terminal can then be generated with respect to any phase-locked point that provides the reference time setting. Once this voltage reference is generated, the corresponding current through the filter-capacitor can be generated as follows. Let the reference voltage for phase a be given by $\sin(\omega t+\phi_a)$. The reference current for this phase is then given by $\omega C_{filt} \cos(\omega t+\phi_a)$.

To generate i_f, note that $i_l = i_f+i_s$. Hence, the reference for i_f must be the instantaneous difference between these two currents. However, in order to prevent distortion creeping in, it is desirable to generate this reference using the fundamental value of the source current, i.e.

$$i_{f-ref} = i_l - i_{s-fund} \tag{9}$$

The fundamental can be extracted using the procedure outlined in Appendix (Section 9.2). Note that the reference generation algorithm eqns. 8 and 9 requires average values over a half-cycle. We have obtained these through moving averages, which is the average between two points that are exactly a half-cycle apart and not necessarily synchronised with the zero crossing of any particular waveform. This has the advantage that the average values are continuously available, and any disturbance in a system variable is fully incorporated in its average a half-cycle later.

To implement the switching control of eqn. 6 using the reduced state feedback, a consistent set of references is required. Note that the terminal voltage is an independent quantity, and the current through the filter-capacitor is dependent on it. In addition, the form of generation of reference for the injected current through eqn. 9 is based on the actual measurements and fundamental extraction. Therefore, these three terms form a consistent set. The consistency of the state references is an integral part of the proof of control convergence, given in Appendix 9.1. Starting from an arbitrary initial state, the stability properties imply that the system will converge; if the reference is sufficiently small, the system will converge to the switching surface. Controller parameters can always be designed so that the above conditions are satisfied and perfect tracking of system states results. Note, however, that unmodelled disturbances such as lightning strikes, faults or large load changes may saturate the control, leading to imperfect tracking.

Example 1: In this example, we demonstrate the performance of a voltage regulating DSTATCOM. The system fundamental frequency is chosen as 50 Hz. It is assumed that the Thevenin equivalent voltages are unbalanced and are given by $v_{sa} = \sin(100\pi t)$ p.u.; $v_{sb} = 1.25\sin(100\pi t - 120°)$ p.u.; and $v_{sc} = 0.85\sin(100\pi t + 120°)$ p.u. The Thevenin equivalent source impedance is given (p.u.) by $R=0.05$ and $X=\omega L=0.3$.

It is assumed that the load buses to the right of the PCC contain passive RL loads. We refer to the combined feeder and load impedances to the right of the PCC as load impedances for simplicity. They are unbalanced and given (p.u.) by $Z_{la}=R_{la}+jX_{la}= 2.0+j1.5$: $Z_{lb}=R_{lb}+jX_{lb}= 2.55+j1.25$: and $Z_{lc}=R_{lc}+jX_{lc}=1.0+j2.3$.

In addition, we include a rectifier-type load that is drawing a peak current of 0.35 p.u. For simplicity in discussion, it is assumed that the VSIs are lossless and supplied by a fixed DC battery, instead of the DC storage capacitor. The DSTATCOM parameters are (p.u.) $V_{DC}=1.5$: $R_f=0$: $X_f=\omega L_f=0.2$: $X_{filt}=1/\omega C_{filt}$: and $C_P=-0.1$.

The control is designed with $\mathbf{Q} = diag(1, 0, 50, 0)$ $R=0.05$. where *diag* is a diagonal matrix. The two most important variables for control are the terminal voltage followed by the current i_f. The weighting matrix $\mathbf{Q}$ reflects the importance of these variables. For this set of parameters, the gain matrix for phase a is then given by $\mathbf{K} = [3.25, 9.23, 30.35, -1.79]$. Using this feedback, the oscillatory closed-loop eigenvalues are to the left of the line $s=-7193$. To avoid the complexity of forming a reference for the load current, the gain matrix is restricted to $\mathbf{K} = [3.25, 9.23, 30.35, 0]$. This reduction in state feedback results in a minimal shift in the closed-loop eigenvalues to the left of $s = -7187$. Thus, stability is not at all endangered by the reduced feedback, but the computation is reduced considerably. Furthermore, the same feedback matrix designed for phase a is also used for the other two phases.

The system is robust and insensitive to changes in the load parameters. The load time constants are largely decoupled from converter dynamics. For load parameter (R_{la} and X_{la}) changes from 10% to 1000% of nominal, the worst case of the oscillatory eigenvalues of the closed-loop system was still left of $s = -7154$.

The DSTATCOM performance is shown in Figs. 6 and 7. Fig. 6*a* depicts the load currents. The compensator is connected at the end of the first half-cycle (10 ms) after the first fundamental extraction is completed or the first power average is obtained. The terminal voltages are shown in Fig. 6*b*. It can be seen that the terminal voltages become balanced sinusoids within about one cycle of the connection of the compensator. The compensator power is shown in Fig. 7*a*, and this quantity is plotted a little longer than the other quantities. It can be seen that, as soon as the DSTATCOM is pressed into service, the compensator supplies power to ride over the transient. However, it quickly settles down to zero mean oscillation, indicating the effectiveness of eqn. 8. Terminal voltage tracking error for phase *b*, shown in Fig. 7*b*, only proves the fast convergence of the algorithm.

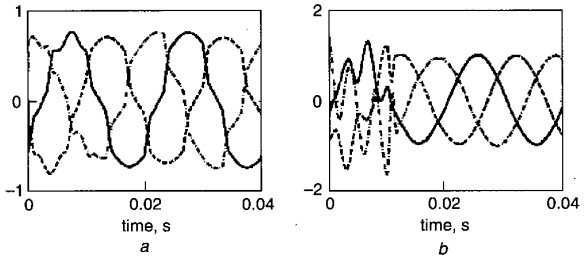

Fig. 6 *Performance of voltage-controlled DSTATCOM when source is unbalanced and load is both unbalanced and distorted. (a) load currents; (b) terminal voltages*

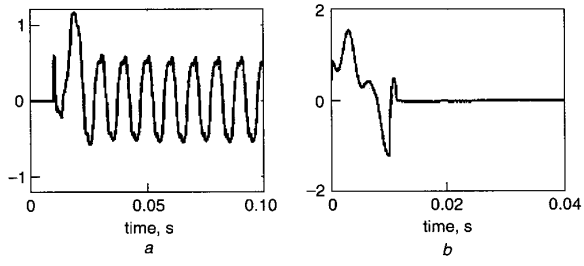

Fig. 7 *Performance of voltage-controlled DSTATCOM when source is unbalanced and load is both unbalanced and distorted. (a) compensator power; (b) voltage tracking error*

We now distort the source voltage by adding the 5th and 7th harmonics to it, with the magnitudes of the harmonic components being inversely proportional to their harmonic number. The source voltage is shown in Fig. 8*a*. The terminal voltage becomes a balanced sinusoid within about one cycle of connecting the compensator. This is shown in Fig. 8*b*. The shunt power and voltage tracking error for phase *a* are also shown, to indicate the effectiveness of the algorithm, see Fig. 9*a* and *b*.

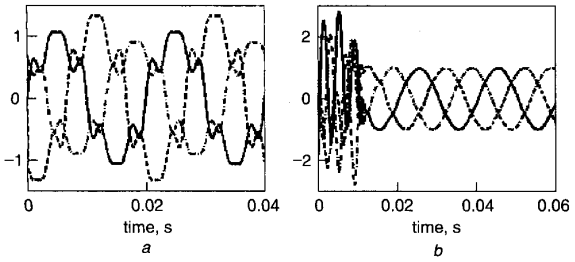

Fig. 8 *Performance of voltage-controlled DSTATCOM when both source and load are unbalanced and distorted. (a) source voltage; (b) terminal voltages*

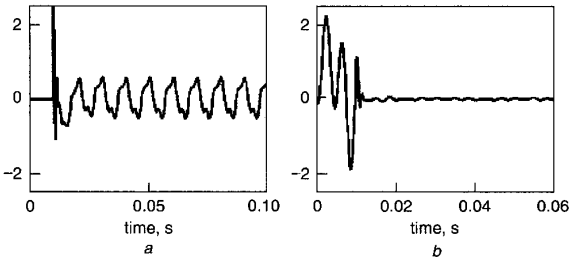

Fig. 9 *Performance of voltage-controlled DSTATCOM when both source and load are unbalanced and distorted. (a) compensator power; (b) voltage tracking error*

Let us now consider the case when there are random variations in the source voltage. We assume that the source is unbalanced and the load is both unbalanced and distorted. The source voltage, as shown in Fig. 10*a*, contains spikes of irregular height that appear randomly. Phase *b* of the uncompensated terminal voltage and source current are shown in Fig. 10*b* and 11*a*, respectively. Owing to the presence of the feeder inductance, these waveforms are not sinusoidal. The compensator is connected at the end of the first half-cycle, and the compensated terminal voltages are shown in Fig. 11*b*. It can be seen that the terminal voltages become balanced sinusoids within two cycles of the connection of the compensator. Note, however, that the glitches in the supply voltage are smoothed by the feeder inductance, thereby providing an opportunity for the DSTATCOM to correct. If the flicker voltage source was very close to the terminal bus itself, it would be impossible for the DSTATCOM to correct it fully due to the limited bandwidth of the VSIs. Note that the switching frequency of the inverters, when operated in the two-level mode, is less than 6.5 kHz for all the cases mentioned in this example.

The above example shows that the DSTATCOM used in the voltage control mode is capable of correcting current harmonics down the radial line, as well as voltage harmonics on the source side. Thus, under this

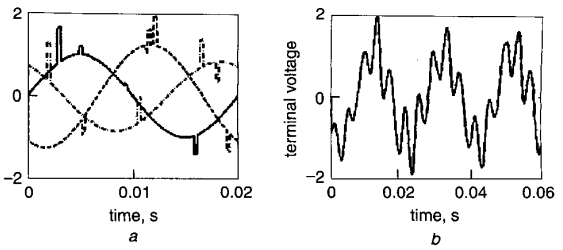

Fig. 10 *Elimination of voltage flicker using DSTATCOM in voltage control mode. (a) source voltages; (b) uncompensated*

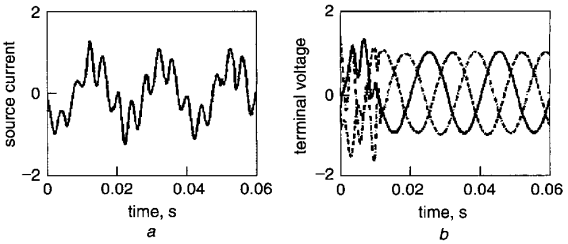

Fig. 11 *Elimination of voltage flicker using DSTATCOM in voltage control mode. (a) uncompensated; (b) compensated*

operation mode, the DSTATCOM is an ideal utility-maintained device that can clean the voltage of a particular load bus.

5 DSTATCOM in current control mode

In this mode, it is assumed that the installation and maintenance of the DSTATCOM is the duty of an individual customer, so that the load does not disturb other customers with its unbalance or harmonic distortion. This may be a very stringent condition on the customer, especially when the supply-side voltage is unbalanced or distorted. Nevertheless, we present some design approaches, based on which the customer can draw sinusoidal current from the feeder. We consider three different cases:

(i) when both source and load are unbalanced.

(ii) when both source and load are unbalanced, and the load is distorted.

(iii) when both source and load are unbalanced as well as distorted.

5.1 Case (i): load and source unbalanced

The reference for the terminal voltage is obtained through the Fourier extraction of the fundamental voltage, i.e. $v_{t-ref} = v_{t-fund}$. Once this reference is obtained, it is easy to obtain a reference for the current through the filter capacitor. To extract a reference for the injected shunt current, we note that the source current must be a fundamental positive sequence. Since $i_l = i_s + i_f$, the compensator must supply the negative and zero sequence required by the load current. We can then write

$$\left.\begin{aligned} i_{f0-ref} &= i_{l0} \\ i_{f2-ref} &= i_{l2} \\ i_{f1-ref} &= 0 \end{aligned}\right\} \tag{10}$$

where $_0$, $_1$ and $_2$ indicate zero, positive and negative sequences, respectively. An algorithm to extract the

sequence components from their samples is given in Appendix 9.2. This algorithm uses a moving average of a half-cycle to extract the RMS sequence components. Once they are obtained, we can use an inverse sequence transform to set the reference value. Note that, since the DSTATCOM only the injects negative and zero sequence of the load current, it supplies no real power.

5.2 Case (ii): load and source unbalanced and load contains harmonics

The reference for the terminal voltage and current through the filter capacitor is obtained in the same way as Case (i). However, to extract the reference for the injected current, we must remember that the compensator should not only supply the sequence currents given in eqn. 10, but also should supply the harmonic content of the load. To facilitate this, let us assume that we have obtained i_{f-ref} from the inverse transformation of i_{f0-ref}, i_{f1-ref} and i_{f2-ref} given in eqn. 10. We then use the following relation to modify the i_{f-ref}:

$$i_{f-ref} = i_{f-ref} + i_l - i_{l-fund} \tag{11}$$

5.3 Case (iii): load and source unbalanced and distorted

This is the case in which we assume that both the source voltages and load currents are distorted by harmonics. This case has to be treated differently to the previous two cases as the generation of references is of a completely different nature. Consider the equivalent circuit of Fig. 3. If we want the source current to be balanced and harmonic-free, then the terminal voltage must contain exactly the same amount of harmonics as the source. The reference for the injected current must be extracted in the same way as given by eqns. 8 and 9. However, the reference for terminal voltage must then be

$$v_{t-ref} = v_{t-fund} + v_{s-harm} \tag{12}$$

where v_{s-harm} is the harmonic content of the source. Typically, the source does not contain any even harmonics and for phase a is

$$v_{s-harm} = \sum_{n=3,5,7,\cdots} V_{san} \sin(n\omega t) \tag{13}$$

Since $\dot{v}_t = i_{filt}/C_{filt}$, the reference for the current through the filter-capacitor is then easily obtained from eqns. 12 and 13.

Example 2: Let us consider the same system as given in Example 1, except that in this case the load is given at a particular bus and the Thevenin equivalent is for the rest of the system. The control is designed with $Q = diag(30, 0, 1, 0)$ $R = 0.05$, which puts a higher gain on the injected current. The gain matrix is then obtained as $K = [23.97, 5.67, 11.47, -3.39]$. Using this feedback, the oscillatory closed-loop eigenvalues are to the left of the line $s = -2529$. However, as mentioned above, we use a reduced feedback of $K = [23.97, 5.67, 11.47, 0]$. Using this reduced feedback, the dominant closed-loop eigenvalues are to the left of $s = -2476$, which is a marginal stability reduction. A load change to 10% of the nominal inductance gave a boundary shift to $s = -1836$, which shows the design is quite robust.

We assume that the source is distorted with the 5th and 7th harmonics, and the source voltage is the same as shown in Fig. 8*a*. The reference for the terminal voltage is generated from eqn. 10, assuming that the source voltage is completely measurable. The results are shown in Figs. 12 and 13. The compensator is connected at the end of the first half-cycle. The source currents become balanced before the end of the second cycle, as evident from Fig. 12*a*. The terminal voltages are shown in Fig. 12*b*. The phase *a* source and terminal voltage are plotted in Fig. 13*a*. It can be seen that they both contain the same harmonics of similar magnitude, since for zero harmonic current to flow, the DSTATCOM must create a harmonic voltage equal to the voltage source harmonics. To illustrate the tracking performance, the reference and actual injected current waveforms for phase *a* are plotted in Fig. 13*b*. This current tracks the reference within a half-cycle.

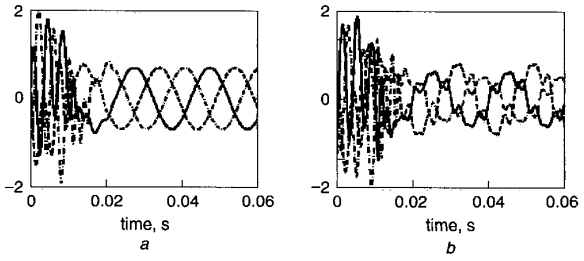

Fig. 12 *Performance of current-controlled DSTATCOM when measurement of source voltage is available. (a) source currents; (b) terminal voltages*

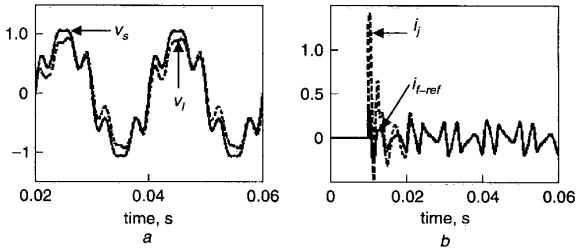

Fig. 13 *Performance of current-controlled DSTATCOM when measurement of source voltage is available. (a) source and terminal voltages; (b) injected current*

In this example, we have assumed that the measurement of the source voltage is completely available. This is not a valid assumption, as the source may be remotely located and is most likely a Thevenin voltage source in a radially connected distribution system. We must therefore estimate the harmonic content of the source voltage from the measured data. This can be easily done when the feeder impedance is completely known. Referring to Fig. 3, we can determine the 5th harmonic component of the source voltage through the measurement of the 5th harmonic component of the terminal voltage and source current as

$$\vec{V}_{s5} = \vec{V}_{t5} + (R + j5\omega X)\vec{I}_{s5} \tag{14}$$

where $\rightarrow$ indicates a phasor quantity. Thus, assuming that the feeder impedance is completely known, we can estimate the 5th harmonic component of source voltage as follows.

(*a*) Before the compensator is connected, estimate the 5th harmonic component of the terminal voltage and source current, and use them in the above relation to estimate the 5th harmonic of the source voltage.

(*b*) Use this value to set a reference for the terminal voltage through eqn. 10. The reference current through the filter capacitor is also set using this.

(*c*) Once the controller tracking system converges, the 5th harmonic component of the source current is zero and we have $\vec{V}_{s5} = \vec{V}_{t5}$.

A similar operation must also be performed for all odd harmonic components up to a defined order.

It is further unrealistic to expect that the feeder impedance of Fig. 3 is completely known, as it may also be a Thevenin impedance. A straightforward use of the above algorithm is then not possible. Fortunately, however, estimation of the entire feeder impedance is not necessary for the extraction of the terminal voltage reference. The circuit to the point of common coupling can be viewed as a uniformly distributed feeder that is supplied by a stiff source. We thus need the voltage at any point on this feeder and the corresponding impedance. We call the procedure of estimating the voltage using a fractional value of the Thevenin impedance 'partial back-projection'. For example, a 50% back-projection will mean using $0.5(R+jn\omega X)$ in computing the source voltage of the nth harmonic. The proof of this reference extraction convergence is given in Appendix 9.3, under the assumption that the harmonic values are used after the circuit reaches steady state.

Example 3: As developed in Appendix 9.3, the stability of the reference formulation depends on the eigenvalues of

$$P\left[jn\omega I - \left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\right]^{-1}\left\{jn\omega\frac{\Gamma_2 K}{K\Gamma_2}\right\} \qquad (15)$$

inside the unit circle. Ignoring the load, the three states of Fig. 3 are i_f, v_t and i_{filt}. In current tracking mode, the reference for i_f is known. The reference for v_t should be found by back-projection of the measured harmonic v_t to the source. The matrix P in eqn. 15 expresses this estimate of the back-projected voltage and the corresponding filter current at a particular harmonic, in terms of the measured harmonic voltage.

Let us consider the same system as in Example 2 with the same set of controller gains. The worst damped eigenvalues for two different amounts of back-projection are shown in Fig. 14, where the dominant eigenvalues for different value odd harmonics are indicated by ●. The unit circle is also indicated. It can be seen that all harmonic eigenvalues of the system are stable for a back-projection of 75%. However, for a back-projection of 250%, all eigenvalues are unstable, except for the fundamental and 3rd harmonic.

We now use partial back projection in the simulation studies. Figs. 15 and 16 show the source currents obtained with four different back-projections. The feedback system is not stable, and the source currents never become sinusoidal for 25% back-projection. For 50% back-projection, the source currents settle in about three cycles, whereas they settle down within two cycles for 75% back-projection. The source currents take considerably longer to settle for 150% back-projection. In fact, through the simulation studies, it was observed that the system attains steady state with perfect tracking when the amount of back-projection is limited between 40% and 160%. Note that there is a slight discrepancy between the results obtained using the simulation studies and that obtained using the convergence proof of Appendix 9.3. In the proof, we have assumed that the system first reaches steady state before we extract the harmonic components. In the simulation, however, the harmonic components are extracted as we move along in time using the moving averaging. The results obtained through the simulation will show a lower range of stability than the convergence formula.

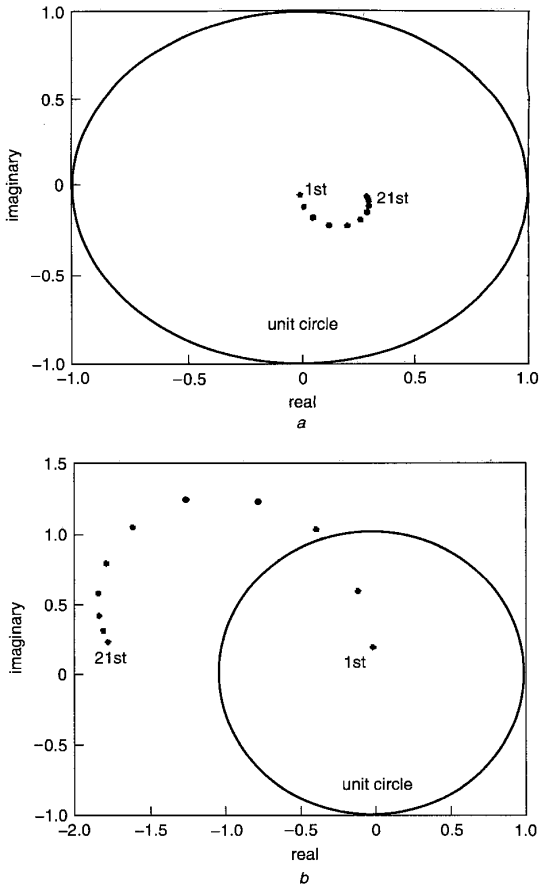

Fig. 14 *System eigenvalues for two different back-projections. (a) 75% back-projection; (b) 250% back-projection*

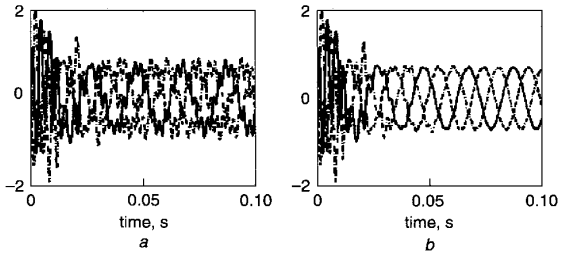

Fig. 15 *Source currents with four different back-projections. (a) 25% back-projection; (b) 50% back-projection*

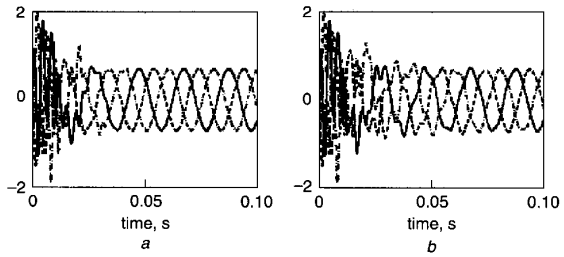

Fig. 16 *Source currents with four different back-projections. (a) 75% back-projection; (b) 150% back-projection*

Another important point to note is that, if the back-projection is below 40%, then the instability in the reference quantities is limited by the operation of pulse-width-modulated VSI. This will result in distortion in source currents, but will not diverge because of the finite gain of the inverter. However, if the back-projection is over 250%, the unstable 5th and 7th harmonics will swamp the fundamental and the whole system will collapse. The example, however, clearly demonstrates that if we use a reasonable estimate of the feeder impedance (including Thevenin impedance, if any), the compensator will be able to correct for the current harmonic at the load side, as well as for the voltage harmonic on the source side.

6 DC capacitor control

So far, we have assumed that a DC source, rather than a DC capacitor, supplies the VSIs of the DSTATCOM. We have further assumed that the compensator is lossless (R_f=0). This is again an invalid assumption, as there are always switching losses and losses in the connecting transformer. These losses will force the DC capacitor to discharge, resulting in a loss of tracking. It is therefore imperative that the DC voltage stored (V_{DC}) in the storage capacitor C_{DC} is maintained around a pre-specified set value. This is only possible by drawing additional power to overcome the losses due to R_f. We present two different control strategies for the two DSTATCOM operating modes.

6.1 DSTATCOM in voltage control mode

We refer to eqn. 8, through which the angle of the reference terminal voltage of the DSTATCOM is computed, in order to force the real power drawn by the DSTATCOM to zero. Since the aim is to draw real power from the source, we now modify this equation. To maintain the capacitor voltage as constant, a negative feedback of this voltage is added in the angle computation as

$$\phi_a(k+1) = \phi_a(k) + C_P p_{f\_av} + C_V\left(V_{DC}^{ref} - V_{DC}^{cyl}\right) \quad (16)$$

where C_v is constant: V_{DC}^{rev} is the reference value of the DC capacitor voltage; and V_{DC}^{cyl} is the average value of the DC capacitor voltage. To influence the control rapidly, we have chosen this average to be the running average.

6.2 DSTATCOM in current control mode

We refer to eqn. 10, which gives the relation for the reference shunt currents in this mode. The equation is derived assuming that the fundamental positive sequence of the source current is equal to that of the load current. This assumption will no longer be true, as the positive sequence of the source current must be higher than its load current counterpart, in order to supply the real power requirement of the DC capacitor. The difference in the two currents will be forced through the shunt path. We can then modify eqn. 10 as

$$\left.\begin{aligned} i_{f0-ref} &= i_{l0} \\ i_{f2-ref} &= i_{l2} \\ i_{f1-ref} &= i_{DC} \end{aligned}\right\} \quad (17)$$

where i_{DC} is the current required by the DC capacitor to maintain its charge, and it must be obtained from the DC capacitor feedback loop.

The feedback should be able to correct the deviation of the average value of V_{DC} from a reference value V_{DC}^{ref}. In the simplest form of feedback, we have used a proportional-plus-integral (PI) controller to correct for any discharge in the capacitor voltage. The controller is then given by

$$u_c = K_P\left(V_{DC}^{ref} - V_{DC}^{cyl}\right) + K_I \int \left(V_{DC}^{ref} - V_{DC}^{cyl}\right) dt \quad (18)$$

where the average value of the DC capacitor voltage V_{DC}^{cyl} can either be measured at the end of a cycle or can be the moving average. The amount of u_c required to sustain the DC capacitor voltage must then be drawn equally from the three phases. As a result of which, we can substitute in eqn. 17.

$$i_{DC} = -u_c/3 \quad (19)$$

Example 4: Let us consider the same system as discussed above. We have assumed that the load side is harmonically distorted, whereas the source side is free of harmonics. We have removed the assumption that the compensator is lossless and have chosen the following p.u. quantities: R_f = 0.1 and $X_{DC} = 1/\omega C_{DC} = 0.106$. The PI controller parameters chosen are C_P = −0.1 and C_V = −0.15 for DSTATCOM in voltage control mode, and K_P = 7.5 and K_I = 12 for DSTATCOM in current control mode.

The system is started from rest, i.e. the compensator is connected at the end of the first half-cycle after the average load power is obtained. The capacitor is assumed to be precharged to 1.5 p.u. and this value is also chosen as the set point of this voltage. Both the controllers are started from zero initial condition. The results are shown in Figs. 17 and 18. It can be seen that the DC capacitor voltage settles within about 0.3 s for either case. The steady-state waveforms of the terminal voltage and source current are also plotted in these figures. It can be seen that these are balanced without any distortion. This implies that, for the DSTATCOM in the current control mode, the additional amount of real current required is distributed equally in the three phases. The power drawn by the DSTATCOM in the voltage control mode is also shown. It has a steady-state value of −0.02 p.u. indicating that the DSTATCOM is drawing power from the supply.

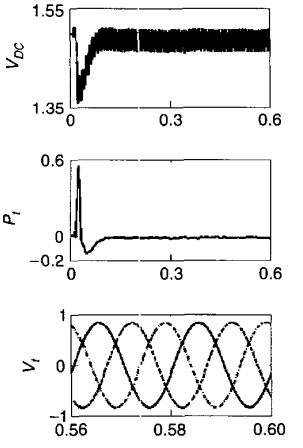

Fig. 17 *Performance of voltage-controlled DSTATCOM*

7 Conclusions

We have discussed a topology and a control technique of a flexible DSTATCOM that can be operated in either the voltage or current control mode. In the voltage control

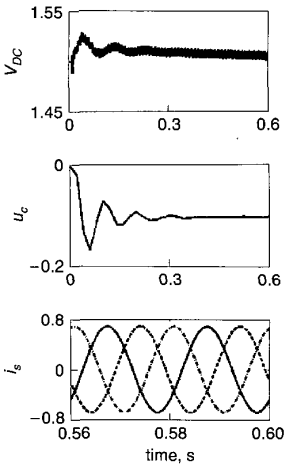

Fig. 18 *Performance of current-controlled DSTATCOM with DC capacitor control system*

mode, it can make a utility bus voltage sinusoidal against any unbalance, harmonic or flicker in the source voltage, or unbalance or harmonic in the load current within the bandwidth. Proper care has been taken in designing feedback control in this mode, such that the DSTATCOM need not inject real power in the steady state. A utility may operate a DSTATCOM in this mode for a particularly problematic bus from the point of view of voltage distortion. In the current control mode, a consumer can employ the DSTATCOM such that it can inject a balanced sinusoidal current in the AC system, irrespective of unbalance and distortion in its load.

We have further demonstrated that the DSTATCOM compensated load can draw a perfectly balanced current to the AC system, even when the supply side is unbalanced or distorted. To accomplish this, it is imperative that the voltage at the point of common coupling must have the same order of unbalance when the source is just unbalanced. This will require no additional hardware or computation, as the proposed control forces the voltage at the point of common coupling to the required unbalance, such that the source currents become balanced. To balance the source currents when the source voltages contain harmonics is a much more complicated problem, and it requires a lot more computation than any of the previous methods. This is because this problem requires the identification of each harmonic component. This is, however, a very stringent requirement on the consumer, as it may be unreasonable to expect that the consumer draws distortion-free current even when the supplied utility voltage is distorted. However, as we have demonstrated it is quite feasible to achieve such a control with added computation.

8 References

1 DUGAN, R.C., MCGRANAGHAN, M.F., and BEATY, H.W.: 'Electrical power systems quality' (McGraw Hill, New York, 1996)

2 AKAGI, H., KANAZAWA, Y., and NABAE, A.: 'Instantaneous reactive power compensators comprising switching devices without energy storage components', *IEEE Trans. Ind. Appl.*, 1984, **IA-20**, pp. 625–630

3 WATANABE, E.D., STEPHAN, R.M., and AREDES, M.: 'New concepts of instantaneous active and reactive powers in electrical systems with generic load', *IEEE Trans. Power Deliv.*, 1993, **8**, (2), pp. 697–703

4 PENG, F.Z., and LAI, J.S.: 'Generalized instantaneous reactive power theory for three-phase power systems', *IEEE Trans., Instrum. Meas.*, 1996, **45**, (1), pp. 293–297

5 GHOSH, A., and JOSHI, A.: 'A new approach to load balancing and power factor correction in power distribution system', *IEEE Trans. Power Deliv.*, 2000, **15**, (1), pp. 417–422

6 QUINN, C.A., and MOHAN, N.: 'Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase non-linear loads'. Applied Power Elect. Conf. APEC'92, 1992, pp. 829–836

7 MISHRA, M.K., GHOSH, A., and JOSHI, A.: 'A new STATCOM topology to compensate loads containing AC and DC components.' IEEE Winter Power Meeting 2000, Singapore

8 ANDERSON, B.D.O., and MOORE, J.B.: 'Linear optimal control' (Prentice-Hall, Englewood Cliffs, New Jersey, 1971)

9 LEDWICH, G.: 'Linear switching controller convergence', *IEE Proc., Control Theory Appl.*, 1995, **142**, (4), pp. 329–334

10 LYON, W.A.: 'Transient analysis of alternating-current machinery' (John Wiley, New York, 1954), Chap. 2

9 Appendix

9.1 Proof of tracking controller convergence

The system state-space description is given in eqn. 3 as

$$\dot{z} = \Lambda z + \Gamma_1 v_s + \Gamma_2 u \tag{20}$$

Let us form a reference that is defined by

$$\dot{z}_{ref} = \Lambda z_{ref} + \Gamma_1 v_s + \Gamma_2 u^* \tag{21}$$

Defining an error vector as $e = z - z_{ref}$, we can then write from the above two equations

$$\dot{e} = \Lambda e + \Gamma_2 (u - u^*) \tag{22}$$

From the control law given in eqn. 5, if we remain on the switching surface [8]

$$K(z - z_{ref}) \cong 0 \Rightarrow Ke \cong 0 \tag{23}$$

We can then write

$$K\dot{e} = 0 \Rightarrow K\Lambda e + K\Gamma_2 (u - u^*) = 0 \tag{24}$$

From eqn. 24, we obtain

$$(u - u^*) = -\frac{K\Lambda}{K\Gamma_2} e \tag{25}$$

Substituting eqn. 25 in eqn. 22, the error equation becomes

$$\dot{e} = \left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right) \Lambda e \tag{26}$$

Hence, the tracking error will converge to zero for any initial condition, provided that

(i) all the eigenvalues of the matrix $(I - \frac{\Gamma_2 K}{K\Gamma_2})\Lambda$ have negative real parts.

(ii) the reference signal can be generated by an equation in the form of eqn. 31.

(iii) since u is bounded between $+1$ and -1, eqn. 25 requires that $-1 \leq u^* - K\Lambda/K\Gamma_2 e \leq +1$.

It is a property of the switching law based on LQR design that condition (i) is satisfied. Most tracking problems are posed as the output of the plant following some reference y_{ref}. Our task is to define a state reference satisfying $y_{ref} = Hz_{ref}$. In the frequency domain, the output equation can be given as

$$Y_{ref}(s) = H(sI - \Lambda)^{-1} [\Gamma_1 V_s(s) + \Gamma_2 U^*(s)] \tag{27}$$

Assuming that we are tracking a single output, and since the plant in eqn. 20 is single input, we can write from eqn. 27

$$U^*(s) = \frac{1}{H(sI - \Lambda)^{-1}\Gamma_2} \left[Y_{ref}(s) - H(sI - \Lambda)^{-1} \Gamma_1 V_s(s) \right] \tag{28}$$

Thus, the corresponding reference state can be formed from

$$Z_{ref}(s) = (sI - \Lambda)^{-1}[\Gamma_1 V_s(s) + \Gamma_2 U^*(s)] \quad (29)$$

Hence, any single output-tracking problem can be translated into a state tracking problem and expressed in the form of eqn. 21. In practice, circuit analysis would be the easiest method to form z_{ref} from y_{ref}, particularly for sinusoidal tracking. This will satisfy condition (ii).

Condition (iii) cannot be truly satisfied for arbitrary references. Since the source v_s is always bounded, from eqn. 28 we can see that a bounded y_{ref} implies a bounded u^*. The system states are not necessarily bounded. However, if y_{ref} and the system states are sufficiently small, then condition (iii) can be satisfied and perfect tracking can occur.

9.2 Extracting sequence components from samples

Here we propose a method for the extraction of phasor symmetrical components of currents (or voltages) from their samples. For this, we utilise the method of instantaneous symmetrical components. For three-phase instantaneous currents i_a, i_b and i_c, this is defined as [10]

$$\begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (30)$$

where $a = e^{j120°}$. Note that i_{a0} is the zero-sequence vector, and i_{a1} and i_{a2} are two vectors that are complex conjugates of each other. A three-phase voltage can also be defined in a similar fashion.

Let us now denote the zero, positive and negative sequence phasors as I_{a0}, I_{a1} and I_{a2}, respectively. Defining a vector as $I_{a012}^T = [I_{a0}, I_{a1}, I_{a2}]$, we use the following to obtain the symmetrical component phasors:

$$I_{a012} = \frac{\sqrt{2}}{T} \int_{t_1}^{t_1+T} i_{a012} e^{-j(\omega t - 90°)} dt \quad (31)$$

where the time interval T is chosen as a half-cycle. Note that these vectors do not contain any odd harmonics even if the original signal contains harmonics, since eqn. 31 signifies the average over a half-cycle. This averaging can be between any two points that are a half-cycle apart and need not be synchronised with the zero crossing of the current (or voltage) waveform.

9.3 Condition for tracking reference convergence

The change from output tracking to state tracking is not a problem if the system model is known perfectly. The approach analysed here is where the reference for the switching controller is fixed for a period. The system reaches steady state. The voltages and currents of the circuit are then used to define the new reference values.

If we satisfy the stability and magnitude conditions, the system will stay in the tracking band and the system performance will approximate

$$K(z - z_{ref}) = 0 \quad (32)$$

This implies

$$K(\dot{z} - \dot{z}_{ref}) = 0 \quad (33)$$

For the system model given in eqn. 20 and eqn. 33 yields

$$K(\Lambda z + \Gamma_1 v_s + \Gamma_2 u - \dot{z}_{ref}) = 0 \quad (34)$$

The effective control in this mode can be found as

$$u_{eff} = -(K\Gamma_2)^{-1}(K\Lambda z + K\Gamma_1 v_s - K\dot{z}_{ref}) \quad (35)$$

Applying the control to the system eqn. 20 we obtain

$$\dot{z} = \Lambda z + \Gamma_1 v_s - \frac{\Gamma_2 K}{K\Gamma_2}\Lambda z - \frac{\Gamma_2 K}{K\Gamma_2}\Gamma_1 v_s - \frac{\Gamma_2 K}{K\Gamma_2}\dot{z}_{ref} \quad (36)$$

which is stable if the eigenvalues of $[I - \Gamma_2 K/K\Gamma_2]\Lambda$ are in the left half plane. We have also obtained this condition in Appendix 9.1. For an LQR-designed system this is guaranteed, provided that controller saturation is avoided.

Expressing this state space model in the frequency domain, when steady state is reached

$$Z(s) = \left[sI - \left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\right]^{-1} \times \left\{\left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\Gamma_1 V_s(s) + s\frac{\Gamma_2 K}{K\Gamma_2} Z_{ref}(s)\right\} \quad (37)$$

Expressing eqn. 37 for the nth harmonic

$$Z(jn\omega) = \left[jn\omega I - \left(\frac{I - \Gamma_2 K}{K\Gamma_2}\right)\Lambda\right]^{-1} \times \left\{\left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\Gamma_1 V_s(jn\omega) + jn\omega\frac{\Gamma_2 K}{K\Gamma_2} Z_{ref}(jn\omega)\right\} \quad (38)$$

If the reference value for the $k+1$ iteration is based on a linear combination of the output reference (y_{ref}) and the steady system solution for other system states, e.g.

$$Z_{ref}(jn\omega)_{k+1} = PZ(jn\omega)_k + TY_{ref}(jn\omega)_k \quad (39)$$

we obtain

$$Z_{ref}(jn\omega)_{k+1} = P\left[jn\omega I - \left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\right]^{-1} \times \left\{\left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\Gamma_1 V_s(jn\omega) + jn\omega\frac{\Gamma_2 K}{K\Gamma_2} Z_{ref}(jn\omega)_k\right\} + TY_{ref}(jn\omega)_k \quad (40)$$

The stability of the reference formulation depends on the eigenvalues of

$$P\left[jn\omega I - \left(I - \frac{\Gamma_2 K}{K\Gamma_2}\right)\Lambda\right]^{-1}\left\{jn\omega\frac{\Gamma_2 K}{K\Gamma_2}\right\} \quad (41)$$

being inside the unit circle.