Towards nanomemories: Ge growth on naturally and artificially nanostructured Si surfaces

Anna Sgarlata*, Adalberto Balzarotti*, Isabelle Berbezier[+], Pierre Szkutnik[+], Federico Rosei[#], Nunzio Motta[**]
*Dip Fisica, Univ. degli Studi di Roma/Tor Vergata, Via della Ricerca Scientifica 1 00173 Roma (Italy)
[+]L2MP – Polytech, Dpt Microelectronique et Telecommunication, IMT Technopole château Gombert, 13451 Marseille (France)
[#]INRS - Energie, Matériaux et Télécommunications, Université du Québec, 1650, Boul. Lionel – Boulet J3X 1S2 Varennes (Canada)
[**]School of Engineering Systems, Queensland University of Technology – GPO BOX 2434, Brisbane 4001 (Australia)
e.mail : n.motta@qut.edu.au

***Abstract*— Quantum dots (QDs) grown on semiconductors surfaces are actually the main researchers' interest for applications in the forecoming nanotechnology era like nanotransistors and nanomemories. Novel approaches to form ordered patterns of homogeneous nanostructures consist of natural patterning induced by surface instabilities, as step bunching of Si(111) or misoriented Si(001) surfaces, and of nanolithographic techniques, as Focused Ion Beam (FIB) or patterning by Scanning Tunneling Microscopy (STM). Based on the analysis of STM images and movies we report on growth and arrangement of Ge islands on nanopatterned silicon. Several issues are discussed: substrate nanostructuring using different techniques, wetting layer growth, transition up to 3D islands formation and arrangement of QDs to form nanomemories.**

Keywords- Quantum dots, nanopatterning; epitaxial growth;

I. INTRODUCTION

Quantum Dots (QD) grown on semiconductor surfaces represent an important area of focus for applications in nanotechnology. Usually 3D islands are named quantum dots (QD) if their dimension is less than the exciton Bohr radius, (24.3 nm in Ge). The heteroepitaxial self assembling of 3-D islands is one of the most promising paths towards the fabrication of QD devoted to nanoelectronic and nanophotonic applications. In particular, the growth of Ge on Si substrates is opening the possibility to integrate optoelectronics with today's Silicon technology [1,2]. To improve the performance of electronic devices, a considerable effort has to be devoted to control size uniformity, density and positioning of the self assembled nanostructures, as well as to shrink their dimensions [3]. Different techniques have been developed to achieve long-range ordering of islands with a very narrow distribution of sizes in the case of Ge/Si(001) system such as growth of stacked multilayers of heteroepitaxial islands [4] or deposition of thin relaxed films of SiGe [5]. Recently very interesting results have been achieved by using a combination of self-assembling QD growth and surface pre-patterning [6-10].

In nanolithography the potential of the single hole is important to stabilize the dots that are nucleating in the nearby region or at the edge [10-11]. Here the aim is to increase the density and to decrease the hole size in order to see how the dots ordering changes, but it must be considered that the perfect control of the holes shape, size and cleanliness is essential to reach the desired results.

We have demonstrated [10] that on Si(100) it is actually possible to form holes by using the STM tip, and that this procedure leads to a clean growth, without the presence of undesired material. However, this technique is limited to small area. Focused Ion Beam (FIB) is able to produce larger patterned area of holes 's arrays on the substrates with much higher throughput. Our experimental results throw light on several issues: substrate nanostructuring, three dimensional (3D) islands formation and arrangement of Qds by study of their lateral ordering and size [11].

II. EXPERIMENTAL

A. *Step bunching on Si(111)*

On Si(111) surfaces, direct current heating may create bunches of natural surface steps, yielding a simple way to obtain a nanopatterned substrate[8]. In a recent paper we have analyzed the evolution and distribution of the 3 Dimensional (3 D) islands that form after the completion of the Wetting Layer (WL) during the growth of Ge on both regular (R) and step-bunched (SB) Si(111) surfaces kept at 450 °C [9]. By varying surface preparation, we found an evident self-ordering on SB surfaces. Initially, triangular islands nucleate and evolve at step edges, rounding their corners up to complete ripening, forming long ribbons. Subsequently, island nucleation takes place at the center of flat terraces. In scanning tunneling microscopy images Ge islands appear to be regularly spaced, with an average distance of about 0.5 µm.

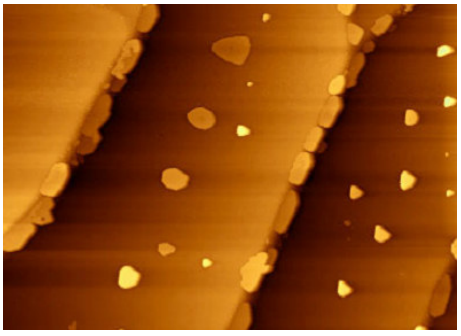

Figure 1. 3.7µmx2.7µm STM image of Ge islands grown at 450°C on Si(111) 1 µm wide terraces obtained by self organization of natural surface steps. The total z range is 80.5 nm.

B. *Ripples on GeSi/Si(100)*

Regular ripples on Si(100) vicinal surfaces can be created by growth instability, exploiting MBE growth of small lattice mismatched GeSi/Si multilayers. We have used Si(100) substrates 10° misoriented in the [110] direction, corresponding to the Si(118) surface, and a Ge_xSi_{1-x} alloy to obtain ripples of the desired wavelength [7] by varying the alloy composition x. Ge/Si nanostructures were grown using solid-source molecular beam epitaxy equipment with a background pressure in the 10^{-11} Torr range.. After 1100 °C *in situ* flashing, a Si buffer layer 50 nm thick is evaporated at 750 °C to obtain a perfectly clean reproducible vicinal surface. Ge and Sb were evaporated from effusion Knudsen cells. A regular ripple structure perpendicular to the step edge develops by evaporating a layer of Ge_xSi_{1-x} alloy at 600 °C on this substrate.

We have deposited on this substrate a surfactant Sb layer before the final Ge layer. A good alignment of the Ge islands could be obtained when the ripple wavelength was of the order of two times the island size. At x=0.5 the typical ripple wavelength was 100 nm, and nice aligned Ge small islands (50 nm typical lateral size) have grown on top of the undulations and at the bottom of the grooves (Fig.2).

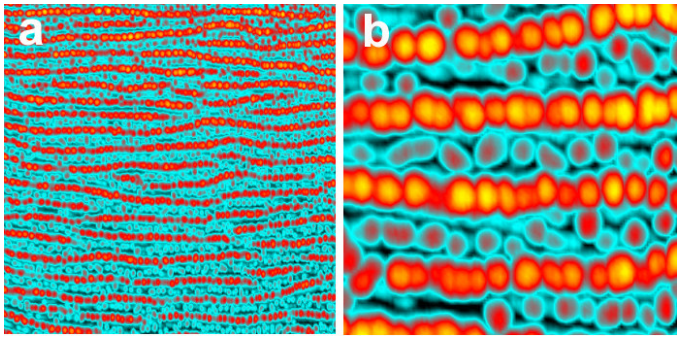

Figure 2. AFM false color images of Ge deposited on a $Ge_{0.5}$ $Si_{0.5}$/Si(118) substrate pattern, obtained at CRMC2-CNRS (Marseille-France) by Molecular Beam Epitaxy with different amount of Sb as a surfactant. The procedure consists in the deposition of a 13 ML layer of $Ge_{0.5}$ $Si_{0.5}$ at 600 ° C on a Si(118) 10º misoriented substrate to obtain a template of periodic ripples with an average wavelength of 90 nm followed by the deposition of 0.5 ML of Sb at ° 400 C. a) (2µm x 2µm) b) (0.5µm x 0.5µm). The lateral size of the islands is about 50 nm.

C. *Nanolithography*

1) *Holes in the WL by STM*

In STM Nanolithography arrays of pits are produced by interrupting feedback and lowering by a z-pulse the STM tip at selected locations, creating preferential nucleation site for islands growth. The Si(100) surface was nanopatterned at 500°C by using STM lithography. At selected positions, pits were elaborated by approaching the STM tip to the surface. The array re-imaged during the next scan, allows us to establish that pits have diameters ranging from 8 to 15 nm, a depth of 1-2 monolayers (ML) and the distance between them is 60±5 nm (Fig 3a). Starting from this kind of surfaces we have followed in real-time the WL growth (Fig 3b and 3c), the formation of an intermediate stage called pre-pyramid and finally the formation of hut clusters [10]. The 2D-3D transition takes place between 3 and 4 ML of Ge coverage. In this sequence of images (250x80x3) nm^3, two different states can be identified: the first stage corresponds to a pre-pyramid, while the second one to a pyramidal hut. Quantitative information on the growth mechanism can be obtained from the volume of the hut as a function of thickness [10].

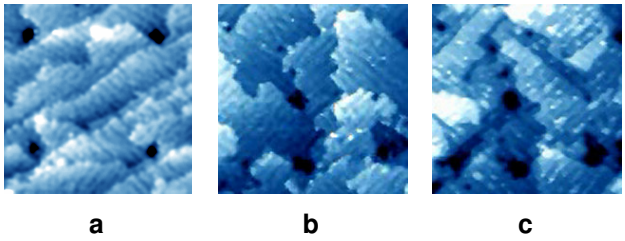

Figure 3. STM microscopic images of the formation of the wetting layer around holes on Si(100) during Ge deposition at 600 °C. a) 100x100 nm image of holes on the bare Si(100) surface after 1 hour annealing at 600 °C. b) 70x70 nm image after 0.87 ML Ge deposition. b) 70x70 nm image after 1.24 ML Ge deposition.

2) *Clean Si(001) FIB patterned substrates*

We have studied also Ge growth on Si(001) substrates patterned by FIB [11, 12]. After FIB patterning, a chemical cleaning in HCl followed by a Rapid Thermal Annealing at 1300K for 1 minute in N_2 has been applied to remove Ga atoms below $4x10^{16}cm^{-3}$. In the UHV chamber an annealing at 873K for about 30 min produces the desorption of the residual contamination from the surface. We have compared the growth on non-patterned and patterned areas where FIB holes (depths 30nm, diameters 150nm, pitch of 780 nm) have been produced. On patterned areas a good matching between pits and islands is found (Fig 4). In Fig. 4(b) we have indicated the corresponding position of pyramids and domes with respect to that of visible and hidden pits. All pyramids (except one) start nucleating nearby a pit and then grow over the pit. We conclude that nucleation starts preferentially at the border of pits. Subsequently islands, increasing their size, evolve to large domes which cover the underlying pits array.

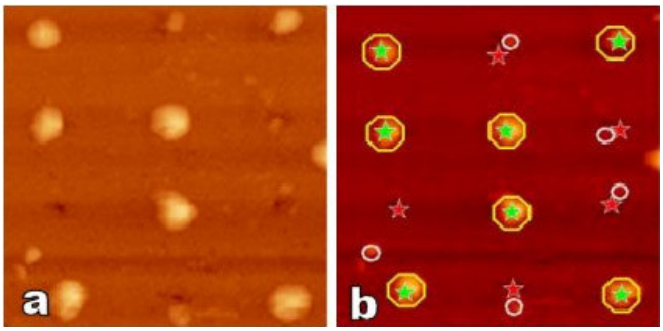

Figure 4. a) STM (2.5µmx2.5µm) microscopic image of the island morphology and position on a FIB Si(100) patterned surface. b) Identification of the image features. Red star: empty hole. Green star: covered hole. Circle: pyramid island. Octagon: dome island

3) *Oxidized Si(001) FIB patterned substrates*

It is well known that Ge doesn't stick on SiO_2, and Ge droplets are formed instead. This effect has been exploited in

order to obtain at the same time smaller Ge dots and electrical insulation in view of the applications of these dots as memory cells.

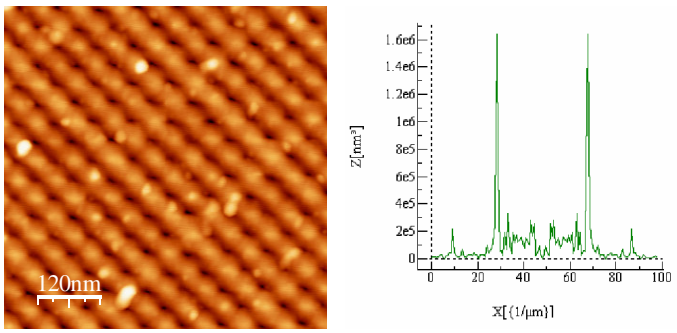

Figure 5. AFM (0.6μmx0.6μm) image of a SiO_2/Si(100) FIB nanopatterned surface (left). The Fast Fourier Transform of the AFM image (right) has been used to determine the average distance between the holes $\ell = (51 \pm 1)$ nm. The average depth of the holes is 4 nm.

An amorphous Ge layer is deposited at low temperature (room temperature) by using a Ge Knudsen cell, than droplets are formed by annealing at 500°C. Self organization of these droplets is expected to be influenced by FIB patterning.

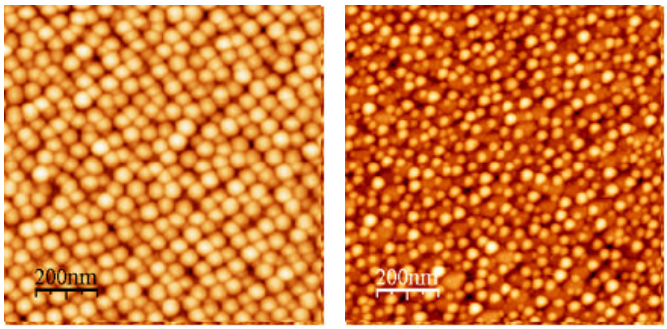

Figure 6. AFM images (1μm x 1μm) of a surface after deposition of 3 ML of Ge at 500°C on a FIB patterned area (a) and on a non patterned area (b). In the left image the average distance between islands is 50.5±0.5 nm, their diameter is 30.9±0.7 nm ,and their height 9.4±0.6 nm.

The procedure has the advantage of the growth of Ge dots directly on a tunnel oxide on FIB patterned substrates. By depositing 2ML of Ge, aligned small islands are nucleated inside the FIB holes, but a localization of Ge islands cannot be determined for sure. After a deposition of 3-4ML of Ge a regular distribution of dots appears on the surface. An AFM image of Ge droplets formed on a FIB patterned substrate (figure 6a) is shown in comparison with an image obtained from a non patterned area (figure 6b).

In Fig 7 the height distribution for the two samples of Fig 6 (after 3 ML deposition) is compared. It is evident the narrowing of the Gaussian distribution in the patterned area, confirming that the patterning works also as a way to improve the island uniformity. In Table 1 we show the measurements of dot distances and diameters obtained after a deposition of 3 ML.

TABLE 1 Average values for Ge droplets formed on the ordered FIB samples. All dimensions are in nm.

Ge thickness	Dot distance	Diameter	Height
3ML	50.5±0.5	30.9±0.7	17.8±4.2

In the case of dense arrays of FIB pits we have demonstrated that the FIB patterns induce a very good ordering and a size uniformity in the Ge islands. This result comes from the comparison with the random nucleation obtained on the same sample on non patterned areas. The annealing process produces an improvement in the narrowness of the distribution of the islands size. Both AFM and STM were used to image these islands and to measure their pitch distance. Pit densities as large as 4.3×10^{10} cm^{-2} have been measured.

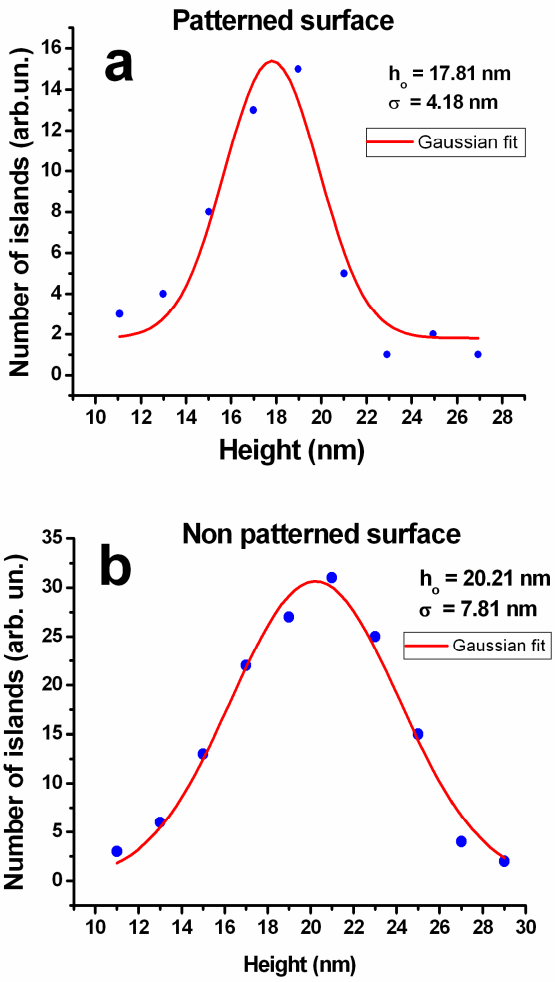

Figure 7. Height distribution of islands in patterned (a) and on a non patterned areas (b) after deposition of 3 ML Ge. The average height on the patterned areas is 17.8±0.2 nm, (σ = FWHM = 4.18 nm) while on the non-patterned areas the average height is 20.21 nm, and σ=7.81 nm

D. *Concept and construction of a memory cell*

Two main effects are involved in a semiconductor nanocrystal memory: quantum confinement and quantum dot charging and Coulomb blockade. Quantum confinement becomes comparable with the charging energy only for very small dot sizes (~1nm). For larger nanocrystals, simplified assumptions may be used, namely that only single charging effects are involved. The Coulomb charging energy ($q^2/2C$) is inversely proportional to the total capacitance C of the quantum dot. For a dot size of 5nm the charging energy is larger than KT even at room temperature. Ge nanocrystals present some advantages compared with Si nanocrystals for memory operation. They are related with the higher band offset of Ge on Si valence band. A p-channel MOSFET with Ge nanocrystals in the gate stack is so expected to show better retention characteristics compared with its silicon nanocrystal counterpart.

Lateral ordering of the Ge nanocrystals in the layer is expected to boost the performances compared to Si memories, where the nanocrystals are formed at random locations. By a precise control of the single nanocrystal position, the performance of memories may be also controlled by monitoring dot size and inter-dot distance. The operation of the memory may be modeled by considering a number of single quantum dot memories in parallel, taking into account dot-to-dot interaction. By using Ge quantum dots embedded in SiO_2 layer, we have established a protocol to create a memory cell. We have developed prototypes of these memories (Fig.8) following this protocol: after FIB patterning of a 5-10 nm thick oxide layer (tunnel oxide) and deposition of Ge at RT, the sample is annealed to form the Ge dots, and a control oxide is deposited to wrap the dots. The metallic gate and a source and drain doped areas are created by subsequent lithographic steps. A number of intermediate steps are actually needed to arrive to a working nanocrystal memory, since careful cleaning and removal of intermediate oxide layers is required to get rid of all the contaminations.

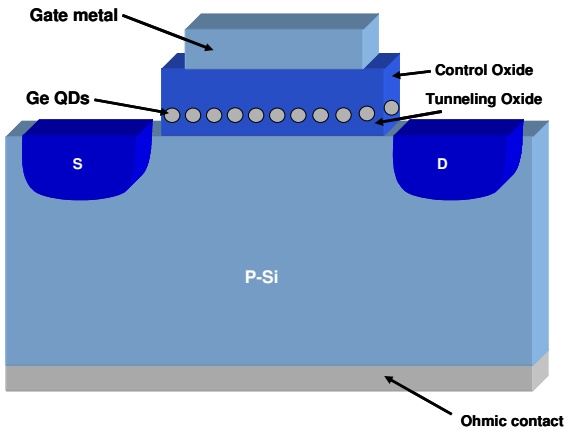

Figure 8. Schematic representation of a Ge nanocrystal memory cell

CONCLUSIONS

We have compared the growth and arrangement of Ge islands on Si(001) substrates nanopatterned using different approaches. The natural method based on the regular step bunching on Si(111) surfaces produces Ge islands aligned at the centre of terraces and regularly distributed at an average distance of 0.36 µm. Unfortunately these islands are too large to be used for nanoelectronic applications. The second, based on the self organization of a Si(001) misoriented surface covered by a thin layer of a GeSi alloy and a fraction of monolayer of Sb, produces densely packed islands with average diameter less than 50 nm. STM has also been used to produce ultra-small holes (10 nm) in a Si substrate, and to follow the growth of the Ge dots. While this approach is very interesting to understand the basics of the dot formation, it is slow and not suited to an industrial process. The fourth approach exploit the tight pattern created by FIB both on bare and oxidized Si(001) substrates. This method needs a very careful treatment of the substrate in order to remove all the contamination without perturbing the holes array. Well ordered arrays of Ge QDs with 50nm spacing (density of $4.1 \times 10^{10} cm^{-2}$) have been obtained, and a prototype of Ge nanocrystal memory has been demonstrated.

ACKNOWLEDGMENT

This work was supported by the European Community (EC) through FORUM-FIB contract (IST-2000-29573) at Roma Tor Vergata University and CRMC2-CNRS (Marseille).

REFERENCES

[1] J. Stangl, V. Holy and G. Bauer, Rev Mod Phys 76 (2004) 725.
[2] Y.-H. Kuo, Y. Kyu Lee, Yangsi Ge, S. Ren, J. E. Roth, T. I. Kamins, David A. B. Miller, and J. S. Harris. Nature 437, (2005) 1334.
[3] M. Goryll , L. Vescan and H. Lüth, Mater. Sci. Eng. B 101 (2003) 9.
[4] G. Capellini, M. De Seta, C. Spinella, F. Evangelisti, Appl. Phys. Lett. 82 (2003) 1772.
[5] C.Teichert, C. Hofer, K. Lyutovich, M. Bauer and E. Kasper, Thin Solid Film 380 (2000) 25.
[6] S. Kohmoto, H. Nakamura, T. Ishikawa, and K. Asakawa, Appl. Phys. Lett. **75**, (1999) 3488.
[7] I. Berbezier, A. Ronda, and A. Portavoce, N. Motta, Appl. Phys. Lett., 83, (2003) 4833.
[8] J.J. Metois, S. Stoyanov, Surf. Sci. 440 (1999) 407.
[9] A. Sgarlata, P. D. Szkutnik , A. Balzarotti, N. Motta, F. Rosei, Appl, Phys, Lett, 83, (2003) 4002.
[10] P. D. Szkutnik, A. Sgarlata, S. Nufris, N. Motta, and A. Balzarotti, Phys. Rev. B 69, (2004) 201309.
[11] A. Sgarlata, P.D.Szkutnik, A.Balzarotti , N.Motta, Proc IVC-16, AIV-17, ICSS12, NANO8, Cinema Festival Palace, (2004), in press.
[12] A. Karmous, A. Cuenat, A. Ronda, I. Berbezier , S. Atha, R. Hull, Appl. Phys. Lett. 85 (2004)