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Ramon B. Salazar
Birck Nanotechnology Center, Purdue University

Saumitra R. Mehrotra
Network for Computational Nanotechnology, Purdue University

Gerhard Klimeck
Network for Computational Nanotechnology, Purdue University, gekco@purdue.edu

Navab Singh
Institute of Microelectronics, Agency for Science, Technology, and Research, Singapore

Joerg Appenzeller
Birck Nanotechnology Center, Purdue University

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Observation of 1D Behavior in Si Nanowires: Toward High-Performance TFETs

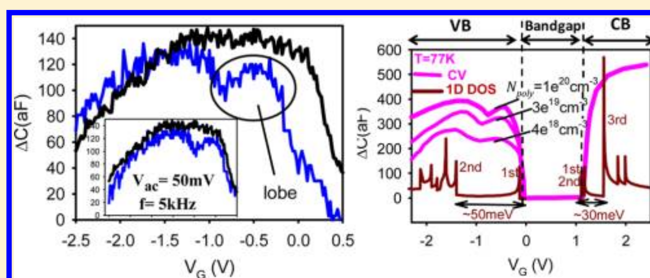
Ramon B. Salazar,*[†] Saumitra R. Mehrotra,[‡,†] Gerhard Klimeck,[‡,†] Navab Singh,[§] and Joerg Appenzeller[†]

[†]Birck Nanotechnology Center, Purdue University, 1205 W. State Street, West Lafayette, Indiana 47907, United States

[‡]Network for Computational Nanotechnology, 207 S. Martin Jischke Drive, West Lafayette, Indiana 47907, United States

[§]Institute of Microelectronics, Agency for Science, Technology, and Research (A*STAR), Singapore

ABSTRACT: This article provides experimental evidence of one-dimensional behavior of silicon (Si) nanowires (NWs) at low-temperature through both transfer (I_d−V_G) and capacitance−voltage characteristics. For the first time, operation of Si NWs in the quantum capacitance limit (QCL) is experimentally demonstrated and quantitatively analyzed. This is of relevance since working in the QCL may allow, e.g., tunneling field-effect transistors (TFETs) to achieve higher on-state currents (I_{on}) and larger on-/off-state current ratios (I_{on}/I_{off}), thus addressing one of the most severe limitations of TFETs. Comparison of the experimental data with simulations finds excellent agreement using a simple capacitor model.



KEYWORDS: *Sub-bands, one-dimensional, silicon, nanowire, capacitance, TFET*

In the quest to find an energy-efficient switching device, the tunneling field-effect transistor (TFET) is one of the most promising routes. TFETs have the potential to operate at low voltages[1−4] due to an inverse subthreshold slope (S) which is smaller than 60 mV/dec at room temperature as found in traditional complementary metal-oxide semiconductor (CMOS) FETs.[5,6]

To compete with CMOS technology, TFETs not only need to exhibit a small S but also should allow for a high on-state current (I_{on}) and a low off-state current (I_{off}) so that I_{on}/I_{off} is high.[7] To achieve this, the parameters that determine the behavior of TFETs must be optimized. Many of these parameters can be studied within the Wentzel−Kramers−Brillouin (WKB) approximation, where the tunneling transmission probability (T_D) is given by[8,9]

$$T_D \propto \exp\left(-\frac{4\lambda_{ch}\sqrt{2m^*}E_g^{3/2}}{3\hbar(E_g + q\Delta\varphi_{ch})}\right) \propto \exp\left(-\frac{4\lambda_{ch}\sqrt{2m^*}E_g^{3/2}}{3\hbar\left(E_g + q\frac{C_{ox}}{C_{ox}+C_q}\Delta V_G\right)}\right) \quad (1)$$

Although WKB is numerically accurate only for semiconductors with direct bandgap,[10] it can be shown that for semiconductors with indirect bandgap WKB predicts similar trends to those found with more rigorous calculations.[3,8,10] The optimization of parameters, such as the bandgap (E_g), the tunneling distance (λ_{ch}), and the effective mass (m^*), in (eq 1) has been extensively discussed in literature.[3,4,6,11−14] However, there is one performance parameter which is often overlooked: the quantum capacitance limit (QCL).[4,15,16] While the impact of the QCL on various figures of merit, such as the gate delay and power-delay product, has been studied theoretically,[3,4,6,15] little experimental work has focused on this topic. To the best of our knowledge, only two experimental studies in carbon nanotubes (CNTs) demonstrated operation in the QCL for one-dimensional (1D) structures.[17,18] However, its impact on the performance of TFETs was not discussed. Due to the nature of the working principle in TFETs,[3,4,7] such devices have significantly lower I_{on} compared to classical devices which operate in the charge control limit (CCL).[6]

To appreciate the impact of the QCL on I_{on} of TFETs, consider the ratio $C_{ox}/C_{ox} + C_q$ in (eq 1), which hereinafter will be referred to as the "quantum capacitance factor (QCF)". We define QCF $\equiv \partial\phi_{ch}/\partial V_G = C_{ox}/C_{ox} + C_q$, where C_{ox} is the oxide capacitance and C_q is the quantum capacitance.[4,15−19] In the QCL (when $C_q \ll C_{ox}$) the QCF reaches its maximum (QCF = 1) even in the on-state of the FET.[4,15] According to (eq 1) when QCF becomes maximum, so does T_D. In practice, this may translate into a higher I_{on} and higher I_{on}/I_{off} ratio, which are both figures of merit of paramount importance in high-performance TFETs.[7] In addition, it has been shown that in the QCL, drain-induced barrier thinning (DIBT) is significantly suppressed, which avoids undesirable effects, such as nonlinearity in the output characteristics and shifting of the threshold voltage.[4] Therefore, operation in the QCL is a critical feature to consider in the design and study of TFETs.

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In terms of channel structure, 1D nanowires (NWs) are highly relevant since they are more likely to reach the QCL.[3,4,6,15] In terms of material choice, silicon (Si) is an attractive option because its relatively large E_g allows to achieve a low I_{off} (hence improving I_{on}/I_{off}). Additionally, Si-based devices are compatible with state-of-the-art CMOS processes and are suitable for top-down approaches and sophisticated integration schemes.

This work presents experimental evidence of Si NWs exhibiting 1D behavior. This is the first time the impact of a 1D DOS is observed through CV measurements in a NW and also constitutes the first experimental demonstration of operation in the QCL in this type of system. In addition, results from simulations including the effect of relevant capacitances are shown. An excellent agreement is found between the theoretical calculations and the experimental data. The devices investigated in this study are gate-all-around (GAA) Si NW FETs. Figure 1a shows the schematic structure of the device with a cross-sectional TEM image of the NW.

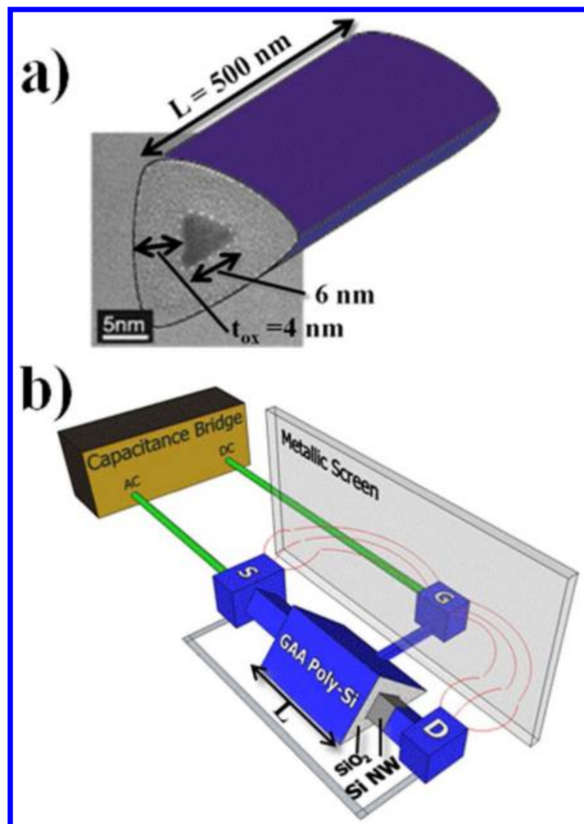

Figure 1. (a) Cross-sectional TEM image of the Si NW. (b) Schematic diagram of the experimental setup for CV measurements.

The length (L) of the Si NWs is 500 nm, and the silicon dioxide (SiO_2) thickness (t_{ox}) is 4 nm. Notice that the Si NW has a triangular shape and the length of each side is approximately 6 nm. The gate, source, and drain contacts are heavily doped (~10^{20} cm^{-3}) structures (crystalline Si for source and drain and poly-Si for the gate). The Si NW is intrinsic (unintentional doping of ~10^{15}cm^{-3}). The transport direction along the wire axis is (110). A complete and detailed description of the device fabrication process and device dimensions is provided in ref 20.

The transfer characteristics (I_d-V_G) as well as the CV measurements were both carried out at room- and low-temperatures (T = 293 and 77 K, respectively), in vacuum and isolated from electromagnetic radiation in a probe station.

I_d-V_G was obtained using a semiconductor parameter analyzer. The CV curves were measured using an ultraprecision capacitance bridge. Figure 1b shows a schematic representation of the experimental setup to measure CV curves of the Si NW FETs. The drain and source terminals are short circuited and act as a single terminal. The ac signal is applied to the source/drain terminal while the dc voltage is applied to V_G. A grounded metallic electrostatic screen was inserted between the drain/source and the gate terminals in order to screen the fringing electric fields between them. This technique was used in previous experimental work to reduce parasitic (fringe) capacitances.[21]

A clear correlation between I_d-V_G and CV measurements is always expected since both techniques capture information about how carriers are accommodated in the channel states as $V_G$varies. Figure 2 displays the full I_d-V_G and CV characteristics of a Si NW FET at room temperature to highlight this current and capacitance relationship. The band diagrams corresponding to each state of the device in Figure 2a are shown on top of the graph. From Figure 2a we conclude that for V_G > 2.5 V band-to-band tunneling (BTBT) from the valence band (VB) at the drain, into the conduction band (CB) in the channel, and from there into the VB at the source creates a current path.[1] BTBT is possible because the NWs are very thin, and this leads to a very small λ_{ch} as defined in eq 1,[3,6] which makes T_D high for large enough positive V_G values.

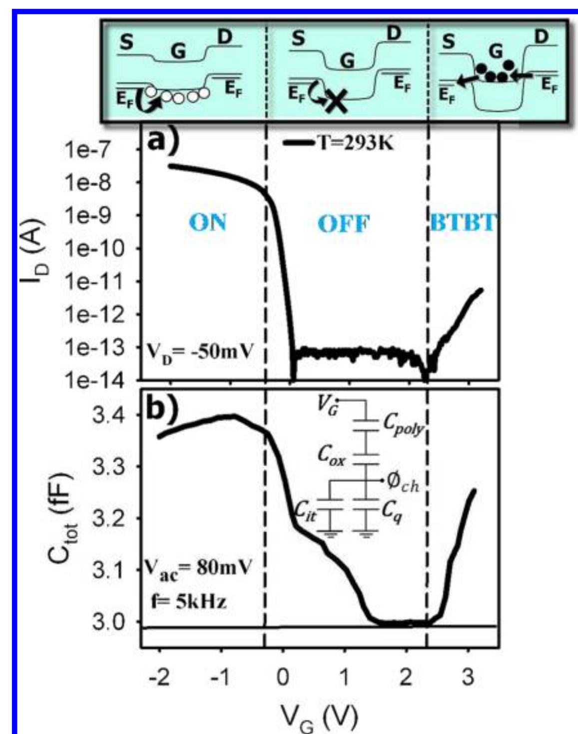

Figure 2. Experimental data obtained for a Si NW FET at T = 293 K. (a) I_d-V_G characteristic and (b) a CV curve for the same device. The inset displays the equivalent circuit with the relevant capacitances in the device.

For V_G < −0.1 V (on-state) thermionic emission of holes through the VB from source to drain occurs. For −0.1 V < V_G <

2.5 the device is in the off-state. In the following we will be focusing on the on-state ($V_G < -0.1$ V) and explore the impact of the VB 1D subbands on the device characteristics.

The measured C_{tot} in Figure 2b contains four components: C_{ox}, C_q, the interface traps capacitance (C_{it}), and the gate poly-Si capacitance (C_{poly}). The inset shows the equivalent circuit of these capacitances (the parasitic capacitances in parallel with the entire circuit are ignored for simplicity). Notice in Figure 2b that for $V_G < -1$ V the capacitance decreases as V_G becomes more negative. This trend is due to the impact of C_{poly} and is well established in conventional MOSFETs. For $V_G > 2.5$ V the capacitance increases because a larger V_G implies a higher T_D, and hence more electrons are populating the CB in the channel due to BTBT. For 0 V < V_G < 2.5 V the capacitance is mainly dominated by C_{it} due to carriers filling trap states available in the bandgap.

The next section highlights the most relevant findings of this study: (i) the direct observation of subbands in Si NWs and (ii) the evidence of Si NW FETs operating close to the QCL. Figure 3 shows I_d–V_G and CV curves at room and low temperatures for the same Si NW FET characterized in Figure 2. We claim that both the "hump" in the I_d–V_G as well as the "lobe" in the CV of Figure 3a,b at 77K are unambiguous evidence of mode quantization in our Si NWs.[22] While this work is the first to experimentally demonstrate both features in Si NWs, other studies have reported similar I_d–V_G characteristics for CNTs[23] and InAs NWs,[24] and in the case of CNTs the experimental signature of 1D subbands has been reported through CV measurements as well.[17,18]

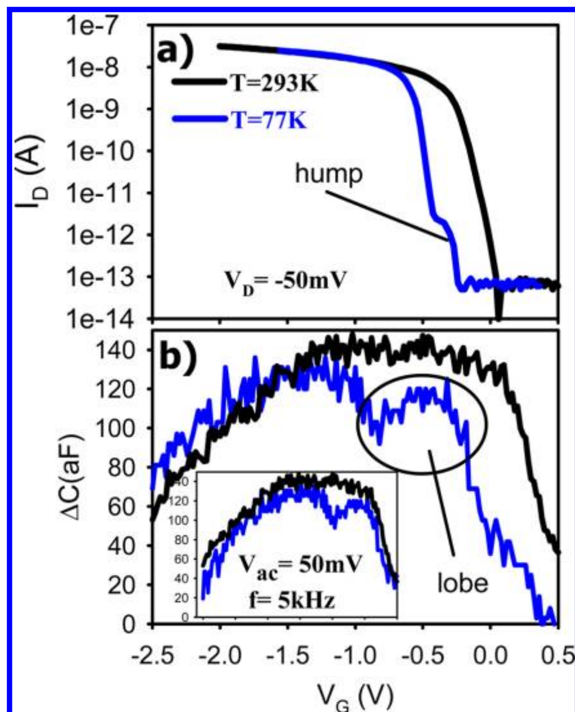

Figure 3. Experimental results for a Si NW FET at $T = 293$ and 77 K for the same device as shown in Figure 2. (a) Displays I_d–V_G characteristics and (b) shows the corresponding CV curves. The inset in (b) shows CV characteristics after shifting along the V_G axis to appreciate the difference between room- and low-temperature behavior.

The results presented in Figure 3 were found reproducibly in four different devices when CV measurements were taken. However, not all devices showing the 1D feature in the CV exhibited the corresponding 1D signature in the I_d–V_G. This finding makes us conclude that observing one-dimensional aspects in transport measurements can be suppressed due to various scattering effects, while the static CV measurement is the more robust way to experimentally study the density of states.

The implications of observing individual subbands in Si NWs through CV measurements are highly noteworthy: being able to observe the (convoluted) 1D DOS in the CV curve implies that C_q is the dominant component of C_{tot}. Therefore, the device is approaching the limit where $C_q \ll C_{ox}$ (i.e., is operating near the QCL). As mentioned above, operating in the QCL leads to higher I_{on} and larger I_{on}/I_{off} thus allowing to overcome one of the major limitations of TFETs. A convenient way to quantify the extent to which the device is within the QCL is by calculating the QCF (0 < QCF < 1). Results from our simulations (see the following discussion) indicate that QCF ≈ 0.25 in the on-state of the devices under investigation.

To understand the impact of individual capacitances on C_{tot} in detail, we have simulated CV curves using input parameters extracted from the characterization and geometry of the devices. A significant effort has been devoted to compute the capacitance of Si NWs using rigorous numerical simulations.[25−28] However, in this work a much simpler approach is proposed. The inset of Figure 2b shows the equivalent circuit of capacitors (C_{poly}, C_{ox}, C_q, and C_{it}) which has been used to calculate the total gate capacitance.

C_{poly} and C_{ox} were modeled assuming a cylindrical capacitor geometry—a reasonable approach for the GAA structure employed here.[7,21] Within this framework, $C_{poly} = (2\pi\varepsilon_{Si}L)/(\ln((d/2 + t_{ox} + W_{dep})/(d/2 + t_{ox})))$ and $C_{ox} = (2\pi\varepsilon_{ox}L)/(\ln((d/2 + t_{ox})/(d/2)))$, where d is the diameter of the Si NW (d = 6 nm), L is the length of the device (L = 500 nm), t_{ox} is the oxide thickness (t_{ox} = 4 nm), W_{dep} is the depletion width of the poly-Si gate, and ε_{ox} and ε_{Si} are the permittivity constants for SiO_2 and Si, respectively.

Eqs 2–5 show how the charge in the poly-Si gate (Q_{poly}), the change in channel potential ($\Delta\phi_{ch}$), the C_q, and the charge in the Si NW (Q_{Si}) were calculated.

$$Q_{poly} = qL\pi[(W_{dep} + d/2)^2 - (d/2)^2]N_{poly} \tag{2}$$

$$\Delta\varphi_{ch} = \Delta V_G \frac{(C_{ox}^{-1} + C_{poly}^{-1})^{-1}}{(C_{ox}^{-1} + C_{poly}^{-1})^{-1} + C_q} \tag{3}$$

$$C_q = \frac{\partial Q_{Si}}{\partial \varphi_{ch}} \tag{4}$$

$$Q_{Si} = qL \int_{-\infty}^{\infty} \frac{\mathrm{DOS}(E)dE}{1 + \exp\left(\frac{E - q(\varphi_{ch}^0 + \Delta\varphi_{ch})}{k_B T}\right)} \tag{5}$$

In (eq 2) N_{poly} is the doping of the poly-Si gate. In (eq 5) ϕ_{ch}^0 is the equilibrium channel potential, and "DOS(E)" is the 1D DOS calculated from the energy dispersion which was obtained using tight binding (TB). For the CB, the nearest-neighbor $sp^3d^5s^*$ TB method without spin–orbit (SO) coupling was employed. Well established and calibrated TB parameters for Si have been used.[29,30] For the VB, the nearest-neighbor sp^5s^* TB

method including SO coupling had been evaluated. The actual triangular-shaped geometry of the Si NW was used to carry out these TB calculations. The CV algorithm calculates $\Delta\phi_{ch}$ and W_{dep} self-consistently, while charge balance between Q_{poly} and Q_{Si} is maintained.

The effect of C_{it}[31,32] is not included in the simulations since our focus is on the device on-state where the impact of interface traps is small. Note that all quantities used in eqs 2–5 are effectively known, and no fitting is required to explain the experimental set of data.

However, in order to develop a sense of the sensitivity of the calculated CV on input parameters, Figure 4a illustrates the dependence on N_{poly}. The doping level of the poly-Si gate has a distinct impact on the lobes and the slope of the CV for negative gate voltages making it a good testing parameter for the validity of our simulation approach. Furthermore, in Figure 4a a number of observations are noteworthy:

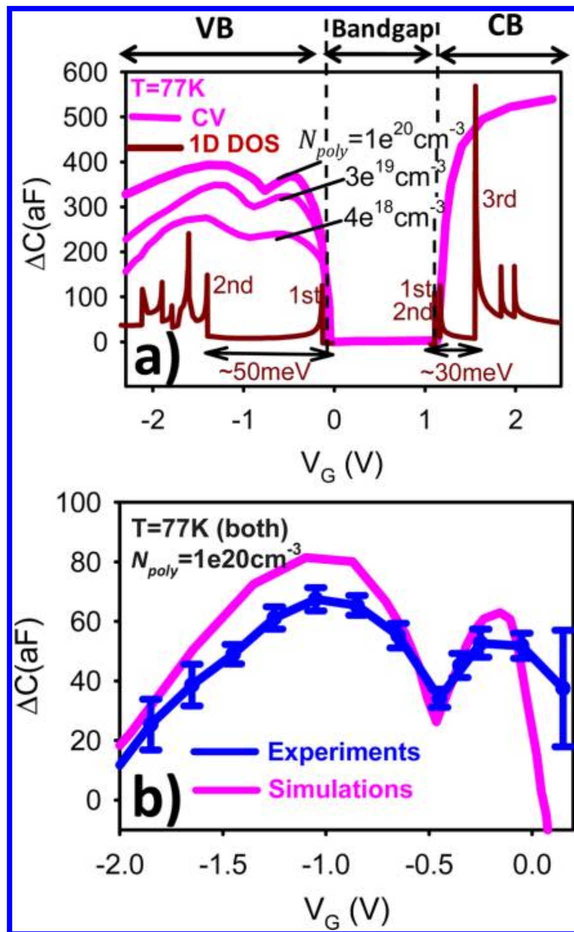

Figure 4. (a) Simulated CV for three different gate poly-Si doping levels (N_{poly}). The 1D DOS is included for illustration purposes to link with the relevant features in the CV curves. (b) Comparison between experimental (blue) and simulated (pink) CV curves.

(i) In the CB, the 1D DOS feature (lobe) is not visible due to the relatively small energetic spacing between the first and third subband (~30 meV) and also because C_q is large enough such that $C_q \gg C_{ox}$ (which makes $C_{tot} \approx C_{ox}$).

(ii) In the VB the lobe is visible due to a relatively large energetic spacing between the first and second subband (~45 meV) and also because C_q is small enough such that $C_q \ll C_{ox}$ (which makes $C_{tot} \approx C_q$). The fact that the 1D DOS feature is seen in the VB but not in the CB is consistent with our experiments. A total of 12 n-type Si NW FETs were tested at T = 77 K, and none of them showed 1D DOS features in the CB, neither in the I_d−V_G nor in the CV curves.

(iii) The lobes in the VB get broader as N_{poly} is decreased. This is because as N_{poly} decreases so does C_{poly}. According to (eq 3) a smaller C_{poly} implies a smaller $\Delta\phi_{ch}$, which translates into broader features (V_G becomes less effective at moving the bands). In the VB, as N_{poly} decreases so does the overall C_{tot} due to the series arrangement of capacitors (see inset Figure 2b). On the other hand, the lower N_{poly}, the easier the poly-Si is depleted with increasing magnitude of V_G, hence (dC_{tot}/dV_G) increases (for $V_G < -1.5$ V).

Before addressing the next subject, it is important to consider device-to-device variations. The threshold voltage (V_{th}) is the approximate value of V_G at which the first subband in the VB is populated. This information is captured by both the I_d−V_G and also the CV characteristic. Therefore, similar devices will exhibit similar CV curves, but those curves may be shifted along the V_G axis due to variations of the threshold voltage V_{th}. Moreover, our setup includes parasitic capacitances in parallel with the arrangement of capacitors shown in the inset of Figure 2b. These capacitances add a constant yet from device-to-device varying value to the measured total gate capacitance and thus produce a shift along the capacitance axis.

Therefore, variations in V_{th} and parasitic capacitances produce shifts along the V_G axis and the capacitance axis, respectively, when the total gate capacitance is measured, but they do not stretch or deform the CV curve at all. To account for this effect an offset was introduced to the simulations presented in Figure 4b in order to compare the relevant 1D features (i.e., the width and height of lobes). Figure 4b shows the final comparison of experimental and simulated CV curves at T = 77 K. The experimental curve is the averaged CV of four different devices. Notice that N_{poly} corresponds to the value of the actual device. It is obvious that there is an excellent agreement between the simulated and experimental CV curves in terms of the width and height of the lobes. Also notice that (dC_{tot}/dV_G) is very similar in the region where C_{poly} is dominant ($V_G < -1.5$ V). This shows that our analytical model successfully quantifies the impact of the 1D DOS on C_q and the effect of C_{poly}.

The QCF can be readily obtained from the simulated C_q and C_{ox}. It is found that QCF ≈ 0.25 in the on-state (average in the range $-0.5 < V_G < 0$ V). This is to the best of our knowledge the first time that operation in the quantum capacitance regime has been experimentally quantified. Preliminary estimates indicate that a minimum QCF ≈ 0.6 is needed in order to exploit the benefits of the QCL for TFETs in future device applications. Although theoretically, operation in the QCL increases I_{on} and I_{on}/I_{off} there are practical issues that may impact the effectiveness of this approach. This is the subject of the following discussion.

First, notice that QCF = 0.25 was obtained at low temperatures. At room temperature, QCF decreases due to thermal smearing and also because ΔE_{sub} (spacing between subbands) becomes smaller. Therefore, achieving QCF = 0.6 at room temperature seems unlikely in the case of Si. However, the important point to keep in mind is that the larger QCF, the

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better the performance of TFETs will be, even when QCF < 0.6 and regardless of the temperature of operation. Second, results from TB simulations (not shown) suggest that by applying tensile strain ΔE_{sub} in the CB may be increased without changing substantially E_g which would favorably impact QCF. This may also prove advantageous for the implementation of a complementary design since it allows both n- and p-TFETs to exhibit similar ΔE_{sub} and hence a similar QCF. Lastly, an alternative approach to increasing QCF occurs possible by using small E_g materials as an active channel. Such materials have intrinsically larger ΔE_{sub}, thus increasing QCF. In this case, I_{on} increases both because QCF is larger and E_g is smaller.

In summary, the impact of the 1D DOS in Si NW FETs has been experimentally observed, both through I_d-V_G and CV measurements. This is the first experimental demonstration of near-QCL operation of a Si-based device. In particular our findings imply that in practice approaching the QCL is in fact possible with state-of-the-art technology. On one hand, this may increase I_{on} and I_{on}/I_{off} ratio which would help to overcome one of the major limitations in TFETs. On the other hand, operating in the QCL suppresses DIBT which eliminates nonlinearity effects in the output characteristics and avoids ultimately shifts of the threshold voltage. An analytical model to calculate the total gate capacitance has been proposed which is able to quantitatively capture the impact of the 1D DOS on C_q and the effect of the gate poly-Si depletion as evident from comparison with experimental data.

AUTHOR INFORMATION

Corresponding Author

*E-mail: ramon@purdue.edu

Notes

The authors declare no competing financial interest.

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