THE EFFECTS OF POWER FACTOR CORRECTION AND POWER BUFFER OPERATION ON THE UTILITY DISTRIBUTION SYSTEM

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CEME-TR-01-4
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1. INTRODUCTION

Recent years have seen a pronounced increase in the number of electronic devices powered by the utility system. From electronic motor drives and industrial controllers to personal computers, these devices provide a tremendous benefit to both industry and consumers alike. However, they also place additional requirements on the utility system.

Linear electric loads such as incandescent lighting and uncontrolled synchronous or induction motors will draw current from the utility at the same frequency as the voltage. While inductive loads create a phase shift and decrease the displacement power factor, the current drawn is relatively sinusoidal. For sinusoidal load currents, the utility can correct the power factor by placing capacitance on the system to balance the inductive load. While adding capacitor banks onto the distribution system raises its own issues for utilities, the effects are well understood, and this practice has been used for years.

Electronic loads, on the other hand, usually do not operate at line frequency, and require a power converter. The conversion process creates a nonlinear load that can add considerable harmonics to the load current, reducing the power factor. However, because the low power factor is not due simply to an out-of-phase sinusoid, it cannot be corrected simply by adding capacitance.

For a purely linear system, low power factor is mainly a concern for the utility. Because larger currents are required to supply a given load, additional stress is placed on equipment, and there are greater resistive losses in the distribution system. To compensate for this, industrial customers must pay a premium to draw power at a low power factor.

With nonlinear loads on the system, new issues arise. Not only will the low power factor increase line losses and energy costs, but the current harmonics coupled with the line impedance

can create harmonics on the system voltage, creating a concern for customers as well as the utility.

The term *power quality* as used in the industry today is synonymous with voltage quality [1]. The quality of the system voltage is becoming increasingly important as the number of nonlinear loads increases, because these systems tend to be sensitive to voltage distortions [2], [3]. Sags, swells, interruptions, and excessive harmonics can disrupt the operation of this type of equipment. This can be costly to certain industrial users, or just plain annoying to the rest of us. An entire industry has been created to address power quality issues for power users, and several organizations have created standards to control the harmonics on the distribution system. These standards place limits on both the utility and power users, and are beginning to force manufacturers to limit the current harmonics placed on the system.

Fortunately, with the advancement of power electronic devices, it is becoming practical to implement power factor correction (PFC) when rectifying ac power. When properly implemented, PFC rectifiers can present a nearly sinusoidal current to the utility that under steady-state conditions will appear as a linear load to the source. However, in reality, PFC rectifiers operate as constant power loads and can create stability issues under transient conditions. This thesis investigates the effects that power factor correction and power buffering have on the utility distribution system and on power users.

Chapter 2 begins by introducing the operation of PFC rectifiers and the advantages they have over basic rectification methods. The PFC rectifier is then incorporated into a power buffer system that allows an ac load to be decoupled dynamically from the utility system. Chapter 3 investigates the stability issues created by the interaction of constant power loads with the distribution system. Chapter 4 relates how a PFC rectifier operates as a constant power load.

The operation of the power buffer is described in Chapter 5, with emphasis on its ability to protect sensitive loads from disruptions on the distribution system. Chapter 6 continues with the description of the power buffer, focusing on its ability to adjust the displacement power factor of the distribution system to compensate for other loads on the system.

2. POWER FACTOR CORRECTION

The utility line frequency of 50 or 60 Hz is a convenient supply for many loads. Incandescent lighting works well plugged directly into the wall. Induction motors operating near multiples of the line frequency have been used for years in factory machinery. Even fluorescent lights will operate off of 60 Hz. However, although 60 Hz power is acceptable for many tasks, in general, it is not ideal, and in many cases is not usable at all. Fluorescent lighting, for example, while operating satisfactorily at 60 Hz, is more efficient at higher frequencies [4]. Induction motor machine tools can perform many tasks; however, they become much more useful if their speed can be controlled. This requires varying the voltage and frequency at the motor inputs. Even more pronounced examples are computers and electronic appliances, which are rapidly becoming ubiquitous. Almost all of these devices need dc power to operate, making ac to dc conversion a required front end for many power supplies. Even devices that output ac power, such as ac motor drives, usually rectify line frequency onto a dc bus before recreating ac through an inverter.

2.1. Rectification and Harmonic Distortion

Ac to dc rectification can be a major cause of harmonics on the utility system. All methods of rectification require some form of switching, making the process inherently nonlinear. To illustrate, consider the simple single-phase classical rectifier shown in Figure 2.1.

The rectifier consists of a diode bridge followed by a filter capacitor, and is extremely common in low-power supplies. Because the diodes only conduct when the source voltage magnitude exceeds the filter capacitor voltage, source current is drawn only in short spikes near the voltage peaks as shown in Figure 2.2.

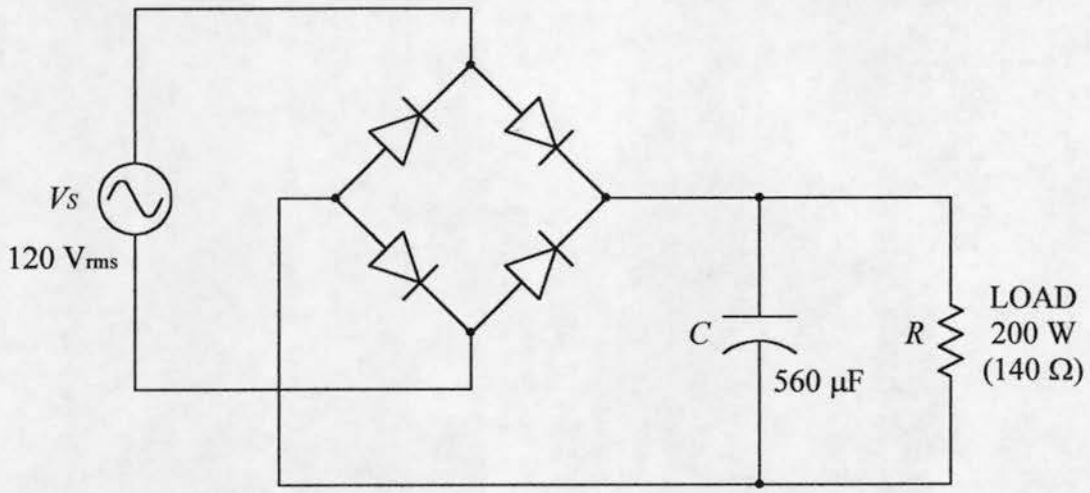

Figure 2.1: Circuit diagram of the classical rectifier.

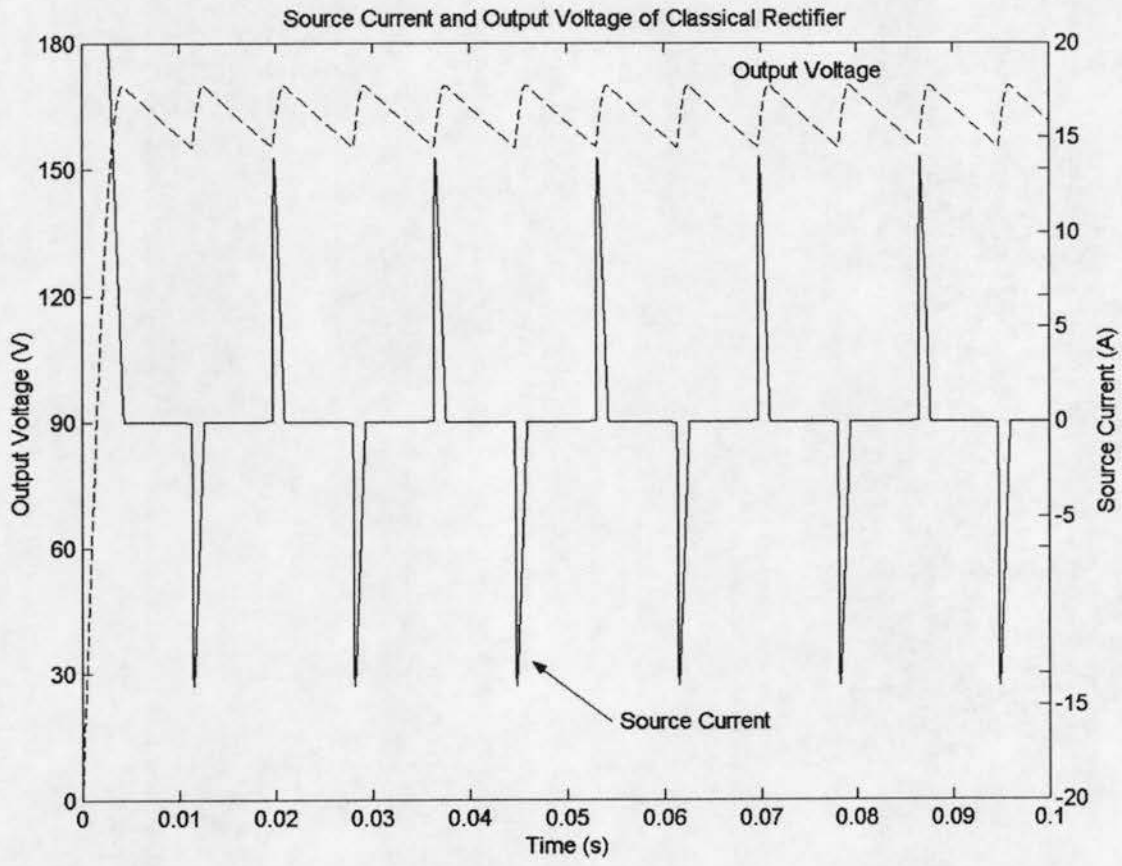

Figure 2.2: Voltage and current of classical rectifier example.

The system simulated is a 200-W, single-phase supply powered from a standard 120-V, 60-Hz source. These ratings are typical for a computer power supply in the United States. The source current has a considerable harmonic content that, in turn, leads to a low power factor [5]. In this example, the 3rd, 5th, 7th, and 9th harmonic amplitudes are 94%, 82%, 68%, and 52%, respectively, of the fundamental, keeping the power factor under 0.5. Because this type of rectifier is generally used in low-power equipment, the effects of a single device on the utility system will be minimal. However, with the rapid proliferation of computers and other electronic devices, the cumulative effects can place a heavy burden on the utility system if all of these devices generate large harmonics. To illustrate the effect that large, nonlinear loads can have on the utility system, consider the one-line system diagram in Figure 2.3.

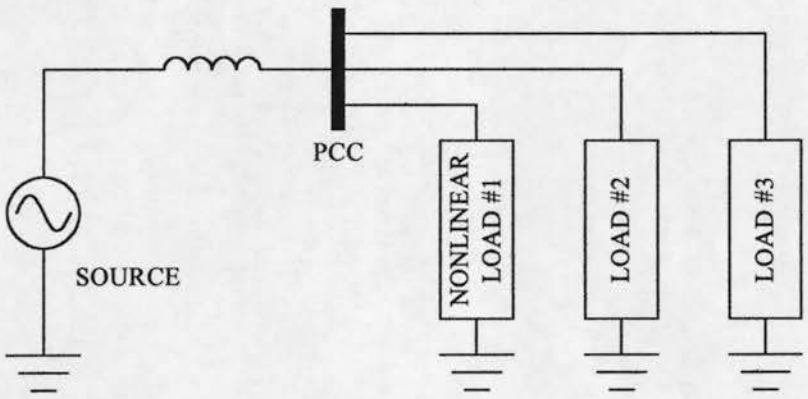

Figure 2.3: Circuit diagram of system for PCC example.

Here, the nonlinear load is part of a distribution system serving additional loads. As in all real distribution systems, there is impedance between the utility and the loads. The point where all of the load currents connect to the source is called the point of common coupling (PCC). Any voltage distortion generated at this point of the system will be seen by any load, not just the load that originated it. Now consider the nonlinear load described above. The generated current harmonics will have to be fed through the source impedance. If this impedance is significant, these harmonics will generate a voltage drop across the source impedance that will be seen by all

of the loads on the same feeder. Figure 2.4 shows an example of the voltage resulting at the PCC from a large, nonlinear load at the end of a long feeder. Notice that the peak of the voltage waveform is now clipped, introducing harmonics. These voltage harmonics are present for any load on the same feeder.

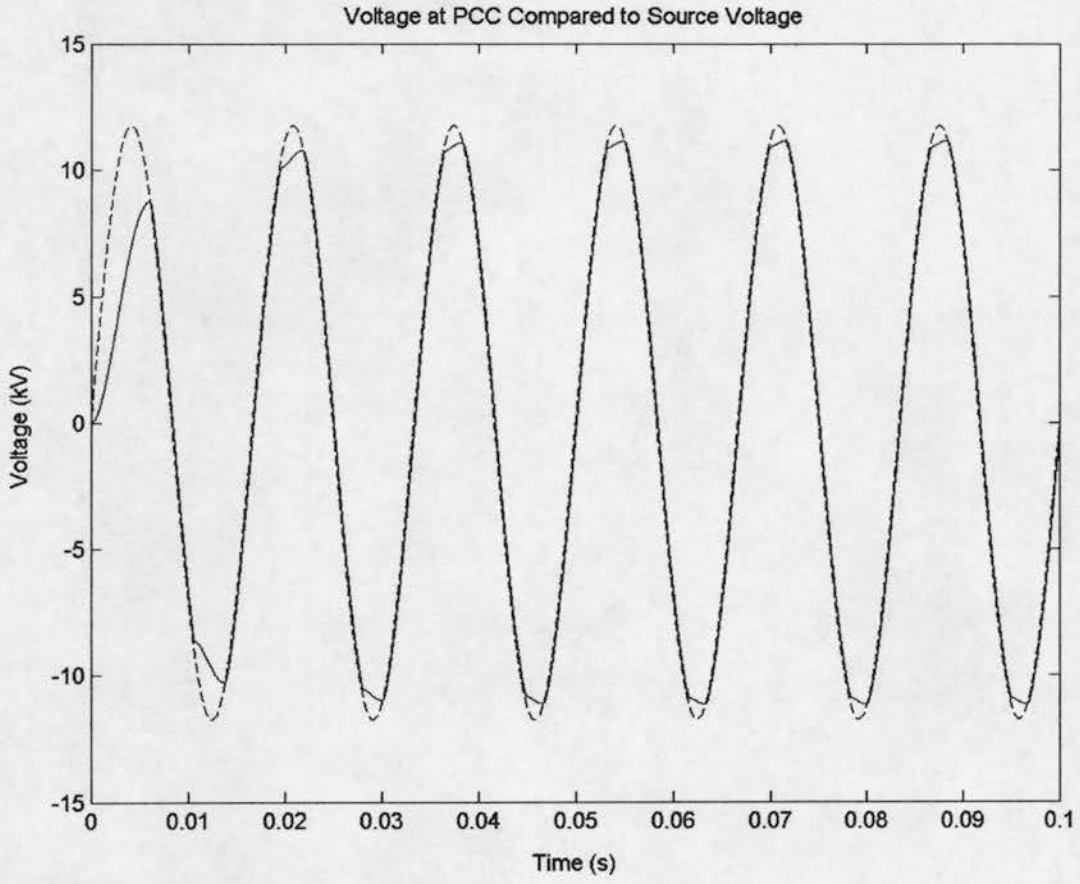

Figure 2.4: Voltage distortion at the PCC.

2.2. Power Factor Correction

The increasing number of harmonics being generated on the utility system along with the increasing sensitivity of many loads to voltage disturbances has increased interest in power quality. Customers require the electric utility to provide clean, sinusoidal voltage at a constant frequency. In turn, to be able to provide this, utilities require customers to limit the harmonics they generate. In an effort to set guidelines to allow this to happen, several standards

organizations including IEEE, CENELEC, IEC, and VDE have created standards limiting the harmonic content allowed on the utility system. IEEE 519, for example, is an industry-recognized standard that places limits on the voltage harmonics allowed by the utility, as well as the current harmonics generated by the user [4]. The voltage harmonic limits depend on the system voltage. For distribution system voltage from 2.3 kV up to 69 kV, the maximum allowed value for any individual harmonic is 3.0% of the fundamental, with the total harmonic distortion limited to 5.0%. To allow the utility to accomplish this, power users must keep current harmonics below the standard limits. The limits depend on the source impedance, but are as low as 4.0% for low-order harmonics generated by users at the end of a long feeder where the available fault current is less than 20 times the normal load current.

To comply with these harmonic limits, manufacturers are turning to power factor correction. With the advances in power electronics, it is now becoming practical to correct for low power factor by controlled switching of the input current, drastically reducing the size and cost of passive filters, and in many cases, providing a level of correction otherwise unobtainable.

In a perfect world, each device placed on the utility system would draw a perfectly sinusoidal current with a unity power factor. With a properly designed power factor corrected interface at the front end of every power supply, it is possible to approximate this. However, cost and design concerns do not always make this approach practical. For nonlinear loads that do not lend themselves well to direct power factor correction, another method to reduce utility harmonics is by using a buffer. By placing a buffer between noisy loads and the utility system, unwanted harmonics can be kept from passing in either direction. The following sections describe both methods, and demonstrate their effects on both sensitive loads and on the utility system.

While several switching topologies and control methods exist to provide power factor correction, a common and practical method is to operate a two-level PWM inverter in reverse, creating a power-factor corrected rectifier. This method has several advantages: it operates naturally as a boost converter, current flow can be bidirectional allowing power to be fed back into the utility system, and it is fairly straightforward to implement for either single- or three-phase systems. Single-phase rectifiers are common as a front end for lower power devices such as personal computers, while three-phase rectifiers are usually used for higher power applications such as motor drives and utility buffers.

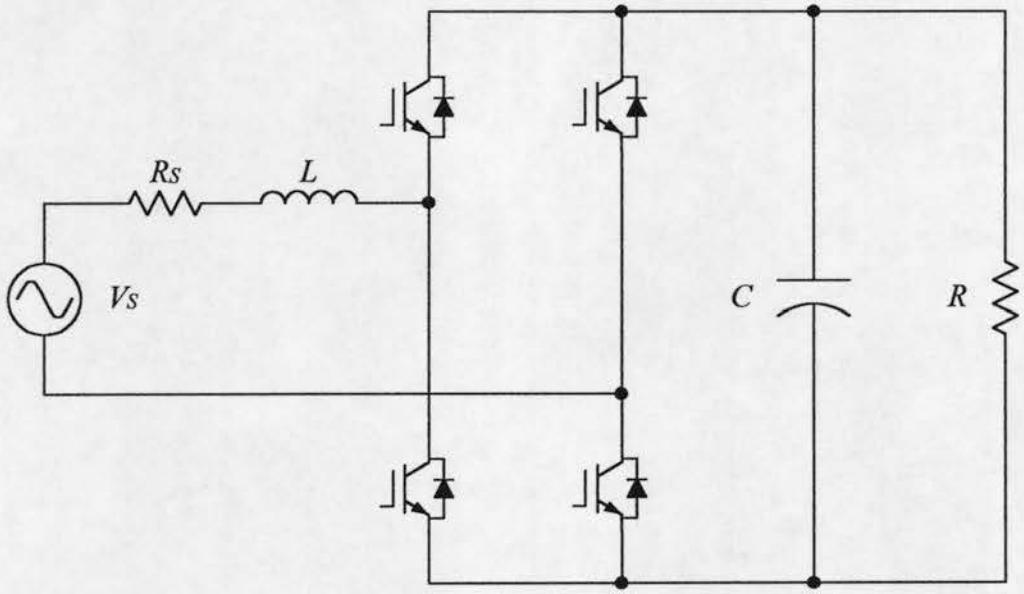

Figure 2.5: Circuit diagram of single-phase PFC rectifier.

To illustrate the advantages of power factor correction, consider the single-phase rectifier shown in Figure 2.5. It consists of two sets of totem-pole switches connecting the input filter inductor to the dc storage capacitor. For off-line power supplies, these switches are generally power MOSFETs or IGBTs [6]. This configuration is a good replacement for the classical rectifier of Figure 2.1 for single-phase power devices. Consider the same 200-W load simulated

earlier for the classical rectifier. The input voltage and current waveforms using the single-phase PFC rectifier are shown in Figure 2.6.

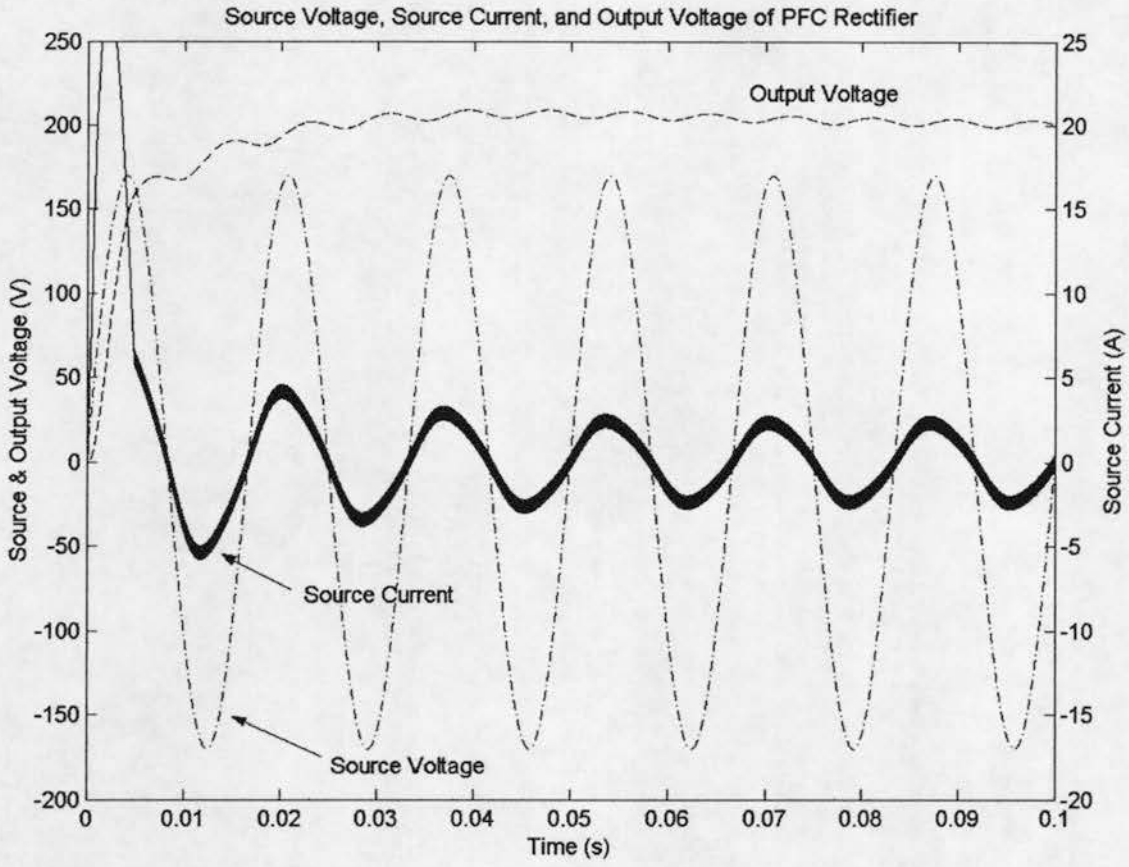

Figure 2.6: Voltages and current of single-phase PFC rectifier.

Note that the fundamental current is sinusoidal and in phase with the input voltage. Harmonics of the 60-Hz fundamental are low, with the majority of the harmonic content being associated with the switching frequency. The harmonic content is considerably less than for the classical rectifier and is easier to filter, if necessary, due to the higher frequency.

2.3. The Power Buffer

Power factor corrected devices go a long way in reducing the harmonics placed onto the utility system, but many uncompensated, nonlinear loads still exist. One straightforward method of keeping the power-frequency harmonics associated with these loads off of the utility system is

to place a buffer between all nonlinear loads and the utility [7], [8]. This can be accomplished by combining a PFC rectifier followed by dc energy storage, followed by an inverter to supply the ac load. For larger loads, a three-phase system is preferred. Such a system is shown in Figure 2.7.

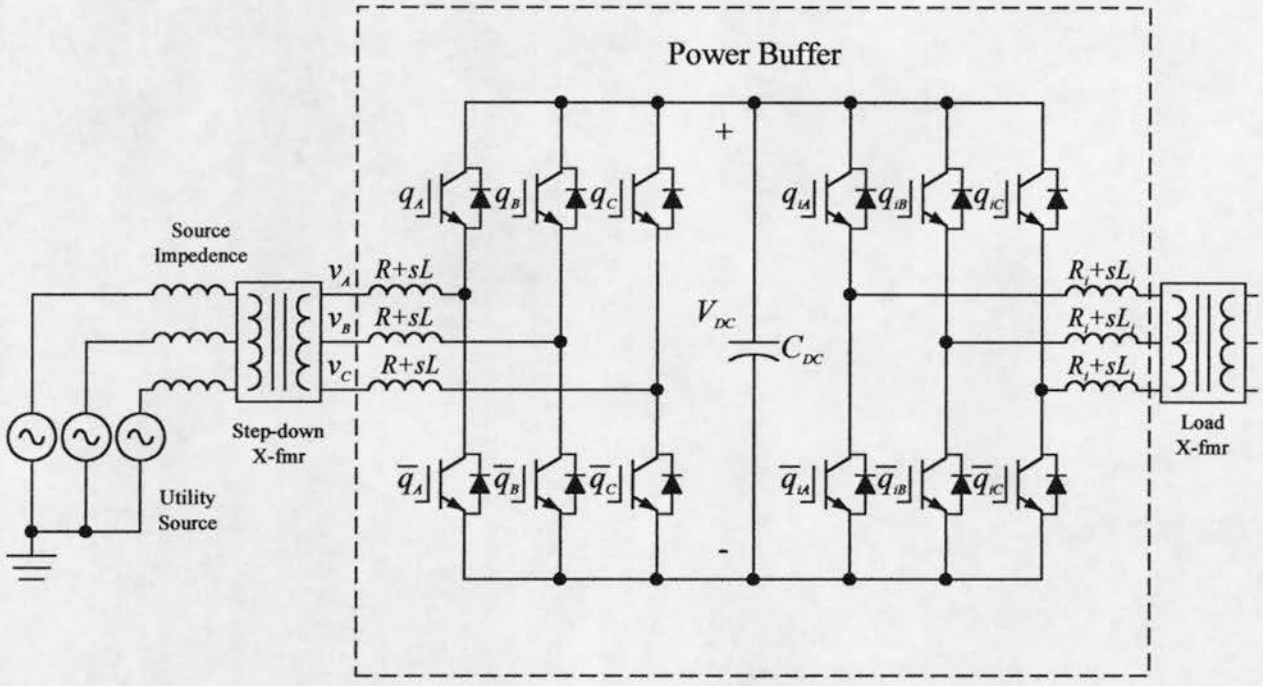

Figure 2.7: Circuit diagram of power buffer.

To protect a high-power load or an entire facility, a convenient location for such a buffer is on the incoming 480-V, three-phase bus. This voltage allows standard switchgear to be used and fits well with the present state-of-the-art of power electronics. At higher power levels, IGBTs are the preferred switching device for this type of application, and at present, 1200-V, 1200-A devices are commonly available from multiple manufacturers [9], [10]. With a 480-V source, a single switching device can be used while still providing adequate margin for transients, avoiding the complication of placing devices in series. Using 1200-A switches fed by a three-phase, 480-V source, a single buffer can control an excess of 500 kW, enough power to supply a moderately sized facility.

As can be seen in Figure 2.7, the PFC rectifier and the inverter share the same topology. The only differences are that the layout is reversed, and that they use different control schemes. The rectifier operates as a three-phase, PFC boost converter, while the inverter operates as a buck dc to ac converter. In a three-phase system, for the rectifier to operate, the dc storage capacitance does not need to be particularly large because it mainly carries the high-frequency switching current. However, as will be evident later, increasing the capacitance can improve the power quality to the load and may be required to keep the system stable under transient conditions.

The characteristic equations governing the operation of the system are described below. Because the PFC rectifier and the inverter share the same topology and because the utility interface is of special concern, emphasis will be placed on the rectifier operation. The characteristic equations for the inverter are identical, with the exception that the current polarities are reversed to have positive current flow from source to load. To provide for a balanced system as well as to simplify the analysis, the input impedance of the individual phases of the rectifier are matched, as are the output impedances of the inverter.

As shown in Figure 2.7, the PFC rectifier consists of six switches that connect the input impedance of each phase to the positive and negative terminals of the dc storage capacitor. The six switches give a possible 2^6 or 64 switching combinations. However, Kirchoff's laws require that exactly one switch be closed per phase. This drastically reduces the number of allowed switching combinations from 64 down to 8. To describe the switch status, the variables q_A, q_B, and q_C represent the position of the two switches connected to phases A, B, and C, respectively. A value of one indicates that the upper switch is closed, and a value of zero indicates that the

lower switch is closed. The characteristic equations of the balanced rectifier for each of the eight switch configurations are as follows:

q_A=0, q_B=0, q_C=0:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C - 3Ri_A) \tag{2.1}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C - 3Ri_B) \tag{2.2}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C - 3Ri_C) \tag{2.3}$$

q_A=0, q_B=0, q_C=1:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C + v_{DC} - 3Ri_A) \tag{2.4}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C + v_{DC} - 3Ri_B) \tag{2.5}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C - 2v_{DC} - 3Ri_C) \tag{2.6}$$

q_A=0, q_B=1, q_C=0:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C + v_{DC} - 3Ri_A) \tag{2.7}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C - 2v_{DC} - 3Ri_B) \tag{2.8}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C + v_{DC} - 3Ri_C) \tag{2.9}$$

q_A=0, q_B=1, q_C=1:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C + 2v_{DC} - 3Ri_A) \tag{2.10}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C - v_{DC} - 3Ri_B) \tag{2.11}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C - v_{DC} - 3Ri_C) \tag{2.12}$$

q_A=1, q_B=0, q_C=0:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C - 2v_{DC} - 3Ri_A) \tag{2.13}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C + v_{DC} - 3Ri_B) \tag{2.14}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C + v_{DC} - 3Ri_C) \tag{2.15}$$

q_A=1, q_B=0, q_C=1:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C - v_{DC} - 3Ri_A) \tag{2.16}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C + 2v_{DC} - 3Ri_B) \tag{2.17}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C - v_{DC} - 3Ri_C) \tag{2.18}$$

q_A=1, q_B=1, q_C=0:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C - v_{DC} - 3Ri_A) \tag{2.19}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C - v_{DC} - 3Ri_B) \tag{2.20}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C + 2v_{DC} - 3Ri_C) \tag{2.21}$$

q_A=1, q_B=1, q_C=1:

$$\frac{di_A}{dt} = \frac{1}{3L}(2v_A - v_B - v_C - 3Ri_A) \tag{2.22}$$

$$\frac{di_B}{dt} = \frac{1}{3L}(-v_A + 2v_B - v_C - 3Ri_B) \tag{2.23}$$

$$\frac{di_C}{dt} = \frac{1}{3L}(-v_A - v_B + 2v_C - 3Ri_C) \tag{2.24}$$

Here, v_A, v_B, and v_C are the source voltages, i_A, i_B, and i_C are the source currents, v_{DC} is the dc bus voltage, and L and R are the source inductance and resistance values for each phase. Note that because only the three-phase connections are used without a separate neutral wire, only two

of the three state equations for the phase currents are needed because $i_A + i_B + i_C = 0$. If the A and B phase currents are chosen as independent, the C phase current can be found from

$$i_C = -(i_A + i_B) \tag{2.25}$$

The characteristic equation for the capacitor voltage is simply

$$\frac{dv_{DC}}{dt} = \frac{1}{C}(i_{CIN} - i_{LOAD}) \tag{2.26}$$

where i_{CIN} is the current into the capacitor from the rectifier and i_{LOAD} is the current out of the capacitor into the inverter. These currents are positive for power flow from the source to the load, but can be negative if power is flowing in reverse. The value of i_{CIN} depends on the position of the switches and is defined in Table 2.1.

Table 2.1: Capacitor input current versus switch status of the PFC rectifier.

Switch Positions			
q_A	q_B	q_C	i_{CIN}
0	0	0	0
0	0	1	i_C
0	1	0	i_B
0	1	1	$-i_A$
1	0	0	i_A
1	0	1	$-i_B$
1	1	0	$-i_C$
1	1	1	0

These equations completely define the PFC rectifier system. As stated earlier, the inverter shares these same characteristic equations with the current polarities reversed. All that remains to be determined is the control of the switching action. The rectifier control is required to accomplish the following:

- Control the individual phase currents such that they are sinusoidal and in phase with the source voltage.
- Keep the dc bus voltage on the energy storage capacitor within a given range of the desired bus voltage.

Because the primary objective of the rectifier is to force the input currents to match the source voltage waveforms, a current-controlled switching scheme makes the control straightforward. This type of control can be divided into two parts. The first generates a reference current value for each of the three phases that will supply the correct amount of power to the capacitor to keep the dc bus voltage constant. The second part controls the switch action to match the input current waveforms to the source voltages.

To keep the system balanced under steady-state operation, it is desirable to keep the magnitude of the input currents of each phase identical. This is accomplished by generating a single reference current value, i_{REF}, and using it as the magnitude for all three phase currents. The actual reference current for each of the three phases then consists of i_{REF} multiplied by the desired unity-peak waveform. Because the system is trying to make the input impedance of the buffer appear resistive, the ideal reference waveform is the normalized source voltage for each phase. Matching the current and voltage waveforms keeps the input impedance of the buffer resistive during transients, aiding in the stability of the distribution system. The three reference currents then become

$$i_{AREF} = \frac{i_{REF}}{V_{NOM}} v_A \tag{2.27}$$

$$i_{BREF} = \frac{i_{REF}}{V_{NOM}} v_B \tag{2.28}$$

$$i_{CREF} = \frac{i_{REF}}{V_{NOM}} v_C \tag{2.29}$$

Here, V_{NOM} is constant and equal to the nominal peak source voltage. As long as i_{REF} is relatively constant over a cycle, the input voltage and current will have similar waveforms and the power factor will be high.

The value of i_{REF} must be controlled to keep the dc bus voltage constant. This can be accomplished by using a standard PI controller with the difference between the bus voltage and the reference voltage as its input. The equation for i_{REF} is then

$$i_{REF} = k_p(V_{REF} - v_{DC}) + k_i \int (V_{REF} - v_{DC})dt \tag{2.30}$$

where k_p, k_i, and V_{REF} are constants; k_p is the gain for proportional control; k_i is the gain for integral control; and V_{REF} is the desired voltage of the dc bus. Because the rectifier topology is a boost converter, for the control to operate properly, V_{REF} must be greater than the peak value of the source voltage V_{NOM}.

Once armed with the reference currents in Equations (2.27), (2.28), and (2.29), there are a variety of ways to implement the switch action, encompassing both pulse-width modulation (PWM) and geometric control methods [11]. In all cases, switching the input inductor to the negative dc bus increases the input current, and connecting it to the positive dc bus decreases the input current. Each method has its own characteristics. However, as long as the switching frequency is significantly larger than the source frequency, the average duty cycle of the switches will be similar for any of the methods. The following examples use a simple hysteresis control, and other control methods are not explored.

The hysteresis control used here consists simply of assigning a tolerance band around the reference current for each phase, and comparing the actual input currents to the appropriate reference bands. If the actual current is above the upper tolerance limit, the input inductor of that phase is switched to the positive dc bus. Likewise, if the current is below the lower tolerance limit, the input inductor is switched to the negative dc bus. If the current is within the tolerance band, the switch position does not change.

To illustrate the ability of the power buffer to decouple the load from the utility, the buffer described in Figure 2.7 can be used to drive a 50-Hz load from the 60-Hz utility source. Here, the buffer is placed between the utility and the load, and the output inverter is driven at 50 Hz. The buffer is driving a 115-kW, three-phase load. Figure 2.8 shows the results. The source voltage and current are shown in Figures 2.8(a) and (b). They are in-phase, with a power factor very near unity. The 50-Hz output voltage is shown in Figure 2.8(c).

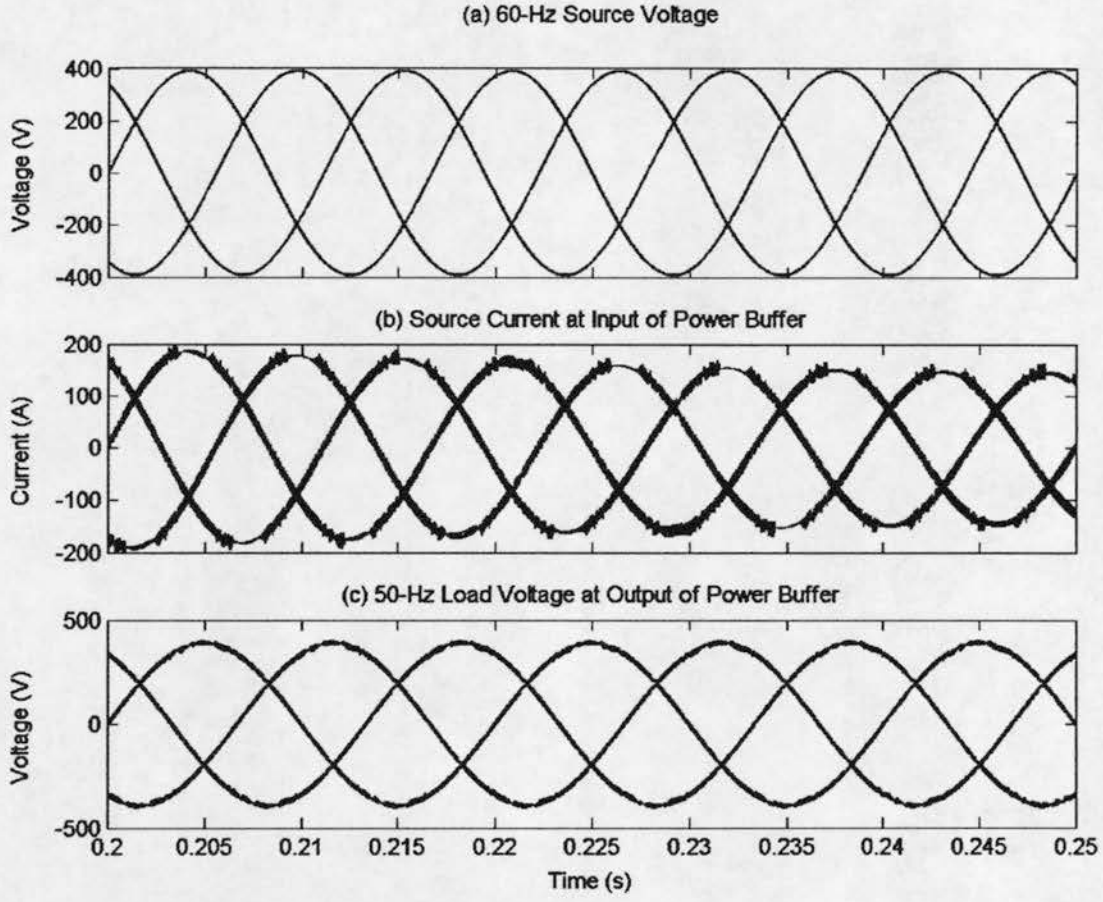

Figure 2.8: Voltages and current for power buffer driving load at 50 Hz.

3. NEGATIVE IMPEDANCE AND CONSTANT POWER LOADS

One concern with using a power factor corrected system is that it can increase the likelihood of system instability under transient conditions. This is due to the input impedance that a PFC controlled load presents to the distribution system [12]. A PFC system is usually controlled to match the load current to the waveform of the source voltage, thereby providing unity power factor. Under steady-state conditions, for a sinusoidal source voltage, the PFC control keeps the load current sinusoidal and in-phase, making the load appear purely resistive. The displacement power factor is corrected to almost unity, and the harmonics associated with highly distorted load currents can be reduced significantly.

3.1. Constant Power Loads

However, despite appearing resistive during the steady state, under transient conditions, the impedance of a PFC rectifier is actually that of a constant power load. This is caused by the rectifier control attempting to maintain a constant dc voltage at its output. If the voltage on the dc bus does not vary, the load will always see a nice, constant voltage, and its power draw will remain constant. Therefore, if the dynamic response of the PFC system is fast enough to maintain a constant dc output voltage, the power drawn from the utility will remain constant, making the system appear as a constant power load. Therefore, if the source voltage drops suddenly, to maintain constant power, the current draw will increase, and vice versa. The input impedance of the system, therefore, is negative under transient conditions, and it is this negative impedance that can lead to instability.

To understand the negative impedance characteristics of a constant power system, it is important to realize that it is inherently nonlinear. As such, the input impedance of the system is defined by

$$Z_{IN} = \frac{dv_{IN}}{di_{IN}} \tag{3.1}$$

Because, in a constant power system

$$v_{IN} = \frac{P}{i_{IN}} \tag{3.2}$$

the input impedance becomes

$$Z_{IN} = \frac{dv_{IN}}{di_{IN}} = \frac{d}{di_{IN}}\left(\frac{P}{i_{IN}}\right) = -\frac{P}{i_{IN}^2} = -\frac{V_{IN}I_{IN}}{I_{IN}^2}\bigg|_{\substack{v_{IN}=V_{IN} \\ i_{IN}=I_{IN}}} = \frac{V_{IN}}{I_{IN}}\bigg|_{\substack{v_{IN}=V_{IN} \\ i_{IN}=I_{IN}}} \tag{3.3}$$

where V_{IN} and I_{IN} are the voltage and current at the operating point.

Given this relationship, the input impedance of a constant power system will be negative at any given operating point, despite the fact that while the load is consuming power, both the voltage and current have the same sign. This characteristic is illustrated in Figure 3.1.

Because of the inherent negative impedance of a constant power system, stability issues arise that do not occur for a passive, linear system. This is a result of the interaction of the load with the source impedance [13], [14], [15]. Any real distribution system has source impedance and is generally some linear combination of resistance, inductance, and capacitance. As will be shown, if a linear distribution system is coupled to a load with negative impedance, the resulting system can be unstable. This is easily demonstrated with some simple examples.

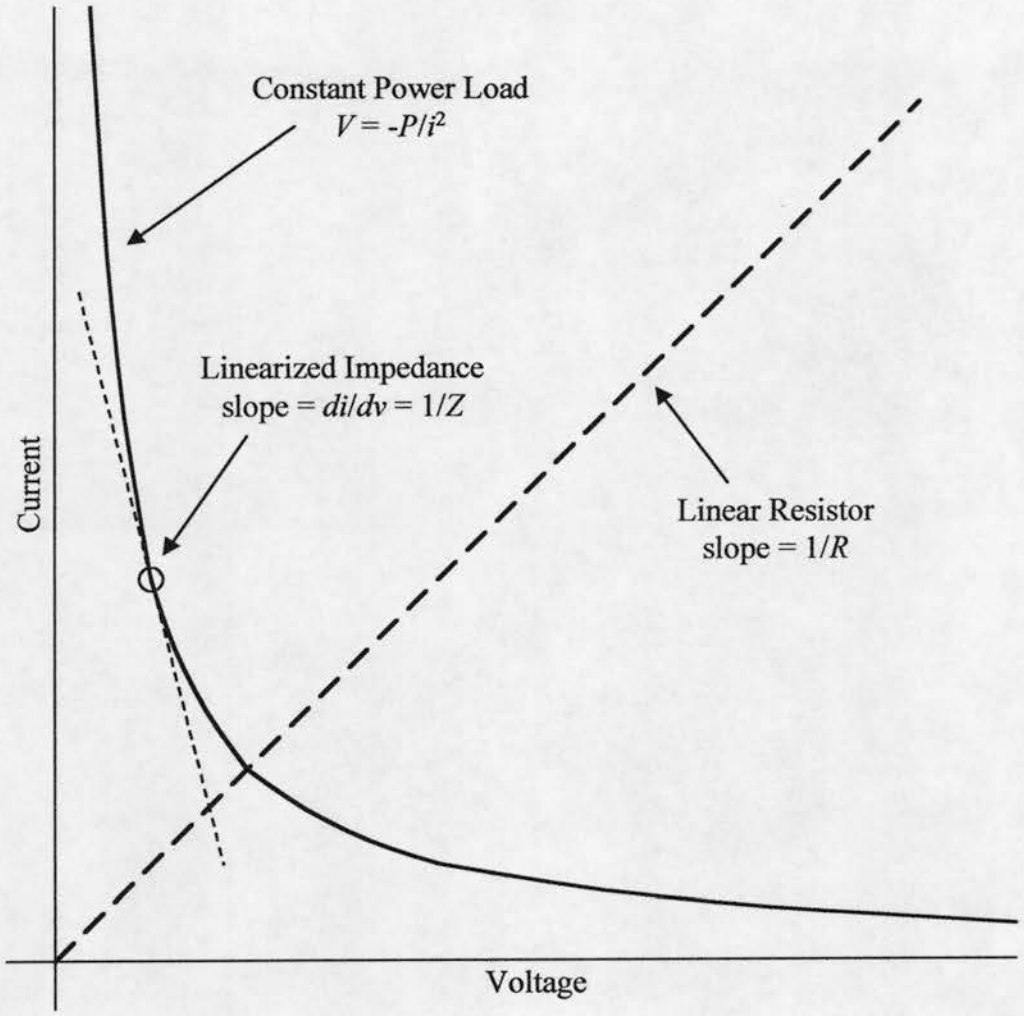

Figure 3.1: Voltage–current graph of constant power load.

3.2. Distribution Systems with RL Impedance Characteristics

Consider the simple case where the source impedance consists only of series resistance and inductance. The load impedance is purely resistive, but can be either positive or negative. In this system which is shown in Figure 3.2, the source impedance is the series combination of R_S and L, and the load is simply the resistance R, where R can be positive or negative. The transfer function V_{OUT}/V_{IN} for the system is

$$\frac{V_{OUT}}{V_{IN}} = \frac{R/L}{s + \dfrac{R+R_S}{L}} \tag{3.4}$$

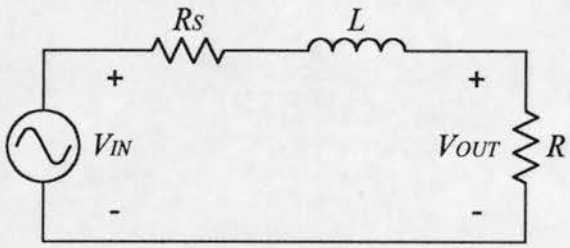

Figure 3.2: Circuit diagram for system with RL source impedance.

For a stable system, all poles of the system must be in the left half-plane of complex space, requiring that all poles are less than zero [16]. This system has only one pole and it occurs at

$$s = -\frac{R + R_S}{L} \tag{3.5}$$

This pole will be negative if

$$R > -R_S \tag{3.6}$$

If R is positive, this condition is always satisfied and the system is stable. However, if R becomes negative, the system is unstable if the magnitude of the load resistance is greater than that of the source resistance. This implies that a system with a negative impedance load can become unstable if it is lightly loaded. Note that this is the opposite behavior of a system with positive load resistance. In that case, it is desirable to minimize the source resistance to avoid wasting energy in the distribution system. Additionally, as the load resistance becomes larger, the system pole moves farther to the left, speeding up the transients.

3.3. Distribution Systems with RLC Impedance Characteristics

A more complete representation of a distribution system includes some shunt capacitance in addition to the series resistance and inductance [17]. The capacitance adds a second pole to the system and additional stability requirements. A system that includes the source capacitance is shown in Figure 3.3, where the shunt capacitance C has been added to the series resistance R_S

and the series inductance L. The load is still represented by the resistance R and can be positive or negative. The transfer function for this system is

$$\frac{V_{OUT}}{V_{IN}} = \frac{1/LC}{s^2 + \left(\frac{R_S}{L} + \frac{1}{CR}\right)s + \frac{(R+R_S)}{LCR}} \tag{3.7}$$

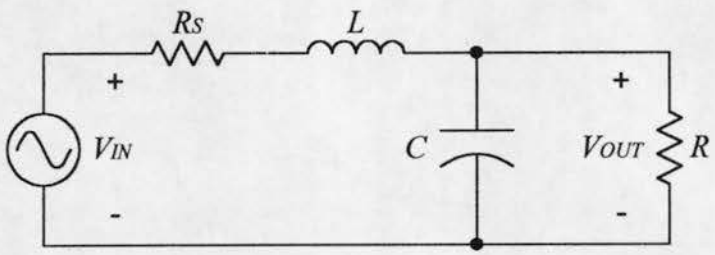

Figure 3.3: Circuit diagram for system with RLC source impedance.

Here again, if the load resistance is positive, the system will be stable. With positive load resistance, all coefficients in the denominator are positive and nonzero, guaranteeing that all poles are negative. If the load resistance is negative, the following conditions must be met to have strictly positive coefficients:

$$\frac{R_S}{L} + \frac{1}{CR} > 0 \tag{3.8}$$

and

$$\frac{(R+R_S)}{LCR} > 0 \tag{3.9}$$

These two equations reduce to

$$\begin{cases} R > 0 \\ \quad or \\ R < -\dfrac{L}{CR_S} \end{cases} \tag{3.10}$$

and

$$R > -R_S \tag{3.11}$$

For negative load resistance, it is more intuitive to use the magnitude of the negative resistance than the resistance itself. By substituting $R = -|R|$ into Equations (3.10) and (3.11), the two stability requirements for a system with negative resistance become

$$|R| > \frac{L}{CR_S} \tag{3.12}$$

and

$$|R| < R_S \tag{3.13}$$

Both of these requirements must be met to guarantee that all coefficients of the denominator of the transfer function are greater than zero. However, because both equations depend on R_S, they are not mutually exclusive. This being the case, not all combinations of L, C, and R_S allow for a system with positive coefficients in the denominator of the transfer function. To allow both equations to be satisfied, R_S must meet the following requirement:

$$R_S > \sqrt{\frac{L}{C}} \tag{3.14}$$

If this condition is met, the two criteria for $|R|$ for positive coefficients can be satisfied simultaneously, and the expressions can be combined into

$$\frac{L}{CR_S} < |R| < R_S \tag{3.15}$$

Notice again that this expression implies that a larger source resistance eases the stability requirements because a wider range of load magnitudes can be accommodated.

While positive coefficients in the denominator of the transfer function ensure that both of the poles will be less than zero, there are stable systems that do not satisfy this condition. To further analyze this situation, it is instructive to look at the root locus of the two poles as the load

resistance is varied from $-\infty$ to ∞. A root-locus plot for a particular system is shown in Figure 3.4.

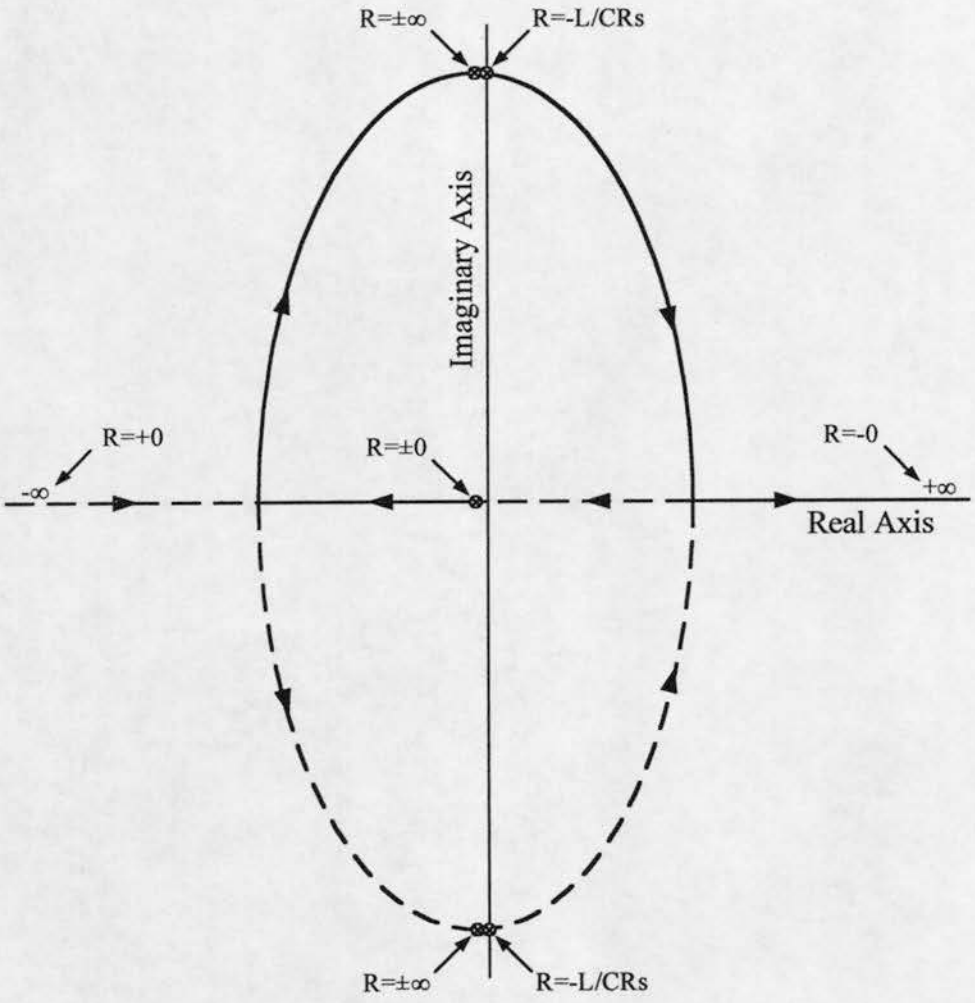

Figure 3.4: Root locus plot of poles for system with RLC source impedance.

In this plot, the locus for one pole is drawn with a solid line, and the other is dashed. Here, the actual resistance R is being used rather than the magnitude $|R|$ to accommodate positive resistance loads as well. The two poles trace a path that encompasses the entire real axis, as well as forming an ellipse. Some good insight can be obtained in analyzing this graph and how it changes as the parameters are varied.

The plot, as drawn, represents a system that will be unstable for a large range of the negative load impedance. When $R = -\infty$, the two poles are located on the ellipse, with their location given by

$$-\frac{R_S}{2L} \pm \sqrt{\left(\frac{R_S}{2L}\right)^2 - \frac{1}{LC}} \tag{3.16}$$

In this example, the system is stable when $|R|$ is very large. As R increases, the poles follow the ellipse to the right. Eventually, they cross the imaginary axis when

$$R = -\frac{L}{CR_S} \quad \text{or} \quad |R| = \frac{L}{CR_S} \tag{3.17}$$

For this value of $|R|$ or less, the system will be unstable. This is the same condition given in Equation (3.12). Note that for this particular system, Equation (3.13) is not required for stability, although it is required to have positive coefficients. As R continues to increase, the poles eventually merge at the real axis, becoming a double pole. At this point, both poles travel along the real axis, with one heading left and the other right. As R approaches zero, one pole approaches $+\infty$, and the other approaches the center of the ellipse at

$$real = -\frac{R_S}{L} \tag{3.18}$$

As R passes through zero, the pole at $+\infty$ jumps to the center of the ellipse, and the other pole jumps to $-\infty$. Both poles are now in the left half-plane, where they will stay. Therefore, the system is stable for any positive load resistance. As R increases, the two poles travel towards each other on the real axis. They eventually meet and leave the real axis, following the ellipse in opposite directions. As R approaches $+\infty$, the two poles approach the same locations that they started out at when $R = -\infty$.

The size and location of the ellipse are controlled by the parameters of the circuit, as would be expected. However, the size of the ellipse is independent of the source resistance R_S, and depends only on the inductance L and capacitance C. The height-to-width ratio of the ellipse remains constant at 2:1. The width is given by

$$width = \frac{2}{\sqrt{LC}} \tag{3.19}$$

and the height by

$$height = \frac{4}{\sqrt{LC}} \tag{3.20}$$

The ellipse is always centered on the real axis because imaginary roots must be complex conjugates. Its location in relation to the imaginary axis depends on the source resistance R_S and inductance L, and is given by

$$real = -\frac{R_S}{L} \tag{3.21}$$

This equation shows that the real axis location of the ellipse is directly proportional to the negative of the source resistance. Therefore, as the source resistance is increased, the ellipse will move farther to the left, making the system stable for more values of negative load resistance. Note that when the source resistance is zero, the ellipse is centered at the origin, as represented by the solid ellipse in Figure 3.5. In this case the system is stable for positive loads and unstable for all values of negative load resistance. The small circles in Figure 3.5 represent the dividing point between positive and negative values of R, with positive values to the left and negative values to the right. As the source resistance increases, the ellipse moves to the left, and the system becomes stable for some high impedance negative loads. The critical value occurs when

$$R = -\frac{L}{CR_S} \tag{3.22}$$

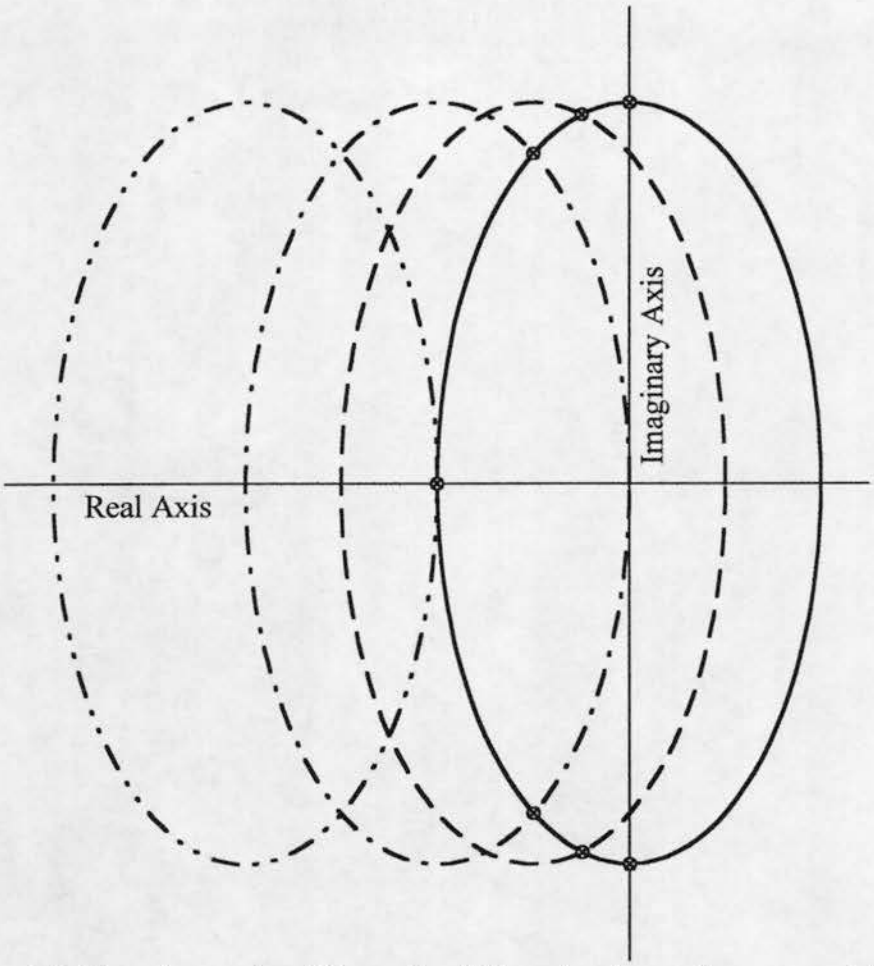

Figure 3.5: Root locus plot ellipses for different values of source resistance.

At this point, the two poles fall on the imaginary axis, and the system will oscillate. Values of R less than this value (higher values of $|R|$) will be stable, and greater values of R ($|R|$ smaller) will be unstable. An example of this case is shown as the dashed ellipse in Figure 3.5. As R_S continues to increase, more of the ellipse enters the stable left half-plane, until

$$R_S = \sqrt{\frac{L}{C}} \tag{3.23}$$

Here, the entire ellipse is in the left half-plane as shown by the dash-dotted ellipse in Figure 3.5. At this point, any imaginary poles will be stable. This is the same requirement that

allows both of the conditions for positive denominator coefficients to be satisfied simultaneously. When R_S increases to the value of

$$R_S = 2\sqrt{\frac{L}{C}} \tag{3.24}$$

the poles associated with negative values of R will no longer fall on the ellipse. This condition is shown as the dash-double-dotted ellipse in Figure 3.5. For values of R_S greater than this, the stability requirement is entirely governed by

$$R > -R_S \quad \text{or} \quad |R| < R_S \tag{3.25}$$

for negative resistances. For this system, therefore, it becomes clear that for a negative load resistance, a larger value of source impedance will tend to stabilize the system. Increasing the capacitance or decreasing the series inductance will also aid in stability.

To clarify the stability issues associated with the system in Figure 3.3, consider a simple low-power example. In this case, Figure 3.3 represents a single-phase of a 480-V grounded-wye three-phase system providing 3 kW to the load. For each phase, the rms phase-to-ground voltage is 277 V. The source resistance and inductance are 100 mΩ and 5 mH, respectively, and the shunt capacitance is 100 μF. Each phase delivers 1 kW to the load, making the effective resistance 76.7 Ω for a resistive load, and –76.7 Ω for a constant power load. The response of the system for both resistive and constant power loads is shown in Figure 3.6, where (a) shows the input source voltage. As discussed previously, for a linear resistive load, the system is stable. The output voltage for the system with a positive resistive load is shown in Figure 3.6(b). If the same system is driving a constant power load, on the other hand, the system is unstable with the output voltage growing over time as shown in Figure 3.6(c). This is due to the system poles being in the right half-plane. However, if the source resistance is increased to 1 Ω, the poles are

moved into the left half-plane, stabilizing the system. The output voltage for the system driving a constant power load with 1 Ω of source resistance is shown in Figure 3.6(d).

Increasing the source resistance may be a practical solution to correct stability problems for a low-power system. However, at higher power levels, the impedance of the distribution system is generally kept as low as possible to minimize power loss, and the shunt capacitance is likewise relatively small. This type of system is difficult to stabilize simply by increasing resistance or capacitance because the values required are too large to be practical.

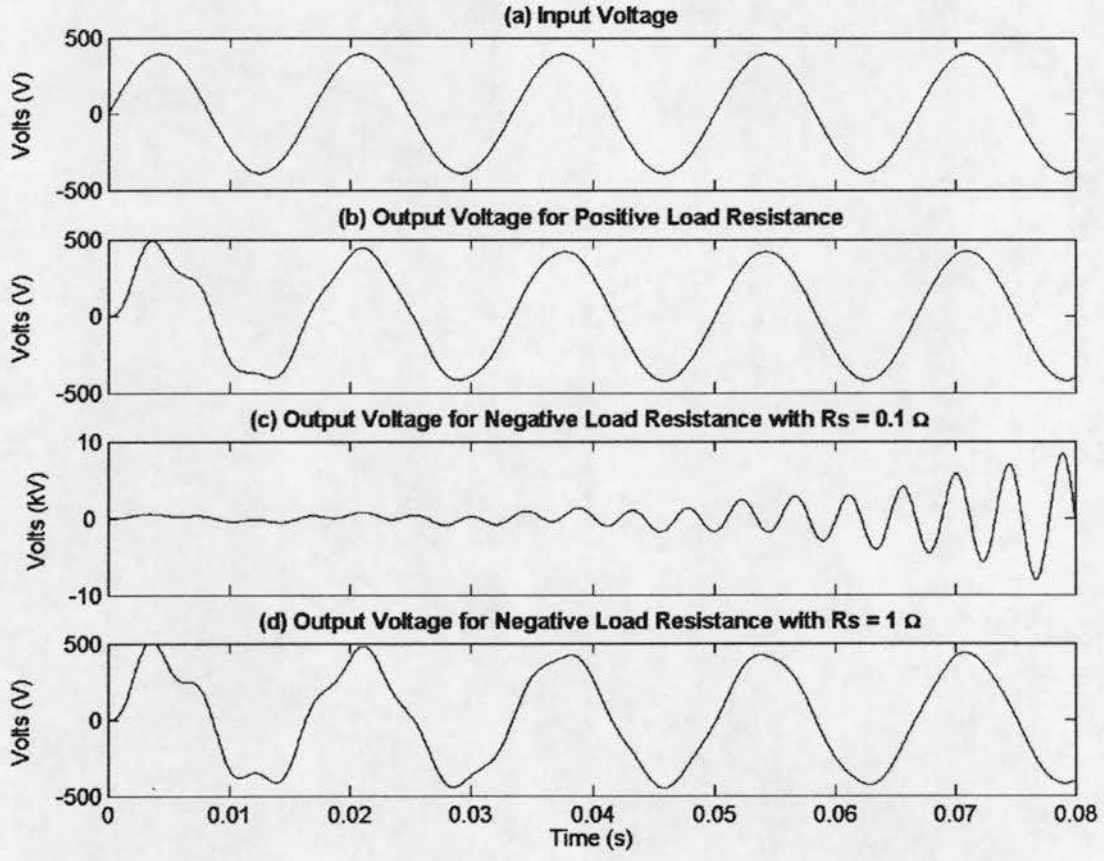

Figure 3.6: System response of system with RLC source impedance.

4. NEGATIVE IMPEDANCE CHARACTERISTICS OF PFC RECTIFIERS

The previous section detailed how a load with negative resistance can interact with the RLC components of the distribution system to cause instability. From that analysis, if the characteristic values of the distribution system are known, limits can be placed on the value of a negative resistance load that will keep the system stable. In general, this requires keeping the magnitude of the negative resistance high, meaning that increases in current draw due to a voltage sag must be limited to some value.

What remains to be shown is how power-factor corrected rectifiers can exhibit a negative impedance to the source. While the complete model of input impedance over all frequencies becomes rather complicated, analyzing the system over different frequency ranges allows for some simplifying assumptions that keep the analysis manageable and intuitive.

For time scales much faster than the switching frequency of the rectifier, the source will not see the effects of any switching action. Referring to the power buffer schematic in Figure 2.7, page 11 and assuming a reasonably sized capacitor on the dc bus, the bus voltage will appear constant for high frequencies. Therefore, at high frequencies the input impedance of the rectifier is the series resistance and inductance appearing before the switches, and will not be negative.

To analyze the system at frequencies significantly below the switching frequency, some simplifying assumptions can be made. At lower frequencies, the value of the input current is determined by the switch action, and the input impedance is defined by the operation of the control rather than by the series impedance. Therefore, the dynamic equations governing the series input impedance are not used. This remains valid as long as at the frequencies of interest the voltage across the series input impedance $R + j\omega L$ remains small compared to the input voltage. To limit the variables and make the presentation more intuitive, the analysis will be

performed on the single-phase PFC rectifier as shown in Figure 2.5, page 9. The analysis for the three-phase case is identical, except that the expression for the current delivered to the dc bus, i_{CIN}, is more complicated because it depends on all three separate phase voltages.

Because we are looking for the characteristics of the PFC system in response to a change in input voltage, it is more intuitive to look at the input admittance than the impedance. Recall that the reference input current the control is trying to match is given by

$$i_{IN} = \left(\frac{i_{REF}}{V_{NOM}} \right) v_{IN} \tag{4.1}$$

Here V_{NOM} is simply a constant equal to the nominal peak voltage of the input. Therefore, if i_{REF} is constant, the equation is equivalent to Ohm's law with $R = (V_{NOM}/i_{REF})$. This, of course, is the desired steady-state operation of the system and results in a unity power factor. During transients, however, i_{REF} will vary as the control tries to keep the dc bus voltage constant. It is this effect that leads to negative input impedance. Recall that i_{REF} is the output of a PI controller and can be expressed as

$$i_{REF} = \left(k_p + \frac{k_i}{s} \right) (V_{REF} - v_{DC}) \tag{4.2}$$

Because k_p, k_i, and V_{REF} are constants, the expression for di_{REF}/dv_{IN} is

$$\frac{di_{REF}}{dv_{IN}} = -\left(k_p + \frac{k_i}{s} \right) \frac{dv_{DC}}{dv_{IN}} \tag{4.3}$$

Here, the inverse relationship between i_{REF} and v_{DC} is apparent. As the dc bus voltage decreases, the reference current will increase, and vice versa. The dc bus voltage is defined by the differential equation for the capacitor voltage:

$$v_{DC} = \frac{1}{sC} (i_{CIN} - i_{LOAD}) \tag{4.4}$$

In a power buffer, the dc bus feeds the input of the inverter supplying the actual load. As long as the dc bus voltage remains above the peak output voltage of the inverter, the inverter draws constant power. Therefore, i_{LOAD} is defined as

$$i_{LOAD} = \frac{P}{v_{DC}} \tag{4.5}$$

where P is the power drawn by the load.

The value of i_{CIN} depends on the position of the switches. In the single-phase PFC rectifier, if the input filter inductor is switched to the positive capacitor terminal, $i_{CIN} = i_{IN}$. If the inductor is switched to the negative capacitor terminal, $i_{CIN} = -i_{IN}$. Because we are interested in frequencies lower than the switching frequency, we can use an average value of i_{CIN} defined as

$$i_{CIN} = Qi_{IN} \tag{4.6}$$

Here Q ranges from –1 to 1, where positive values indicate current into the positive capacitor terminal and negative values indicate current into the negative terminal. In the quasi-static state we are looking at, Q will assume a value that keeps the current through the input inductor constant. Ignoring the series resistance, the voltage across the input inductor is

$$v_L = \left(v_{IN} - Qv_{DC}\right) \tag{4.7}$$

For v_L to be zero, Q must be

$$Q = \frac{v_{IN}}{v_{DC}} \tag{4.8}$$

Now, substituting Equations (4.1), (4.5), (4.6), and (4.8) into Equation (4.4) gives

$$v_{DC} = \frac{1}{sC}\left(\left(\frac{v_{IN}}{v_{DC}}\right)\left(\frac{i_{REF}v_{IN}}{V_{NOM}}\right) - \frac{P}{v_{DC}}\right) \tag{4.9}$$

which can be rewritten as

$$sCV_{NOM}v_{DC}^2 = i_{REF}v_{IN}^2 - V_{NOM}P \tag{4.10}$$

Taking the derivative with respect to v_{IN} of both sides of Equation (4.10) gives

$$s2CV_{NOM}V_{DC}\frac{dv_{DC}}{dv_{IN}} = V_{IN}^2\frac{di_{REF}}{dv_{IN}} + 2I_{REF}V_{IN} \tag{4.11}$$

Now, combining Equations (4.3) and (4.11) gives us an expression for di_{REF}/dv_{IN}:

$$\frac{di_{REF}}{dv_{IN}} = -(2I_{REF}V_{IN})\frac{k_p s + k_i}{2CV_{NOM}V_{DC}s^2 + k_p V_{IN}^2 s + k_i V_{IN}^2} \tag{4.12}$$

The actual input admittance is di_{IN}/dv_{IN}. Rewriting Equation (4.1) gives

$$i_{IN} = \frac{1}{V_{NOM}}(i_{REF}v_{IN}) \tag{4.13}$$

Because both i_{REF} and v_{IN} are dependant on v_{IN}, the expression for the input admittance is

$$\frac{di_{IN}}{dv_{IN}} = \frac{1}{V_{NOM}}\left(I_{REF} + V_{IN}\frac{di_{REF}}{dv_{IN}}\right) \tag{4.14}$$

Substituting in Equation (4.12) and simplifying leads to

$$\frac{di_{IN}}{dv_{IN}} = \frac{I_{REF}}{V_{NOM}} - \left(\frac{2I_{REF}V_{IN}^2}{V_{NOM}}\right)\left(\frac{k_p s + k_i}{2CV_{NOM}V_{DC}s^2 + k_p V_{IN}^2 s + k_i V_{IN}^2}\right) \tag{4.15}$$

This expression defines the input admittance of the PFC rectifier driving a constant power load for frequencies below the switching frequency, and provides some enlightenment to its operation. At higher frequencies, the second term will approach zero, reducing the admittance expression to

$$\left.\frac{di_{IN}}{dv_{IN}}\right|_{s\to\infty} = \frac{I_{REF}}{V_{NOM}} \tag{4.16}$$

This reflects the delay of the system in changing i_{REF}. At higher frequencies, the voltage on the capacitor will not change much, keeping the control from changing i_{REF}. Thus, for these

frequencies, the impedance appears resistive. At low frequencies, on the other hand, the admittance expression approaches

$$\left.\frac{di_{IN}}{dv_{IN}}\right|_{s\to 0} = -\frac{I_{REF}}{V_{NOM}} \tag{4.17}$$

Because I_{REF} is equivalent to the peak input current during steady-state conditions, this expression indicates how a heavily loaded system can be unstable. In this case, the input impedance is

$$Z_{IN}|_{s\to 0} = -\frac{V_{NOM}}{I_{REF}} \tag{4.18}$$

The more power the system draws, the higher I_{REF} becomes, decreasing the magnitude of the input impedance. As was shown in the previous section, for negative impedance, the stability of the system deteriorates as the magnitude of the impedance drops.

5. POWER BUFFER OPERATION DURING UTILITY DISTURBANCES

The key advantage of using a power buffer is the protection it provides to both the distribution system and to the load. By dynamically decoupling the load from the source, stability issues that arise from the interaction of constant power loads and the distribution system can be corrected. Additionally, the energy storage of the power buffer protects the load from disturbances on the distribution system.

5.1. System Stability

As discussed in Chapter 3, the interaction of a constant power load with the impedance of the distribution system can lead to instability. While a power buffer can be used to decouple the dynamics of a constant power load from the distribution system, the buffer itself can act as a constant power load if its dynamic response is fast. To illustrate, consider the single-phase PFC rectifier of Figure 2.5, page 9, supplied by the distribution system of Figure 3.3, page 23. The rectifier has 10 μF of capacitance on the dc bus and is driving a 1000-W, constant power load. The control of the PFC rectifier is designed to respond quickly to changes in input voltage or load power. The source resistance R_S of the distribution system is 100 mΩ, the source impedance L is 5 mH, and the shunt capacitance C is 100 μF. The system is operating at 277 V rms, and experiences a sag to 30% for 200 ms. The response of the system is shown in Figure 5.1.

The source voltage is shown in Figure 5.1(a) with the sag beginning at 0.4 s. The buffer input voltage and the dc bus voltage are shown in Figure 5.1(b). Note that the input voltage to the buffer is distorted both during and after the sag. Additionally, after the sag is removed, the voltage oscillates slightly at about 15 Hz. Throughout the event, however, the dc bus voltage remains relatively constant. This is because the buffer input current increases to compensate for

the voltage sag. Both the buffer input current and the reference current generated by the control are shown in Figure 5.1(c).

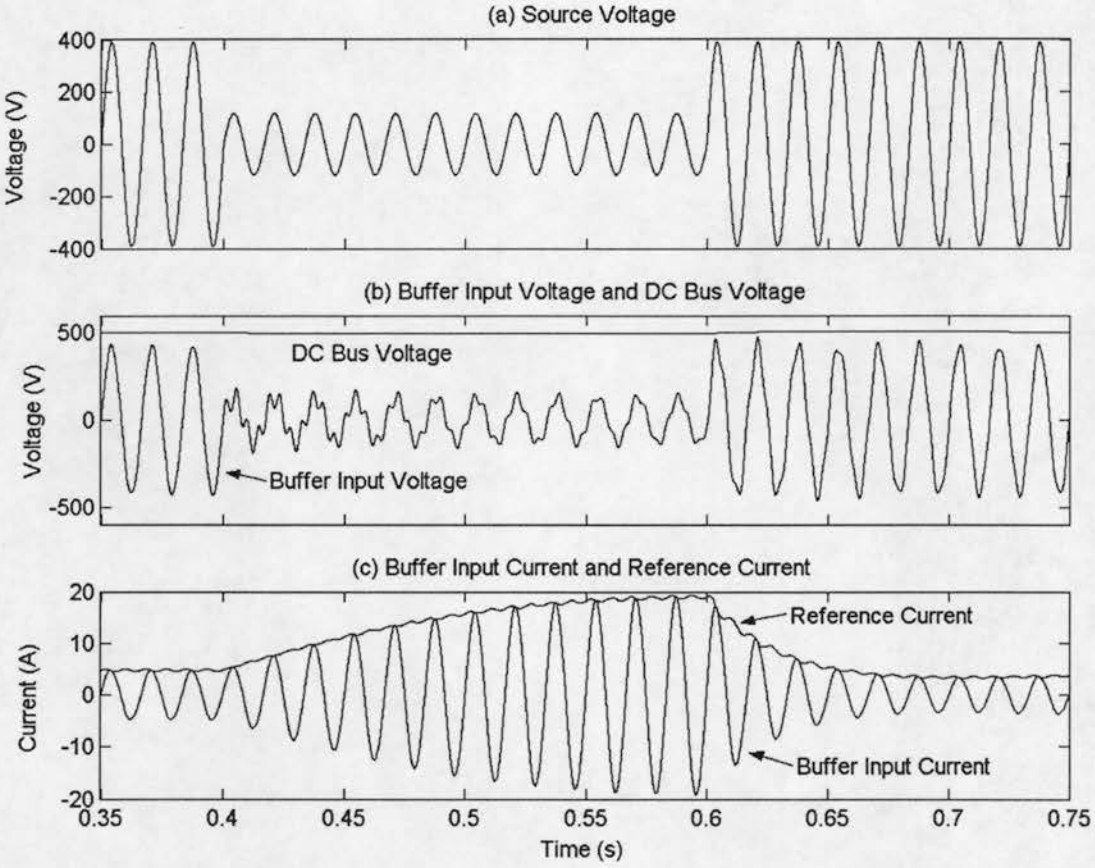

Figure 5.1: Unstable system response of distribution system with constant power load.

As discussed in Chapter 3, modifying the distribution system by increasing the source resistance and the shunt capacitance can improve the system stability. In this example, increasing the source resistance to 500 mΩ and the shunt capacitance to 300 μF stabilizes the system without altering the operation of the PFC rectifier. The results of applying the same sag to the modified system are shown in Figure 5.2. Once again, Figure 5.2(a) shows the source voltage, Figure 5.2(b) shows the buffer voltages, and Figure 5.2(c) displays the currents. The buffer input voltage is now steady and sinusoidal within about three cycles of each voltage step. The operation of the PFC rectifier was not altered, so the buffer current remains relatively unchanged.

The slight difference in the current magnitudes between Figures 5.1(c) and 5.2(c) is due to the voltage increase at the input of the buffer from the added capacitance on the distribution system.

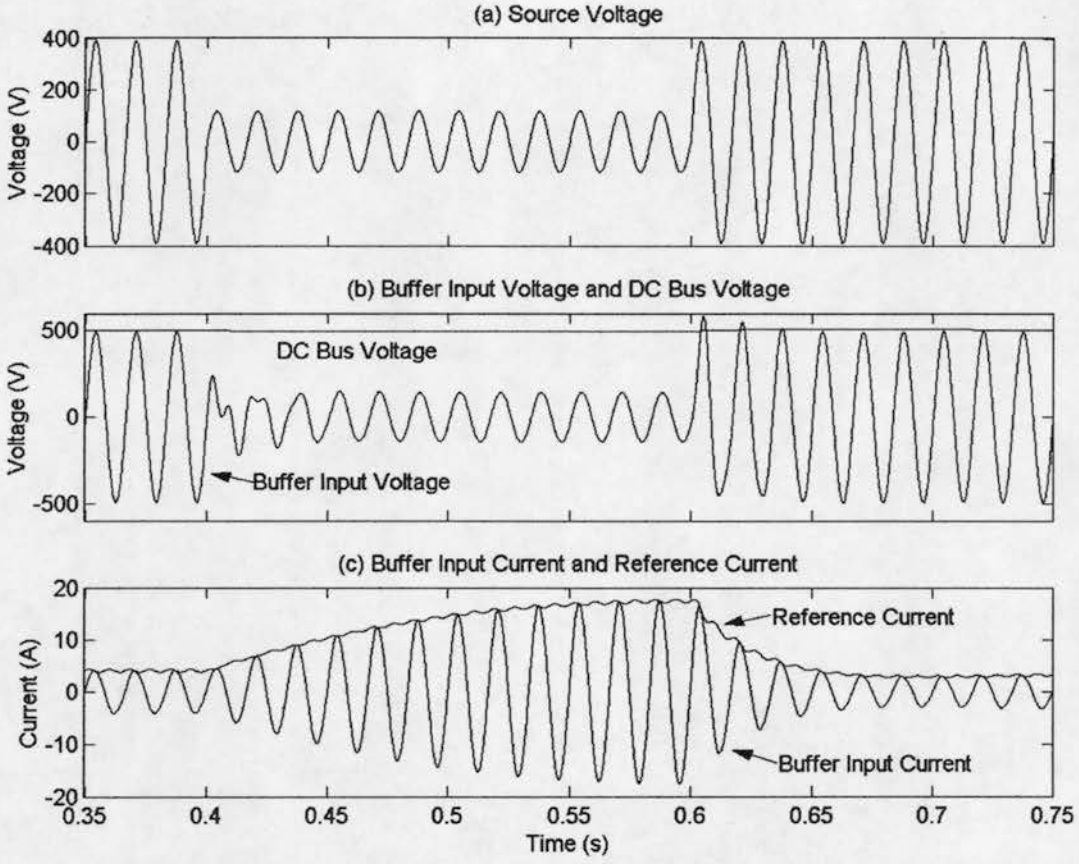

Figure 5.2: Stable system response of distribution system with constant power load.

Generally, modifying the distribution system is not a practical solution. Increasing the source resistance increases power loss, and adding capacitance can magnify transients from other switching operations on the system. Fortunately, changing the control of the PFC rectifier can alter the incremental impedance of the buffer and improve system stability without modifying the distribution system.

The control method described in Chapter 2 attempts to match the input current waveform to the input voltage. As shown in Equations (4.15) and (4.16), the high-frequency response of this type of control leads to resistive behavior at the onset of a disturbance. Therefore, for a rapid

change in voltage, as occurs during a sag, the buffer appears to be a resistive load to the distribution system. As time goes on, the incremental impedance of the buffer becomes negative to compensate for the voltage change on the dc bus, with the magnitude determined by the controller gains and the bus capacitance. However, the response of the buffer to any subsequent step change in the voltage will appear to be resistive.

To demonstrate the stability improvement that can be obtained with this control method, consider the original distribution system with $R_S = 100\ \text{m}\Omega$, $L = 5\ \text{mH}$, and $C = 100\ \mu\text{F}$. The power buffer is identical except for the control. The control method described in Chapter 2 is used with the proportional gain set at one and the integral gain set at ten. The results are shown in Figure 5.3.

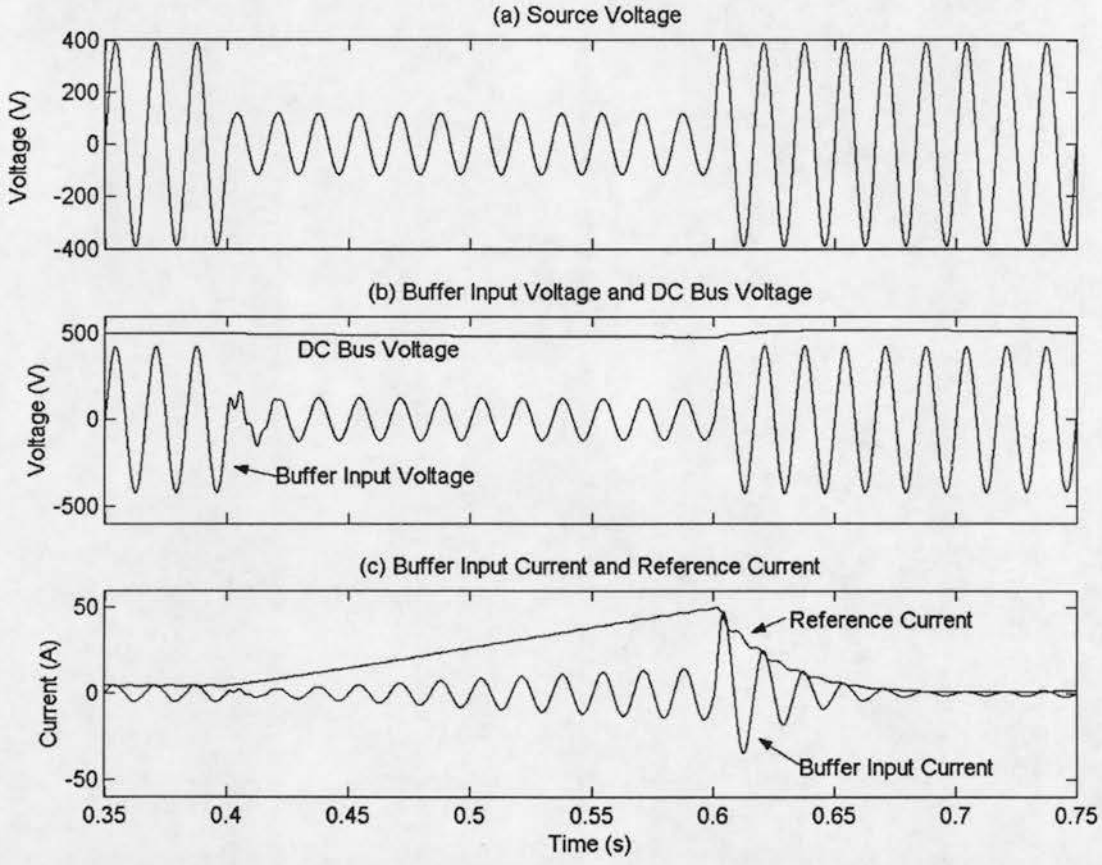

Figure 5.3: System response using the power buffer control.

The source voltage reflecting the sag is shown in Figure 5.3(a). The buffer input voltage and the dc bus voltage are shown in Figure 5.3(b). The buffer input voltage is now stable both during and after the sag. However, because the rate of change of the reference current isn't limited, the attempt of the control to compensate for the decrease in input voltage causes the reference current to increase almost tenfold during the 200 ms sag. Although the initial change of the input current is limited by the reduction of the input voltage, when the voltage is restored, the initial resistive behavior of the buffer causes it to draw a large current from the source. Both the reference current and the buffer input current are shown in Figure 5.3(c).

One way to avoid this effect is to directly limit the rate of change of the reference current. This slows down the response of the buffer, and for short disturbances the buffer can behave quite resistively. Including this limit on the reference current to the buffer in the previous example leads to the response shown in Figure 5.4.

The same sag is applied to the source voltage as shown in Figure 5.4(a). The buffer voltages are given in Figure 5.4(b), and the currents in Figure 5.4(c). In this example, the current reference changes very little over the course of the sag, allowing the incremental impedance of the buffer to appear resistive to the distribution system.

5.2. Energy Storage Requirements

The disadvantage of slowing the system response is that it will increase the variance of the dc bus voltage. If the bus voltage becomes too low, there will not be enough voltage to allow the inverter to operate properly, and if it becomes too high, it can damage the switches or the capacitor itself. To prevent this, more energy storage is needed. The simplest way to do this is to increase the size of the capacitor. During a disturbance, the capacitor will supply the needed energy to the load until the control catches up. Adding additional energy storage creates another

benefit by providing the system the opportunity to ride through brief disturbances that may occur on the distribution system.

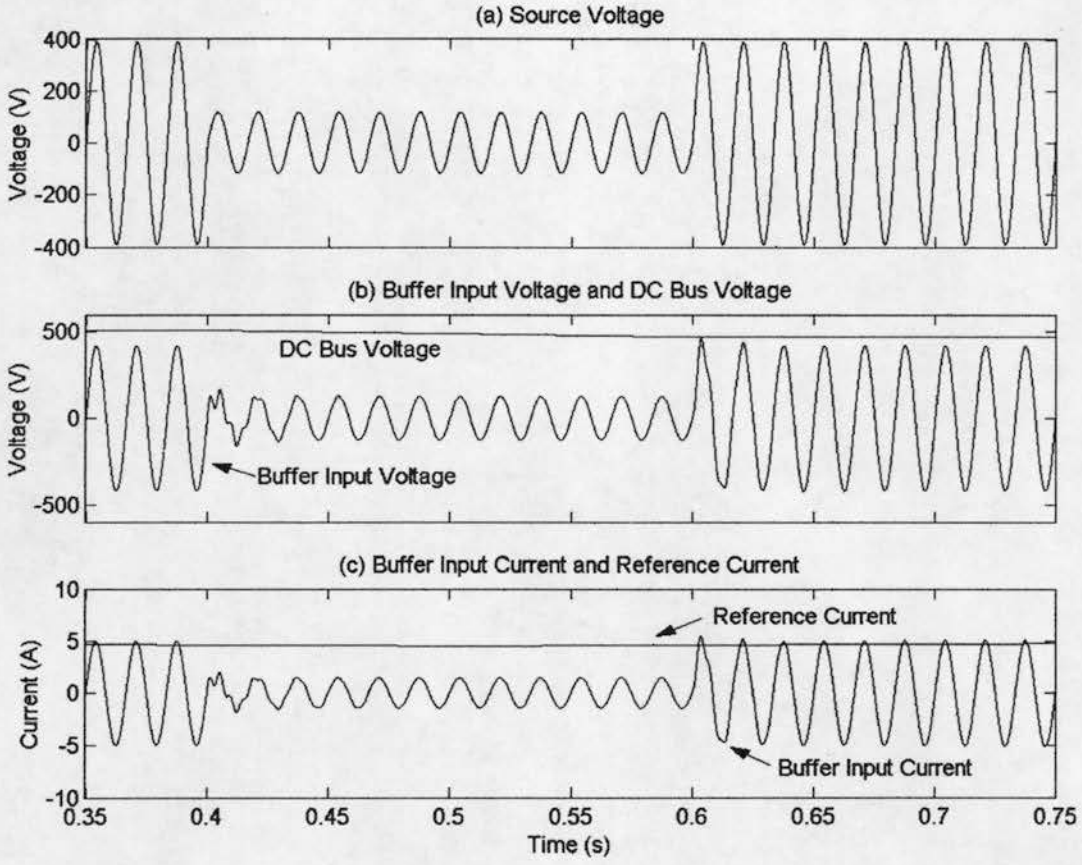

Figure 5.4: System response with rate limit on reference current.

For sizing the capacitor, two different conditions need to be considered. The first concerns a severe sag or an interruption on the system. In this case, the buffer will not be able to draw enough energy from the distribution system to run the load until the system recovers. Here, the capacitor is required to provide all of the power to the load, and its size determines how long it is able to do this. The second condition occurs when a sag or swell on the system is small enough that the system can still provide power to the load. Under this condition, the buffer will eventually compensate for the disturbance and provide continuous power to the load. The

capacitor is only required to provide additional power to the load (or absorb addition power for a swell) until the control catches up to the event.

The capacitor size required to supply the load of a power buffer during a complete interruption can be found as follows. The energy stored in a capacitor is $\frac{1}{2}CV^2$. During the interruption, the capacitor must supply all power to the load. Because the inverter driving the load is a constant power device, the energy drawn from the capacitor bank is simply $P\Delta t$, where P is the load power, and Δt is the duration of the outage. The energy delivered by the capacitor is simply the difference between the starting and final values of the capacitor energy. Equating this to the energy drawn by the load leads to the equation

$$P\Delta t = \frac{1}{2}CV_{DC}^2 - \frac{1}{2}C(V_{DC} - \Delta V_{DC})^2 \tag{5.1}$$

which reduces to

$$C = \frac{P\Delta t}{\Delta V_{DC}\left(V_{DC} - \frac{1}{2}\Delta V_{DC}\right)} \tag{5.2}$$

where ΔV_{DC} is the allowed voltage change across the capacitor.

The required capacitor size that allows the power buffer to protect the load indefinitely during a minor sag or swell can be found as follows. The allowable rate of change of the reference current magnitude i_{REF} is m_{IREF}. Assuming that i_{REF} changes linearly at this rate following an event, the energy change that the capacitor must accommodate is

$$\Delta E = \frac{1}{2}(1 - a^2)P\Delta t \tag{5.3}$$

In this case, a is the ratio of the voltage during the disturbance to the steady-state voltage, and Δt is the time it takes the reference current to change to the level required to supply all of the load power. In terms of the steady-state current I_{SS}, Δt is

$$\Delta t = \frac{I_{SS}}{m_{IREF}}\left(\frac{1-a}{a}\right) \tag{5.4}$$

Substituting ΔE from Equations (5.3) and (5.4) for $P\Delta t$ in Equation (5.2), the required capacitor size can be found as

$$C = \left(\frac{PI_{SS}}{2am_{IREF}}\right)\frac{(1-a)(1-a^2)}{\Delta V_{DC}\left(V_{DC} - \frac{1}{2}\Delta V_{DC}\right)} \tag{5.5}$$

5.3. Power Buffer Effects on the Load

Up to this point, the discussion has focused on the effects that the power buffer and power factor correction in general have on the utility distribution system. However, because the dc bus isolates the load from the utility source, using a power buffer, provides the load protection from disturbances on the utility. This section will briefly discuss the types of utility disturbances and the protection that a power buffer can provide to the load.

Disturbances on the utility distribution system can be grouped into the following main catagories [1]:

- Transients
- Short-duration variations
- Long-duration variations
- Voltage imbalance
- Waveform distortion
- Voltage fluctuations
- Power frequency variations

The following sections discuss the effects of each of these types of disturbances on a load protected by a power buffer.

5.3.1. Transients

There are two basic types of transients that occur on a power system: impulsive and oscillatory. Lightning is the main cause of impulsive transients, and they are characterized as

unidirectional, high-magnitude transients with fast rise and fall times. Lightning transients usually disappear within microseconds. As described in IEEE C37.34, the standard waveform used to test for lightning resistance is a 1.2 × 50 μs impulse with a peak voltage defined by the system voltage [18]. For indoor gear on a 15-kV system, the peak voltage is 95 kV. The 1.2 × 50 μs definition means that the impulse rises from zero to its peak voltage in 1.2 μs, and decays to half of its peak value in 50 μs.

As the name implies, oscillatory transients consist of a damped sinusoidal waveform with a frequency that is generally much higher than the power frequency. Oscillatory transients are the result of the RLC components of the system interacting in response to switching or impulsive events. They are generally initiated by capacitor switching, cable switching, transformer energization, or lightning impulses. The voltage magnitude of oscillatory transients is generally limited to a maximum of 200% of the peak system voltage, and is usually less.

The dc bus of the power buffer does an excellent job of protecting the load from both impulsive and oscillatory transients because both types are generally of a short duration compared to the power frequency. Over such a short time, the dc bus voltage will not change significantly, keeping the load from seeing any effect of a transient. The main danger to a power buffer system from utility transients is to the buffer itself. The switches and inductors of the PFC rectifier must be able to withstand the transient voltage and current without damage. Because the voltage magnitude of oscillatory transients is limited, it may be possible to design the components to withstand these transients without additional protection. Lightning impulsive transients, on the other hand, can produce very high voltages on the system, and generally require additional components for protection. If the power buffer is connected to the utility system through a transformer as shown in Figure 2.7, page 11, the impedance of the transformer

will help to limit transient currents. In this case, placing lightning surge arresters at the input of the system may provide adequate protection.

5.3.2. Short-duration variations

Short-duration variations of the system voltage consist of interruptions, sags, and swells, and are generally caused by faults on the system, energization of large loads, or other load changes. The ability of a power buffer to protect the load against these voltage variations is dependent on the size of the dc bus capacitor, and the duration and magnitude of the event.

An interruption occurs when the system voltage drops below 10% of its nominal value. In this situation, the buffer will not be able to draw enough power from the distribution system to compensate for the low input voltage, and the power to the load must be supplied almost entirely by the dc bus capacitor. The amount of time that the buffer will be able to support the load can be found by rearranging Equation (5.2):

$$\Delta t = \frac{C\Delta V_{DC}}{P}\left(V_{DC} - \frac{1}{2}\Delta V_{DC}\right) \tag{5.6}$$

As expected, the holdup time is directly proportional to the capacitance and the allowed voltage variation, and inversely proportional to the load power. As long as enough energy storage is provided, a power buffer will allow the load to ride through a short-duration interruption without any variation on the load voltage. However, to support a large load for any appreciable length of time, the required energy storage will soon exceed the practical limits of capacitors.

A sag occurs when the voltage drops to between 10% and 90% of its nominal value. For severe sags, the power buffer has the same limitations as during an interruption. However, for minor sags, if enough capacitance is provided to allow the buffer to adjust its current draw to provide the required power, the buffer will allow the load to ride through the disturbance indefinitely. Because the PFC rectifier operates as a boost converter, a sag at the source requires

the system to increase the boost to hold the dc bus constant, increasing the source current. As an example, consider again the power buffer in Figure 2.7, page 11. The buffer operates on a 480-V, three-phase system and delivers power to a 115-kW load. The dc bus has a nominal value of 800 V, and has 20 mF of bus capacitance. At 0.1 s, the distribution system experiences a 70% sag for 50 ms. Figure 5.5 shows the effects of the sag on the system. Figures 5.5(a) and (b) show the source voltage and current, while Figures 5.5(c) and (d) show the dc bus voltage and the load voltage. Notice that the load voltage is unaffected by the disturbance. Because the response of the buffer is slow, the dc bus voltage drops initially, but remains high enough to allow the inverter to operate properly.

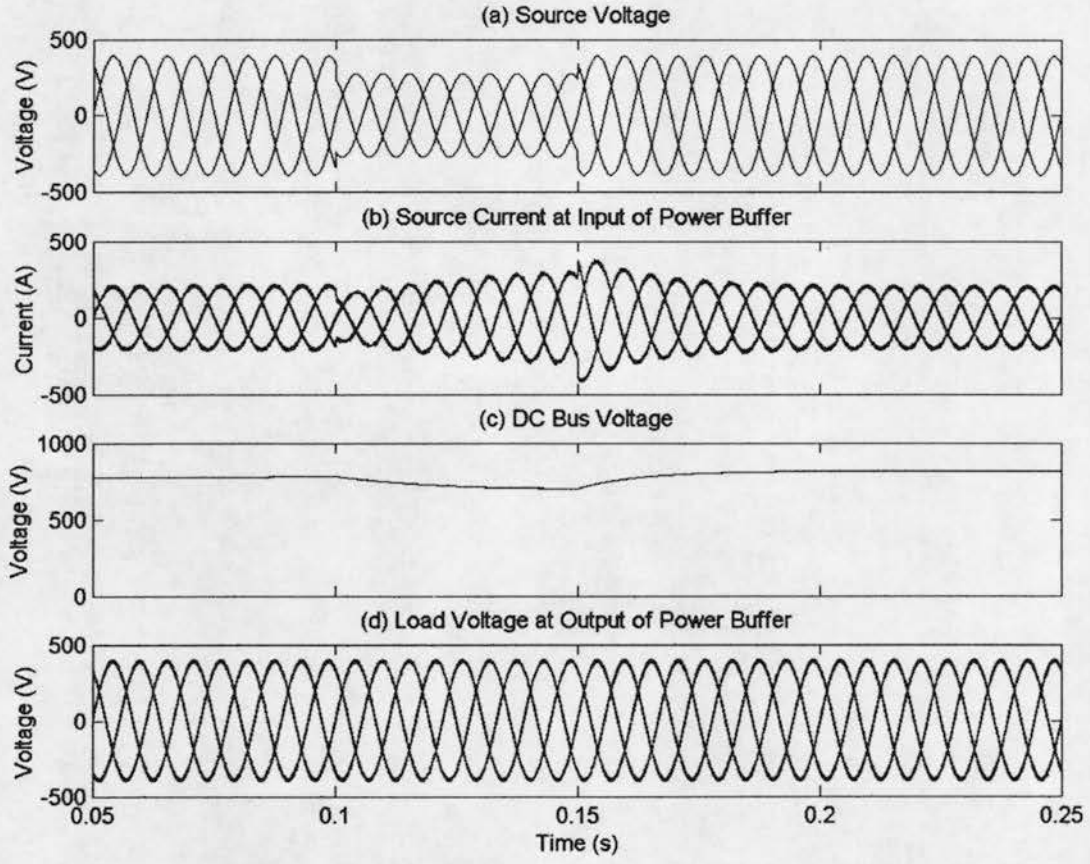

Figure 5.5: System response of power buffer system during a voltage sag.

A swell on the utility system occurs when the system voltage increases above 110% of its nominal value. For proper operation of the buffer, the voltage on the dc bus must remain higher than the peak voltage at the input. Therefore, in a three-phase system without adjusting the dc bus voltage, the power buffer can protect against swells until the peak phase-to-phase input voltage equals the dc bus voltage. Beyond this point, the PFC rectifier would no longer be able to operate properly as a boost converter. However, if the voltage rating of the dc bus capacitors has enough headroom, the dc bus voltage can be increased during a swell to allow for proper operation of the boost rectifier. This will increase the depth of modulation of the output inverter and may decrease the efficiency, but this is preferable to disturbing the load. Because the input voltage increases during a swell, the required current to supply a constant power load drops, and the current handling ability of the buffer is not an issue. As for a sag, if the dc bus capacitance is large enough to allow the power buffer to adjust its current draw appropriately, the buffer can ride through a minor swell indefinitely. Using the same power buffer system as for the sag example, Figure 5.6 shows the system response to a 20% swell for 50 ms. Figures 5.6(a) and (b) show the source voltage and current, and Figures 5.6(c) and (d) show the dc bus voltage and the load voltage. Again, the load is unaffected by the disturbance.

5.3.3. Long-duration variations

Long-duration variations consist of sustained interruptions, undervoltages, and overvoltages that last for over one minute. The definition of these disturbances is identical to their short-duration counterparts with the only difference being the duration. A power buffer can protect the load from undervoltage and overvoltage variations within the same guidelines as for short-duration sags and swells. However, a buffer cannot protect the load against a sustained interruption. One minute is a long time for even a full-sized UPS system to supply the entire

load. True protection from a sustained interruption generally requires either a backup generator or an independent alternate source.

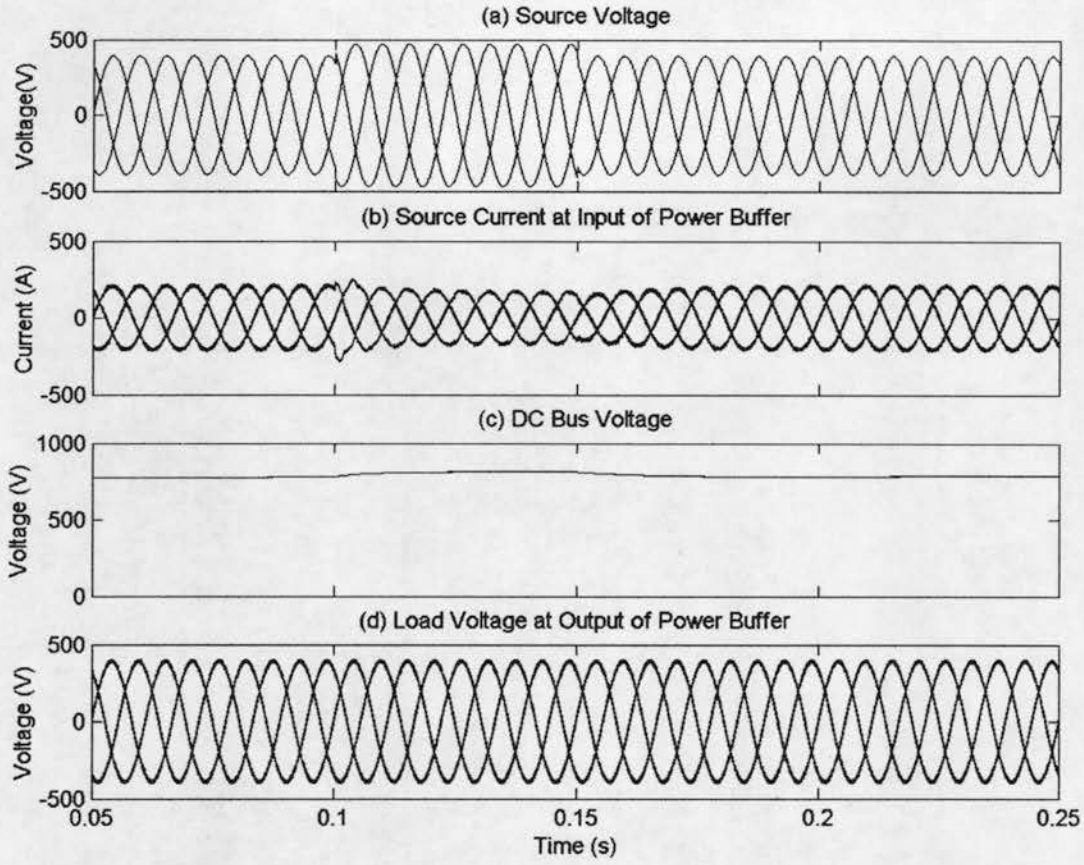

Figure 5.6: System response of power buffer system during a voltage swell.

5.3.4. Voltage imbalance

On a three-phase distribution system, voltage imbalance occurs when the voltage magnitudes of the three phases are not the same, leading to negative- or zero-sequence symmetrical components [1], [19]. Single-phase loads are the main cause of voltage imbalance on the distribution system. Because the load is supplied directly from the inverter, the power buffer isolates the load from any voltage imbalance on the system.

5.3.5. Waveform distortion

Waveform distortion includes dc offset, harmonics, interharmonics, notching, and noise. Waveform distortion is the result of nonlinear loads on the power system as has been discussed previously in Chapter 2. Again, the dc bus capacitance of the power buffer provides an excellent filter to keep these disturbances from influencing the load. It is interesting to note that it is exactly these types of disturbances that the power factor correction methods of Chapter 2 attempt to remove from the utility system.

5.3.6. Voltage fluctuations

Voltage fluctuations are repeated variations in the system voltage, usually in the range of 90% to 110% of the nominal. They are generally caused by nonlinear loads such as arc furnaces and differ from long-duration variations in that the voltage magnitude varies randomly or at a fixed frequency. As with long-duration variations, the power buffer can successfully protect the load from voltage fluctuations as long as the average voltage magnitude remains large enough to deliver the required power to the load.

5.3.7. Power frequency variations

As the name implies, power frequency variations occur when the system frequency varies from its nominal value. Frequency variations are uncommon on the main utility grid, but can occur in response to large load changes if power is being provided from a local generator. Because the load voltage is controlled entirely by the inverter and can be completely independent of the incoming source voltage, a power buffer can completely isolate the load from any power frequency variations at the source.

6. SYSTEM POWER FACTOR CONTROL WITH THE POWER BUFFER

Up to this point, the operation of the power buffer has been restricted to emulating a purely resistive load, with the displacement power factor of the system as close to unity as possible. This is a highly desirable mode of operation and is almost always the best choice for applying a load to a distribution system with unknown system characteristics. However, the operation of the buffer is not limited to operating at a unity power factor. By altering the control, the displacement power factor can be adjusted to make the buffer's load appear leading or lagging. While this provides no benefit to the load downstream of the buffer, it does allow the buffer to compensate for the system upstream as well and can be useful to the utility. Generally, capacitor banks are added to the system to correct for a low power factor. However, as will be demonstrated, capacitor switching can cause severe transients on the utility system. Adjusting the power factor of the power buffer can improve the overall power factor on the system without having to switch capacitor banks.

6.1. Capacitor Switching

Consider a simple example. A utility has a feeder that supplies two industrial customers. One of the customers has several sensitive nonlinear loads and has decided to use a power buffer to protect its load from transients as well as to correct the power factor to keep its electrical costs down. The second customer has a relatively linear electrical load that includes several electrical machines, giving it a lagging power factor. The machines run only during the day, and the power factor overnight is much closer to unity. A one-line diagram of this system is given in Figure 6.1.

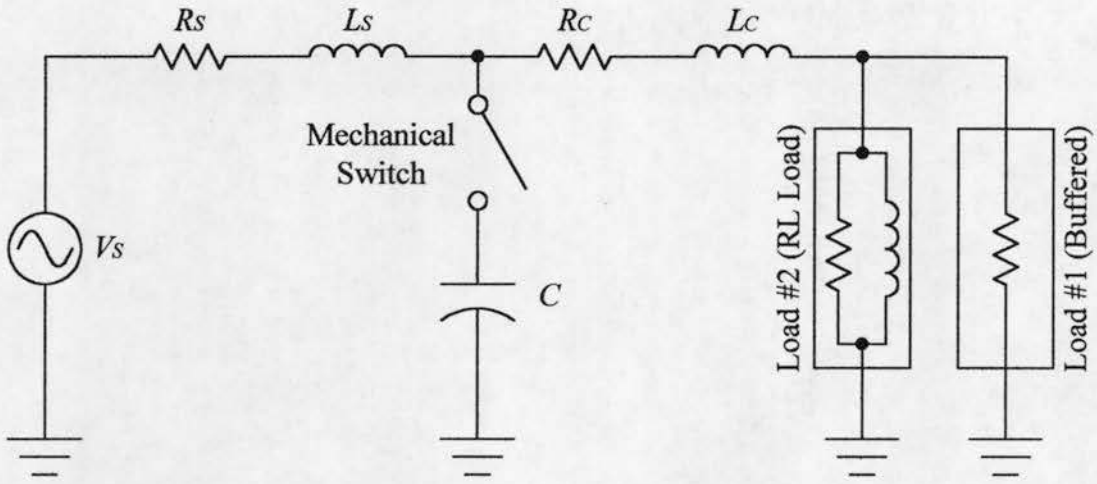

Figure 6.1: Circuit diagram of system with switched capacitor banks.

The loads are at the end of a long feeder, so the distribution source impedance is significant. Because the load of the second user is fairly linear, the normal method of correcting the power factor is to add capacitor banks on the feeder. Because the power factor is significantly different from day to night, the utility switches the capacitor banks in and out of the system as the load changes. The capacitor banks are shown in Figure 6.1 as *C*. The impedance between the capacitor banks and the load is shown as R_C and L_C. The phase-to-phase voltage of the distribution system is 14.4 kV; however, for simulation purposes, all voltages, currents, and impedances are scaled to the 480-V system voltage at which the power buffer operates. The system parameters are given in Table 6.1.

Table 6.1: System parameters of circuit in Figure 6.1.

Parameter	Value
System Voltage	480 V_{rms} phase-to-phase
Source Resistance, R_S	44 mΩ per phase
Source Inductance, L_S	270 μH per phase
Cap.-to-Load Resistance, R_C	4.4 mΩ per phase
Cap.-to-Load Inductance, L_C	27 μH per phase
Capacitance, *C*	1000 μF per phase
Daytime Load, Load #1	115 kW, 1.0 PF (power buffer)
Daytime Load, Load #2	115 kW, 0.8 PF lagging

To correct the power factor to unity, the value of the capacitor bank is chosen to match the impedance of the inductive component of the load at the line frequency. This requires that

$$C = \frac{1}{\omega^2 L} \tag{6.1}$$

With the proper value of capacitance added to the system the power factor can be kept near unity for linear loads. However, capacitor bank switching is not an easy duty for mechanical switches, and can produce significant transients on the system [20]. Generally, the worst transients will occur when a fully discharged capacitor bank is closed into a system at the voltage peak. Under this condition, the line voltage near the capacitor bank will momentarily be forced to zero to match the capacitor voltage. This places the full system voltage across the line impedance creating a current surge. The RLC circuit created by the capacitor bank and the line impedance oscillates until damped out by the system resistance. The results of performing a capacitor switching operation on the system are shown in Figure 6.2.

Notice the voltage dip and the excessive peaks on both the voltage and current traces. The magnitude of the peak transient voltage is typically 1.6 to 1.8 times the nominal peak voltage and can trip the overvoltage protection of electronic drives and controls. These transients result from attempting to force an instantaneous change on the system with the mechanical switch. Figure 6.2 shows that the power factor is changed from lagging to near unity within one cycle.

6.2. Correction of the System Power Factor with the Power Buffer

By taking advantage of the power buffer already present on this system, capacitor switching can be eliminated. By adjusting the power factor of the buffer from purely resistive to leading, the buffer can compensate for the lagging power factor of the second load without adding capacitor banks on the system. Basically, the dc bus capacitance of the power buffer now

supplies the reactive power required to compensate the lagging load. By adjusting the phase angle of the current slowly, the transients shown in Figure 6.2 are eliminated.

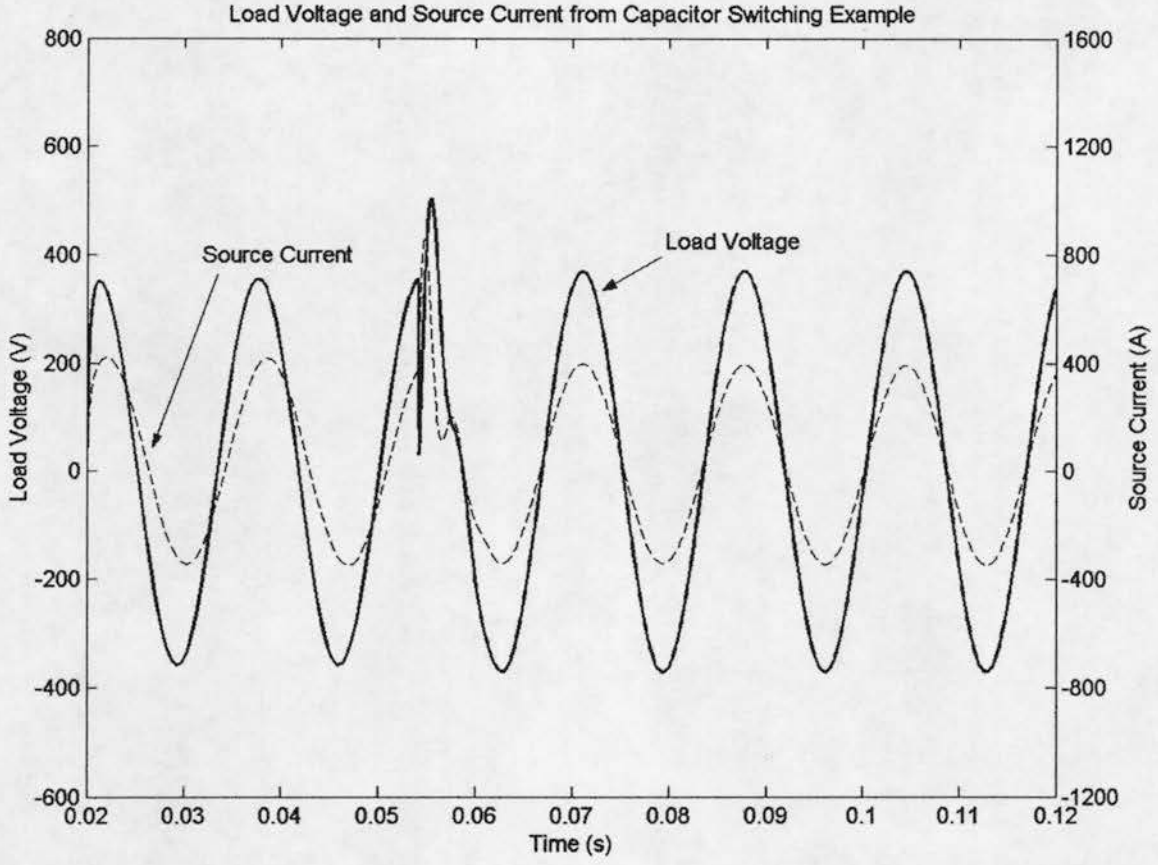

Figure 6.2: System response during capacitor switching for power factor correction.

The main advantage of such a system is that the compensating capacitance is now buffered from the distribution system. This not only removes the problem of switching transients as the power factor is corrected, but it also isolates the capacitor banks from the distribution system at all times, keeping them from contributing to transient oscillations as other switching takes place on the system. Figure 6.3 shows the waveforms for the system with the power buffer operating with a unity power factor. For clarity, only the A-phase voltage and currents are shown. Notice that the overall source current is lagging, while the current of Load #1 is in phase with the source voltage.

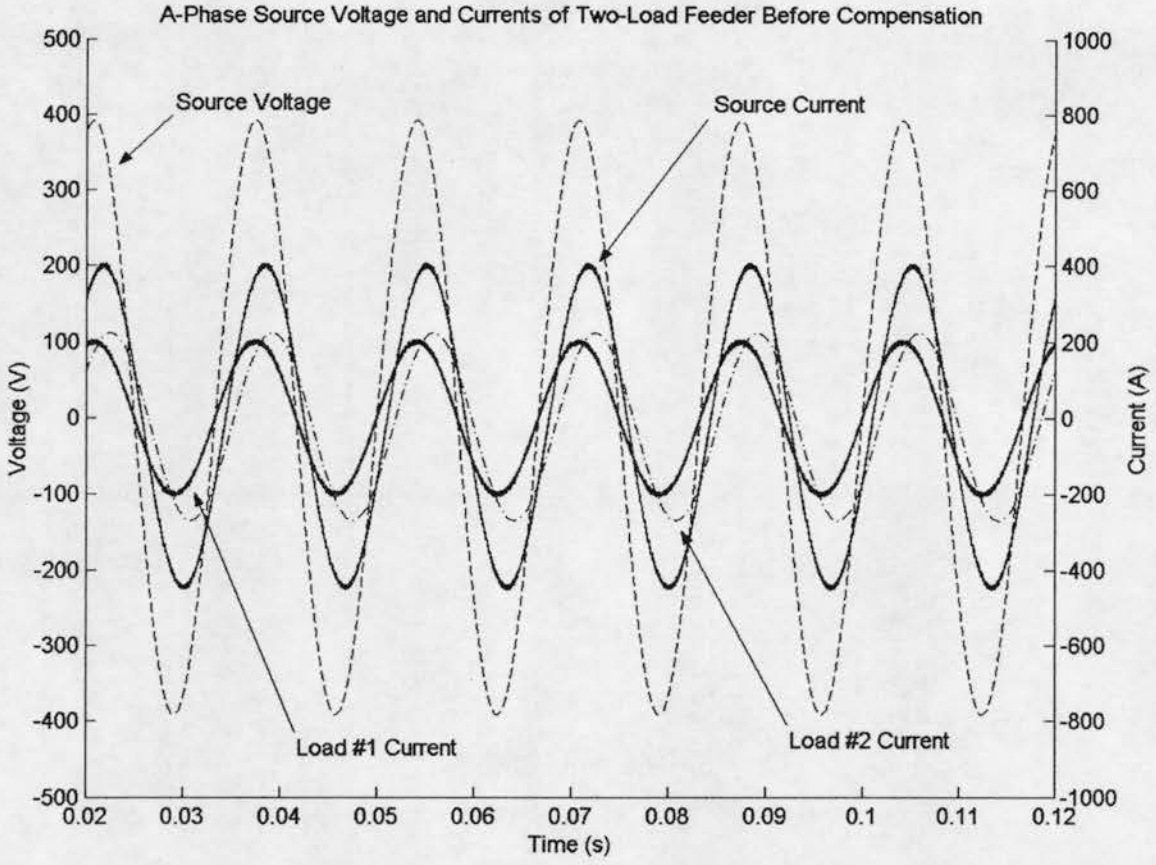

Figure 6.3: Response of system with power buffer operating at unity power factor.

Figure 6.4 shows the waveforms with the power buffer operating with a 37° leading current. The source current is in-phase with the voltage, creating a unity power factor for the system. However, changing the buffer's power factor away from unity increases the input current because the real power of the buffer's load is the same. Altering the power factor adds a reactive power component that increases the apparent power, and hence the current. To correct the system power factor to unity, the magnitude of the reactive power Q supplied by the buffer must equal the magnitude of the reactive power Q_S on the system. The system reactive power can be found from the real power P_S and the power factor PF_S of the system outside of the buffer as follows:

$$Q_S = P_S \sqrt{\frac{1}{(PF_S)^2} - 1} \tag{6.2}$$

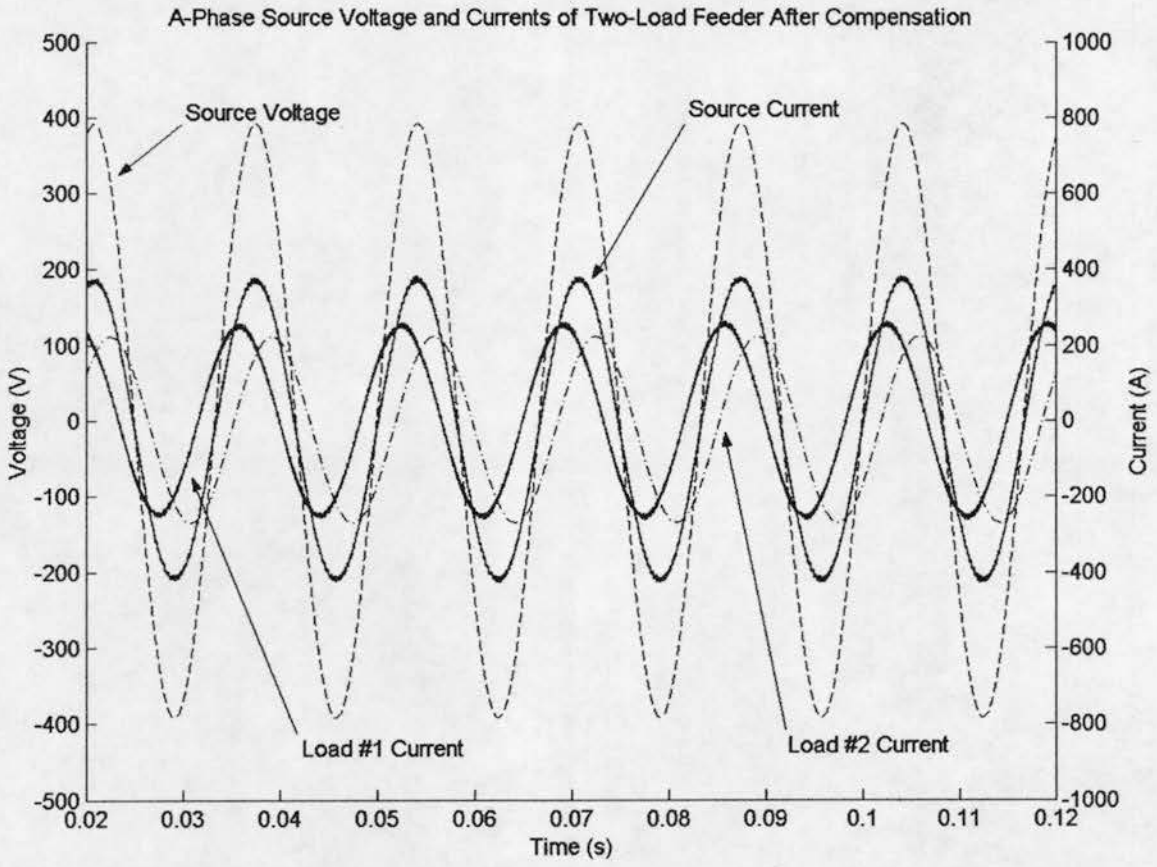

Figure 6.4: Response of system with power buffer correcting system power factor.

Using $Q = -Q_S$ and the real power P of the buffer, the required power factor angle θ of the power buffer is

$$\theta = \arctan\left(\frac{Q}{P}\right) \tag{6.3}$$

and the required current draw of the buffer expressed as a percentage of the current draw for the unity power factor case is

$$\text{current ratio} = \sqrt{1+\left(\frac{Q}{P}\right)^2} \times 100\% \tag{6.4}$$

Table 6.2 shows the current required at the input of the power buffer for a variety of power factor angles, compared to the unity power factor current.

Table 6.2: Power buffer current required for reactive power compared to the resistive case.

θ	Input Current Percentage
0°	100.0%
5°	100.3%
10°	101.5%
15°	103.5%
20°	106.4%
25°	110.3%
30°	115.5%
35°	122.1%
40°	130.5%
45°	141.4%
50°	155.6%
55°	174.3%
60°	200.0%

For the power buffer to be able to operate with a nonzero power factor angle at its input, the system components will need to be able to handle the increase in current. From Table 6.2, it is clear that for small angle changes, the current increase is minimal. However, for a 60° change, the input current doubles, and the current increases rapidly for higher angles.

7. CONCLUSION

As nonlinear loads continue to propagate on the utility system, power quality will continue to be a major concern for both utilities and power users. Fortunately, as the cost of high-power electronic switches continues to decrease, power electronic techniques can be used to create solutions to some of these power quality issues.

Power factor correction is a useful tool to prevent nonlinear loads from adversely affecting the distribution system and other the power users on it. It can be implemented as a front end to the power supplies of individual components, as well as in the form of a power buffer to protect multiple loads. When used properly, power factor correction can drastically reduce the harmonics generated on the distribution system.

However, as power factor correction becomes the norm, stability issues on the distribution system will become more of a concern. As discussed, PFC rectifiers behave as constant power loads, presenting negative incremental impedance to the source. The interaction of these constant power loads with the impedance of the distribution system can create stability problems. However, if additional energy storage is provided in the form of capacitance, the rectifier control can adjust its incremental input impedance as required to keep the system stable.

Additional energy storage also allows a power buffer to provide some limited protection to the load from disturbances on the distribution system. While it lacks the energy storage of a complete UPS system, the switching elements are identical to that of an in-line UPS, allowing the buffer to protect the load from short interruptions and low-magnitude sags and swells.

Single-phase PFC rectifiers are now becoming common as replacements for classical rectifiers, with integrated circuits available to control the required switching functions. The costs

of the semiconductor switches required for an off-line power supply on a 120-V system make such systems practical.

However, outside of high-voltage dc transmission, the use of power electronics for high-power applications on the utility system has been limited due the associated costs. Only users with very sensitive loads, or processes that incur high costs if interrupted, have been willing to pursue the benefits that can be gained by using power electronic solutions. However, as more users require better power quality and the costs associated with the required systems decrease, power electronic applications on the distribution system should become more widespread.

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