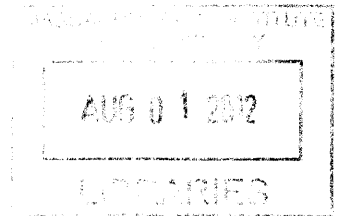


Low Cost Analog Signal Processing for Massive Radio Telescope Arrays

ARCHIVES

by

Eben A. Kunz



S.B., E.E.C.S., Massachusetts Institute of Technology (2010)

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

January, 2012

© 2012 Massachusetts Institute of Technology

All rights reserved.

Author

A handwritten signature in black ink, appearing to read "Eben A. Kunz", written over a horizontal line.

Department of Electrical Engineering and Computer Science

January 27, 2012

Certified by

A handwritten signature in black ink, appearing to read "Max Tegmark", written over a horizontal line.

Prof. Max Tegmark

Thesis Supervisor

Accepted by

A handwritten signature in black ink, appearing to read "Dennis M. Freeman", written over a horizontal line.

Prof. Dennis M. Freeman

Chairman, Masters of Engineering Thesis Committee

Low Cost Analog Signal Processing for Massive Radio Telescope Arrays

by

Eben A. Kunz

Submitted to the Department of Electrical Engineering and Computer Science

January 27, 2012

In Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering and Computer Science

Abstract

Measurement and analysis of redshifted 21cm hydrogen emissions is a developing technique for studying the early universe. The primary time of interest corresponds to a signal in the the 100-200MHz frequency band. The Omniscoppe is a new type of radio telescope array being developed at MIT which images the entire sky in this band at low resolution using spatial Fourier transforms. In order to gain the maximum benefit from this type of telescope, a regular array of more than 10,000 antennas will eventually be necessary. I detail a low cost analog signal path which was developed to test and refine the signal processing and imaging pathways of the Omniscoppe. This signal path begins at the output of a preexisting antenna design and ends with digitization.

Thesis Supervisor: Max Tegmark

Title: Professor, MIT Department of Physics

Acknowledgments

I would like to thank everyone who worked with, around, and despite me on the Omniscope in the last two years: Kris Zarb Adami and Jack Hickish for getting me off on the right foot in Oxford. Ashley Perko for seeking out and battling Omniscope evils. Hrant Gharibyan and Katelin Schutz for being good minions. Adrian Liu for teaching me what the Omniscope is really supposed to measure. Jon Losh and Nevada Sanchez for forwarding the cause of electrical engineers and being sounding boards. Andy Lutomirski for being Andy. Jeff Zheng for carrying the torch. Thanks to Adam Baird for teaching me that reality is just an illusion, Jean Papagianopoulos for helping me buy lots of shiny things, and of course Max Tegmark for giving me an opportunity to learn RF design and make lots of things that work.

For the record, I'd also like to thank all of the professors, TAs, LAs, staff, and fellow students who made my MIT education what it was. Thanks also to Sheri Ann Cheng for putting up with me all these years, to my parents for putting up with me for even longer.

Contents

1	Introduction	8
2	System Design	11
2.1	Starting Point	11
2.1.1	Signal Gain	11
2.1.2	Crosstalk	11
2.1.3	Group Delay	12
2.1.4	Signal Band	12
2.1.5	Antenna	12
2.1.6	Digitization and Processing	13
2.2	Hardware Scaling and Distances	14
2.2.1	Asymptotic Scaling	14
2.2.2	Cable Types	14
2.2.3	Power Distribution	14
2.3	Demodulation	15
2.4	Devices	15
2.4.1	Line Driver	15
2.4.2	Receiver	15
2.4.3	Swapper	16
2.4.4	Analog Chain Overview	16
2.5	Software	16
3	Line Driver Design	16
3.1	Hardware	17
3.1.1	PCB Selection	17
3.1.2	Enclosure	18
3.2	Passive Elements	18
3.2.1	Coupling Capacitors	18
3.2.2	Power Filter	18
3.2.3	Notch Filter	19
3.2.4	RF Choke	20
3.2.5	Impedance Matching	20
3.3	Active Elements	20
3.3.1	Amplification	20
3.3.2	Noise Figure	20
3.3.3	Power Regulation	21
3.4	Final Design	21
3.4.1	System Diagram	21
3.4.2	Appearance	22
3.4.3	Usage Specifications	22
4	Receiver Design	22
4.1	Signal Chain	22
4.1.1	Clock Splitter	22
4.1.2	Bandpass Filter	23
4.1.3	Attenuator	23
4.1.4	Amplification	23
4.1.5	IQ Demodulator	23
4.1.6	Differential Impedance	24
4.1.7	Low Pass Filters	24
4.2	Final Design	25
4.2.1	Overview	25
4.2.2	Appearance	25

4.2.3	Usage	25
5	Swapper Design	26
5.1	Structure	26
5.1.1	Swapper Driver	26
5.1.2	Shift Registers	27
5.2	Details	28
5.2.1	Controller Power Supply	28
5.2.2	Transceiver to Controller Connection	28
5.2.3	ROACH to Transceiver Connection	28
5.2.4	Timing	28
5.2.5	IQ Channel Selection	29
5.3	Final Design	29
5.3.1	System Diagram	29
5.3.2	Appearance	30
5.3.3	Usage	30
6	Hardware Performance	30
6.1	Line Driver v5.0 (Notch Filter)	31
6.2	Receiver v2.0	33
6.3	Swapper v1.0	34
7	Clock Distribution	35
7.1	ADC/ROACH Clock	35
7.2	2xLO Clock (IQ Demodulator)	36
8	Conclusion	36
8.1	Performance	36
8.2	Cost	37
8.3	Deployment	37
A	Background Knowledge	39
A.1	TEM Impedance	39
B	Schematics and PCBs	41
B.1	Line Driver v5.0 Schematic	41
B.2	Line Driver v5.0 PCB	42
B.3	Receiver v2.0 Schematic	43
B.4	Receiver v2.0 PCB	48
B.5	Schematic v1.0 Schematic	49
B.6	Swapper v1.0 PCB	53

List of Figures

1	The Universe Over Time[17]	8
2	Omniscope Architecture	9
3	Omniscope Digital Architecture	10
4	The Omniscope in Greenbank, West Virginia	11
5	2753 Bandpass Filter, S21, 100-200MHz	12
6	MWA Antenna LNA, S21, 2-2000MHz	13
7	System Diagram	16
8	Line Driver Power Filter, S21	19
9	Line Driver Notch Filter, S21	20
10	Line Driver System	21
11	Line Driver v5	22
12	Receiver LO Splitter, S21	23
13	Receiver Output Filter S21	24
14	Receiver System	25
15	Receiver v2.0	25
16	Swapper Signal Path	26
17	Swapper Driver	27
18	Swapper Data Path	27
19	Swapper System	29
20	Swapper Controller	29
21	Swapper Transceiver v1.0	30
22	Swapper Controller v1.0	30
23	Line Driver v5.0, S Parameters, 50-200MHz	31
24	Line Driver v5.0, Group Delay, 50-200MHz	31
25	Line Driver v5.0, S Parameters, 2-2000MHz	32
26	Line Driver v5.0, Power S21, 2-2000MHz	32
27	Receiver v2.0, S21, 150MHz LO	33
28	KR 2753 Bandpass Filter, Group Delay, 50-200MHz	33
29	KR 2999 Low Pass Filter, Group Delay, 1-50MHz	33
30	Receiver v2.0, Power S21, 2-200MHz	34
31	Swapper v1.0, Transitions	34
32	Swapper v1.0, Power S21, 20200MHz	35
33	West Forks Array Deployment	37
34	TEM Impedance Mismatch Power	40
35	Line Driver v5, Schematic	41
36	Line Driver v5, PCB	42
37	Receiver v2.0, Schematic 1 of 5	43
38	Receiver v2.0, Schematic 2 of 5	44
39	Receiver v2.0, Schematic 3 of 5	45
40	Receiver v2.0, Schematic 4 of 5	46
41	Receiver v2.0, Schematic 5 of 5	47
42	Receiver v2.0, PCB (Top/Bottom)	48
43	Swapper Transceiver v1.0, Schematic	49
44	Swapper Controller v1.0, Schematic, Logic	50
45	Swapper Controller v1.0, Schematic, Power Supply	51
46	Swapper Controller v1.0, Schematic, Driver	52
47	Swapper Transceiver v1.0, PCB (Top/Bottom)	53
48	Swapper Controller v1.0, PCB (Top/Bottom)	54

1 Introduction

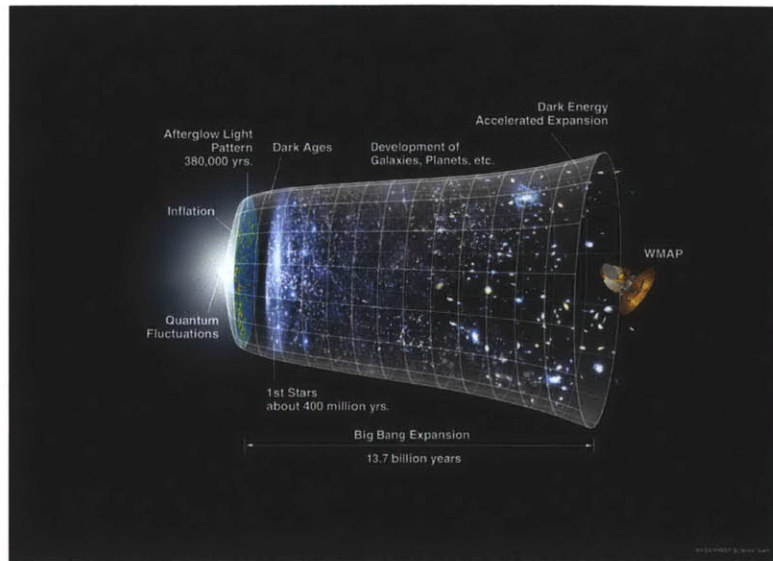


Figure 1: The Universe Over Time[17]

In order to study the development of the universe, astrophysicists would like to measure the universe at each point in time from the Big Bang until the present. Prior to the first 400,000 years after the Big Bang, the universe consisted of plasma. While plasma radiates plenty of energy, it also reabsorbs energy, so nothing about the structure of the universe was transmitted forward in time. As the universe cooled the plasma coalesced into atoms, especially neutral hydrogen. Radiation from the last of the plasma could then propagate through the universe without being reabsorbed. This plasma radiation, called the cosmic microwave background (CMB), is the focus of NASA's WMAP[17], which has created maps of the universe during the recombination of plasma into atoms.

After atoms formed, it was 400 million years before those atoms began to coalesce into stars. The period of time between the formation of atoms and the formation of stars is called the Epoch of Reionization. At the start of the EoR, the universe was comprised of neutral hydrogen, which only radiates when its electrons change spin states, corresponding to a 21cm wavelength (1.4GHz). As the universe expands, existing radiation is observed at lower frequencies due to the Doppler effect (redshifting), so older 21cm radiation has a larger wavelength. Examining different frequencies is therefore equivalent to looking at different periods in the development of the universe. It is the the goal of this thesis to further the study of the EoR by constructing components of the Omniscope radio telescope.

The Omniscope is a new type of radio telescope array being developed to study the EoR by mapping the entire sky[22]. The general method is to observe several different frequencies simultaneously with many antennas, then use all the data from each individual frequency to construct a map of the sky at a different point in time. The Omniscope is unique because it organizes antennas into regular grids, and then exploits that regularity by using Fast Fourier Transforms to correlate N antennas with $O(N \log N)$ cost. Low asymptotic cost is critical for scaling to large numbers of antennas, which are required for good accuracy.

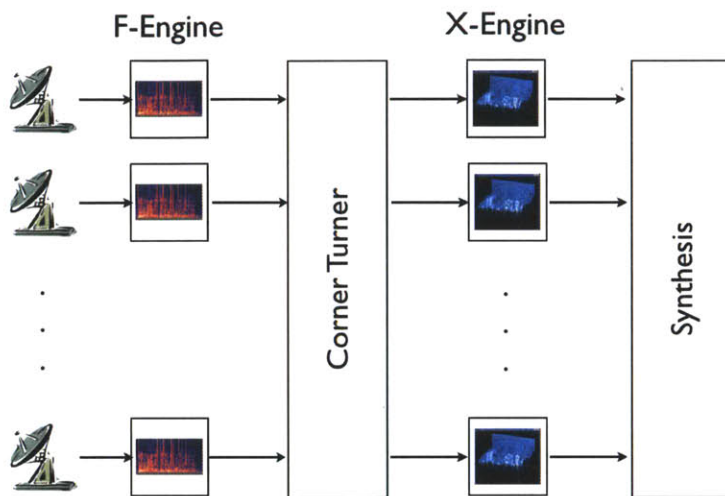


Figure 2: Omniscope Architecture

Each antenna’s signal is first sent to an F-Engine, which performs a temporal FFT on it, thus separating the signal into different frequencies. The resulting frequency bins are redistributed by a Corner Turner so that all of the bins for any given frequency are sent to a single X-Engine. The X-Engine performs a spatial FFT on the bins from a single frequency, and from that a sky map of the EoR at a particular time can be generated. The Corner Turner hardware has $O(N \log N)$ cost, since it must be able to distribute bins between each F-X pair. The X-Engine has the same cost since it must FFT the bins from each of N antennas. In order to properly form a sky map of the EoR, other radiation from later in the universe, called foreground radiation, must be removed from the map. Removing foreground radiation is also an important aspect of the Omniscope[13, 14].

The current iteration of the Omniscope will have 4 F-Engines and 4 X-Engines. Each F- and X-Engine can handle multiple antennas and multiple frequencies, respectively. Due to the hardware used, this is the largest architecture where the Corner Turner can be implemented with wires instead of dedicated hardware, which has yet to be developed. Andrew Lutomirski[15], Ashley Perko[19], and Nevada Sanchez[21], have already completed theses related to the Omniscope hardware, which should be consulted for more thorough coverage of some topics.

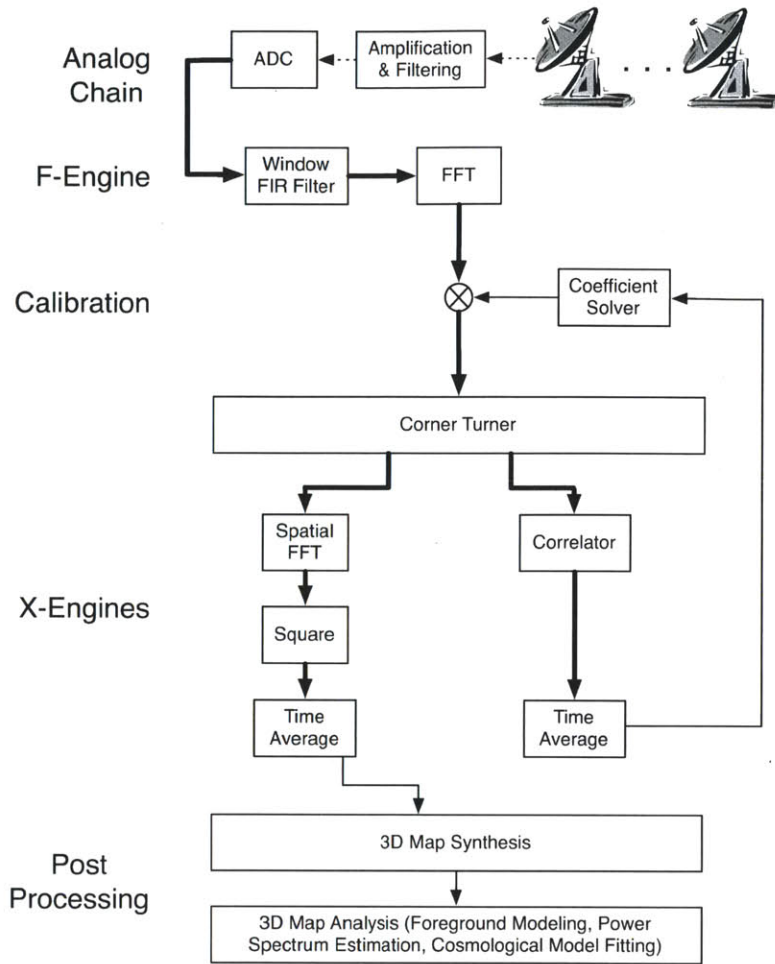


Figure 3: Omniscopie Digital Architecture

The Omniscopie is capable of calibrating itself to correct for phase errors between antenna signals. Each antenna signal is digitized with exactly the same clock frequency, but is assumed to have some phase error relative to other signals, such as from different length cables. The correlation between signals is used to analyze phase error by examining known sources, such as the sun, and providing a phase adjustment to each digitized signal on a per-frequency basis. This makes life much easier when designing analog components. As long as phase error does not change suddenly, it can vary between antenna signals with no penalty. Accepting a fixed phase error means more design choices can be made in favor of reduced cost and complexity instead of favoring phase accuracy.



Figure 4: The Omniscope in Greenbank, West Virginia

Prototypes of the Omniscope have been deployed in Greenbank, West Virginia and West Forks, Maine to test the architecture as it is being developed. Finding locations on the East Coast of the USA which do not have too much RF interference is a challenge. West Forks, Maine is the closest to MIT that the Omniscope has been successfully operated.

2 System Design

The goal of this thesis is to help create a 128 polarization (128p) Omniscope by developing, building, and characterizing an appropriate analog processing chain. Most of the hardware for the 128p Omniscope has been built, tested, and mass produced by now (January 2012), and the rest is currently in the works. This system is not intended to be directly scaled up to more than 128 polarizations, and there are undoubtedly more lessons to be learned before designing a larger array. Instead, this system is a prototype for future arrays, as well as a test bed for developing the current digital processing elements of the Omniscope.

2.1 Starting Point

2.1.1 Signal Gain

In order to detect the EoR, the analog chain must amplify the incoming signal enough that it can be digitized and provide good data. At the same time, it can't amplify so much that foreground signals saturate circuits in the analog chain. Too much signal power will ultimately result in a square wave along the analog chain, since signals are limited by the voltage which powers any active circuits. Varying degrees of this condition are called saturation, and result in the loss of any signal information except the saturating frequency. The original estimate was that 100dB would be sufficient gain between the antenna and digitization. Variable attenuation is necessary for test deployments in areas with high foreground noise, especially places with nearby broadcast radio stations, in order to avoid saturation.

2.1.2 Crosstalk

Crosstalk is when a signal radiates into the processing chain of another signal. In a linear system, crosstalk is bilateral. The two signals are mixed, which results in lost precision for both. Because signals in the Omniscope are averaged after digitization, they can theoretically provide more information than the accuracy of the digitization hardware, so the accuracy of the ADC is not necessarily related to a minimum crosstalk threshold. Crosstalk was prevented as much as possible, but ultimately extreme measures were necessary to counteract crosstalk.

2.1.3 Group Delay

Group delay, which is a measure of how different frequencies propagate at different speeds, should be as flat as possible. Flat group delay is equivalent to signals propagating at the same speed through the system, and is better for signal analysis when considering clock jitter and FFT spectral leakage. A group delay which varies wildly means that a slight change in a signal's frequency would result in a significant phase jump. There is no specific criteria for group delay, so the system is measured where possible to make sure group delay seems reasonable.

2.1.4 Signal Band

The signal band is the range of scientifically interesting frequencies which the Omniscope is intended to analyze. It is most significantly defined by filters which are used to eliminate signals at uninteresting frequencies. The amount of signal power a circuit can output is limited by total signal power across all frequencies it responds to. Reducing uninteresting signal power is important because it allows any given amplifier in the analog chain to output the interesting signals with more power, thus providing more information for digitization and analysis.

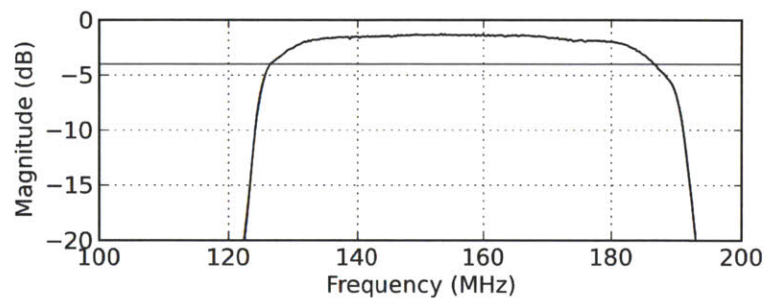


Figure 5: 2753 Bandpass Filter, S21, 100-200MHz

In the Omniscope, use of the KR Electronics model 2753 bandpass filter was borrowed from the Berkeley PAPER telescope[24], and represents the current area of interest for the EoR. The 2753 has a 55MHz bandwidth, a center frequency of 157.5MHz, and attenuation of at least 60dB out of band[11]. When measured, the filter has an insertion loss of 1dB, and a 3dB bandwidth of 126-186MHz. The system is designed with 125-185MHz in mind, which is a slight adjustment to account for the asymmetry of the bandpass characteristics.

While astronomical foreground radiation is a significant concern for digital signal processing, the analog chain has bigger problems. In the USA, FM broadcast radio stations operate in the 88.1-107.9MHz range (“FM band”). Near MIT, for example, WBMX has a license to broadcast 21kW at 104.1MHz from one of Boston’s tallest buildings[7]. The antenna for WBMX is clearly visible from the lab where the Omniscope is currently being constructed, and can result in a -70dBm signal within a 2m long terminated SMA cable. That amount of power is enough so lab analysis is nearly impossible for some components. For deploying the telescope within the USA, additional filtering of the FM band is necessary to avoid saturating early gain stages before digital foreground correction can even occur.

Originally the analog chain was intended to operate up to approximately 1GHz so it could be used with different antennas for other areas of astronomical study. As the drawbacks of this level of flexibility became apparent, some wide band features were left in place to avoid redesign, even though other elements are based on the 125-185MHz band. Wide band features are evident in the design, and associated drawbacks are mentioned so they may be avoided or accounted for in the future.

2.1.5 Antenna

The antenna used in the Omniscope was developed for the Murchison Widefield Array[1], which is a similar telescope that uses analog rather than digital beam forming. The MWA antenna is inexpensive and the band of interest is identical,

so reuse of the design is appropriate. Each antenna has two polarizations which are rotated by 90° from each other. The antenna was designed for a response of 100-300 MHz, and has an attached low noise amplifier (LNA) with 20dB of gain. The noise figure of the amplifier is 0.2dB, and the 20dB of gain means that following gain stages will not contribute significantly to the noise figure. The antenna is powered by a 5VDC bias at 100mA on the signal output port.

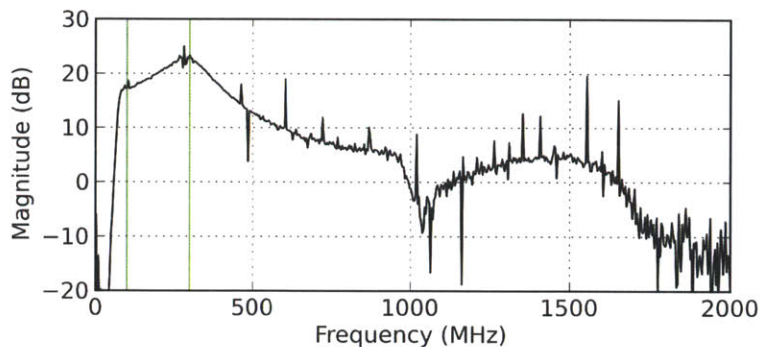


Figure 6: MWA Antenna LNA, S21, 2-2000MHz

The response of the LNA only tapers off gradually above 300MHz, so in cases where excess signal power is a factor, extra low pass filtering may be necessary shortly after the LNA. The figure shown was generated by connecting the LNA inputs directly to a VNA via a 1:1 transformer, and makes no correction for antenna/LNA impedance, which is not known. Despite these limitations, it should be clear that LNA response is still significant at frequencies above 300MHz, which must be taken into account. Ashley Perko has done some analysis of MWA antenna/LNA behavior, including saturation effects[19].

2.1.6 Digitization and Processing

Each F- and X-Engine is a ROACH (Reconfigurable Open Architecture Computing Hardware) FPGA board designed by the CASPER group at UC Berkeley[23]. The current generation of ROACH board uses Xilinx Virtex 5 FPGAs, and has a pair of Z-DOK differential digital connectors for peripherals, especially ADCs. Each Z-DOK connector has 40 differential pairs operated at 600Mbps. The array uses an ADC board with 64 single ended 50Msps inputs, which was designed by Rick Raffanti for CASPER. These ADC boards are the only model available for the ROACH with sufficient inputs for a massive array. Each ADC board occupies both Z-DOK connectors of a single ROACH, and has 8 Analog Devices ADS5272 ADCs[3], which are 12-bit ADCs. 64 Z-DOK pairs are used for data, and 16 are used for ADC output clocks (1x and 6x sample clock per ADC chip). The clock which drives the ADC is either generated by the ADC board itself or driven into a 0.1" header on the side of the board.

Signals enter the ADC through a Samtec 80 conductor QSE series port[20]. Each conductor is 50Ω single ended, and is converted to a differential signal via transformer for the ADC. The associated Samtec cables (EQR series) are intended to be digital cables, and require a converter to individual SMA cables so that signals can originate from multiple separate PCBs. A maximum input power of approximately 12dBm can be driven into the ADC via the SMA adapter cable. Based on the ADC specifications, this is 10dB of power at the ADC with 2dB of cable and circuit losses. There is a phase imbalance between the SMA input and the ADC, which has been observed to be up to 2.5° at 10MHz. Measurement and digital adjustment is necessary if exact phase is needed between ADC channels.

The current digital architecture requires that all ADCs be clocked by the same source. The ADC clock input could be driven from the ROACH with some minor adaptation. Ideally the ADCs will be clocked from a common ROACH clock which is then sent to the ADCs. It is not known at this time whether it is feasible for the ROACH to redistribute a clock signal, mostly due to limitations in the ROACH programming tool chain.

Because the ADCs are tied to the digital processing system, which must be tightly interconnected, analog signals must converge at a single digital processing hub somewhere within or near the antenna array. As such, accurately transmitting signals from the antenna array to the processing hub is an important factor of this system.

2.2 Hardware Scaling and Distances

2.2.1 Asymptotic Scaling

If all the hardware works, the logistics and cost of deploying a massive array become the next dominant design consideration. Although economies of scale relating to manufacturing are not achieved at 128 polarizations, the design should be appropriate for low cost at larger scales. Quantity of hardware scales as $O(n)$ for antennas and most signal processing hardware, and $O(n \log n)$ for corner turner hardware[22, 15, 21]. Total cable length between a grid of antennas and a central point, however, scales as $O(n^{3/2})$. Cable length is approximated as a square array of continuous “antenna”, as well as calculated discretely to confirm the approximation for low quantities, assuming antennas connect to a point at the center of the array. For an array with spacing d and total number of elements n , total cable length L to a central point is approximated by starting with $1/8$ of a square in polar notation:

$$L_A = 8 \cdot \int_{\theta=0}^{\pi/4} \int_{r=0}^{(d\sqrt{n}/2)/\cos\theta} r^2 dr d\theta \quad \text{continuous “antenna”}$$

$$L_A = 8 \cdot \frac{(d\sqrt{n}/2)^3}{3} \int_{\theta=0}^{\pi/4} \frac{1}{\cos^3\theta} d\theta$$

$$L_A = 8 \cdot \frac{(d\sqrt{n}/2)^3}{3} \cdot \left(\frac{1}{\sqrt{2}} + \frac{1}{2} \ln(1 + \sqrt{2}) \right) \quad \text{or} \quad L_A = O(n^{3/2})$$

$$L_C = 4 \cdot \sum_{i=0}^{\sqrt{n}/2} \sum_{j=0}^{\sqrt{n}/2} d \cdot \sqrt{(i+0.5)^2 + (j+0.5)^2} \quad \text{discrete antennas}$$

With spacing of $d = 2m$, the minimum total cable length is $L_C = 25km$ for $n = 1024$, and $L_C \approx 1600km$ for $n = 16384$. Realistically, cables converge at the side of the array, and must travel some distance away to prevent interference between antennas and digital equipment, so the amount of cable would actually be greater. The system should work with the smallest number of cables of the least expensive variety between antenna and processing hub. For massive arrays, some of this cost can be mitigated by digitizing and aggregating antenna data at local nodes before reaching the processing hub, which reduces cabling at the cost of potential synchronization effort. For unaggregated arrays, cables should not be equal length to avoid cable length scaling as $O(n^2)$.

2.2.2 Cable Types

Finding the least expensive sufficient cable is important due to cable length scaling. Unlike scientific 50Ω cable, 75Ω RG6 cable is used in cable TV installations throughout the US. It is available inexpensively in mass quantities (\$60/1000ft unterminated), has good frequency response, and is commonly weatherized for long term exposure. The only disadvantage is that many RF ICs are designed with 50Ω ports, so impedance conversion is necessary when connecting to standard RF circuitry.

2.2.3 Power Distribution

As antenna cable length scales with array size, so do the resistive losses of sending power to antennas and other elements located within the array. Using moderately high DC or AC voltage for any long distance power transfers reduces power consumption, or alternatively reduces necessary conductor size for a given amount of loss. The tradeoff is that additional conversion hardware at one or both ends of the cable is necessary, since none of the RF hardware should handle high voltage. The simplest and least expensive method for meeting these requirements is to send 120/240VAC line voltage as far as possible, then use commercially available high efficiency AC/DC converters as necessary to provide appropriate low DC voltage close to where it is needed. Standard 100 foot extension cords are relatively inexpensive and can be left outdoors safely. Filtering will be required to remove conversion noise, but filters will already be in place for other sources of noise.

6VDC supplies are used as much as possible in order to simplify the construction and use of the system. This voltage leaves enough head space to use a low dropout 5V linear regulator for 5V components. Negative voltages are generated by designing switching supplies into devices rather than requiring additional or customized power supplies. While this may increase device costs, the external simplicity will greatly benefit lab use and small scale testing deployments.

Maintaining a connection to earth ground in as many places as possible is important for avoiding trouble with the antenna array. Although the signal pathways will be capacitively decoupled enough that there should be no unintended DC current, additional earth ground connections will help attenuate interference picked up on the ground plane.

2.3 Demodulation

Demodulation in this case means to move some part of the signal band to a different frequency where it is easier to digitize with an ADC. The Omniscope has 50Msps ADCs, so moving some amount of the signal to below 25MHz would allow it to be sampled most easily. The Omniscope uses IQ demodulation to convert signal from 125-185 MHz to below 25 MHz[15, 21]. The tradeoff is that two ADC channels are required per polarization, but the analysis bandwidth is doubled. IQ demodulation requires only a single LO (Local Oscillator), and the filtering requirements are more lenient than for up/down conversion. Because of the transformers and filter roll off, the final available bandwidth is approximately 40MHz around the LO frequency with a 1MHz gap in the center.

The alternatives to IQ demodulation are direct sampling, under sampling, and up/down conversion. Direct sampling would require 400Msps ADCs and eliminating unnecessary frequency bins after the FFT. Each ADC would be much more expensive and require more digital bandwidth, which would use expensive ROACH resources. Under sampling would require extremely tight filters and a fixed bandwidth, which is not flexible enough for the Omniscope's signal band. Up/down conversion would convert the signal band up to filter one end of the band, then down to the ADC range for the other end. This requires a steep high frequency filter as well as two LO signals instead of one. While up/down conversion is a viable alternative, the hardware infrastructure is simpler with IQ demodulation.

2.4 Devices

When designing the components of this system, using purchased ICs and filters was preferred in order to focus on system design and construction. In some cases, amplifiers for example, the cost of the IC is less than the cost of enough discrete transistors to implement even a rough approximation of the same functionality. Less expensive filters can be made from discrete components, but the characteristics of purchased modules are much better due to custom inductors and shielding.

Specific device designs are given version numbers. Not all version numbers were created or prototyped, and only the most recent hardware versions are described here.

2.4.1 Line Driver

Line Drivers amplify a single antenna's signal while powering that antenna's LNA. Line Drivers only handle a single signal to reduce potential crosstalk from sharing a PCB. They are placed near the antenna in order to reduce resistive losses from powering the antenna at low voltage. Additional gain early in the analog chain helps the signal overpower any noise picked up along the way to the processing hub, and maintains the low noise figure set up by the LNA.

2.4.2 Receiver

Receivers take input from several Line Drivers, filter the incoming signals, adjust the power level, and demodulate. The resulting signals go directly to an ADC. Receivers are placed near the ADC/ROACH to which they are connected to reduce cabling for LO distribution and ADC connection. Multiple signals are handled on each receiver, which is designed to fit into a 6"4U high equipment rack. While a single-signal receiver would be ideal, some aggregation is necessary to make managing hardware feasible.

2.4.3 Swapper

After the Line Driver and Receiver were well into production, it became apparent during testing that crosstalk within the ADC and cabling would significantly affect signal quality. Analysis is ongoing, but approximately -40dB of crosstalk can be expected between nearby channels. The solution is to cancel out crosstalk during time averaging of FFT results by selectively inverting analog signals[15, 21]. Each signal is inverted 50% of the time relative to all other signals, and re-inverted after digitization. Any first order crosstalk is eliminated in this way. The ideal position for the analog signal inversion is immediately after the antenna, in order to cancel as much crosstalk as possible. A purchased inversion module is used, so the bulk of the work is enabling a ROACH to drive the purchased modules. This aspect of the Omniscope is referred to as the Swapper system.

2.4.4 Analog Chain Overview

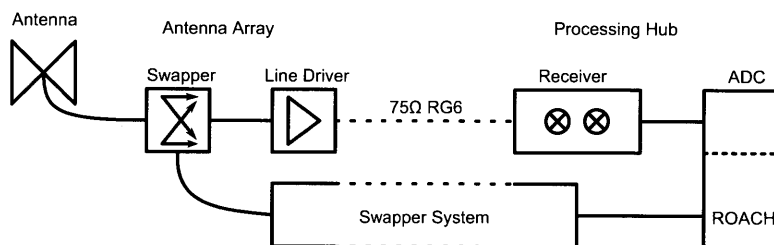


Figure 7: System Diagram

2.5 Software

Software has been selected for low cost (free) and suitability. While many complex and otherwise expensive software packages are available at MIT for very little money, this may not be true at other institutions who may collaborate or benefit from these designs. In addition, if small changes need to be made, or if new hardware is needed after a long delay, free software is easier to acquire on a short term basis.

- FreePCB: PCB Layout. Better than Eagle for tiling (repeat and combining designs), which is critical for cheap prototypes.
- TinyCAD: Schematic capture. Compatible with FreePCB. Stores and exports BOMs reasonably well.
- LTSpice: Circuit simulation. Good for simulating Linear Technology power conversion parts.
- Microwave Office: Circuit simulation. Good for filter design and component selection. Requires an educational license.
- Python / NumPy / SciPy: Calculation. Personally preferred over MATLAB due to open source nature.
- Lyx: Text layout. Used for this document.
- Inkscape: Vector graphics.

3 Line Driver Design

The line driver input must have a 50Ω SMA input port for the antenna, and must provide 5VDC at 100mA to power the antenna's LNA. The output port must be a 75Ω F-type jack for compatibility with RG6 cable. It should provide 40-60dB of gain in the 125-185MHz band. The line driver must be resistant to interference from power supply noise, as well as filter high powered input signals in the USA FM band of 88.1-107.9MHz.

3.1 Hardware

3.1.1 PCB Selection

Many exotic PCB types are available for high frequency design, with associated high costs. The Omniscope does not operate at high enough frequency to justify anything more than a standard FR4 fiberglass and epoxy PCB. FR4 is the easiest and cheapest option for prototyping and low cost hardware, and can be expected to work reasonably up to at least 1GHz.

Layer	Thickness (mil)
Top Copper	1.4
PrePreg	9.8
Inner Copper 1	1.4
Core	40
Inner Copper 2	1.4
PrePreg	9.8
Bottom Copper	1.4

Table 1: PCB Stack Up

A 4 layer 62mil PCB with FR4 substrate and 1oz copper is used since it is a standard low cost 4 layer substrate. The standard 4 layer stack up from Advanced Circuits is used since they made all prototypes for this project, and it is available for inexpensive volume production. The relative permittivity of FR4 is 4.5 up to ~1GHz, though this is infrequently specified in a rigorous manner. SMA jacks are most commonly available for 62mil PCBs, and a thicker PCB is more structurally sound, especially for prototype boards that may be used without a case or mounting. 4 layers are required in order to use 50Ω microstrip lines, which is the impedance of most of the signal pathway, since a 50Ω microstrip across a 62mil FR4 core would be unreasonably wide.

For calculating microstrip impedance, it is first necessary to judge the approximate thickness of the PrePreg, which is specified based on how much copper is left on the inner layers. Inner copper layers are used as ground planes, so nearly all copper should remain, and the thickness should be 9.8mil. There is also a specified 10% error in PrePreg thickness, which should be taken into account. The method of Hammerstein is used, with modifications for effective trace width[10].

$$w' = w + (1 + 1/\cosh \sqrt{\epsilon_r - 1}) \frac{t}{\pi} \ln \left(1 + \frac{4 \cdot e}{t/h \cdot \coth^2 \sqrt{6.517w/h}} \right)$$

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + \frac{10}{w/h} \right)^{-a(w/h) \cdot b(\epsilon_r)} \quad a(w/h) = 1 + \frac{1}{49} \ln \left[\frac{(w/h)^4 + [(w/h)/52]^2}{(w/h)^4 + 0.432} \right] + \frac{1}{18.7} \ln \left[1 + \left(\frac{w/h}{18.1} \right)^3 \right]$$

$$b(\epsilon_r) = 0.564 \left(\frac{\epsilon_r - 0.9}{\epsilon_r + 3} \right)^{0.053}$$

$$F_1 = 6 + (2\pi - 6) \exp \left[- (30.666 \cdot h/w)^{0.7528} \right]$$

$$Z_o = \frac{60 \ln \left[\frac{F_1}{w/h} + \sqrt{1 + \left(\frac{2}{w/h} \right)^2} \right]}{\sqrt{\epsilon_{eff}}}$$

The resulting microstrip trace width for 50Ω is 14-16mil. The penalty for a 10% impedance mismatch is negligible (0.05 dB), which allows for leeway in variations of PrePreg thickness, trace width, and copper thickness. 14mil trace width is used because error is reduced if the PrePreg is slightly thinner, which corresponds to a PCB that is compressed to an exact 62mil thickness. This same PCB stack up is used for all devices in the system.

3.1.2 Enclosure

Manufacturer	OKW Enclosures
Model	456.15
Interior Dimensions	61.5mm x 42.0mm x 15.5mm
Material Thickness	0.5mm

Table 2: Line Driver Enclosure

A thin metal case is used for the line driver, which shields against EMI by at least 110dB up to 200MHz and at least 75dB up to 2GHz[6, 12]. Shielding for the line driver is most important since interference before gain affects the signal most significantly.

Some insignificant amount of feedback is possible from radiation within the enclosure, but serious problems could occur if the enclosure resonates at a frequency within the amplifier's bandwidth, causing positive feedback. In order to avoid such resonance, the fundamental mode (lowest resonant frequency) of the enclosure should be well outside of the bandwidth of the amplifier. For the fundamental mode of the enclosure, the largest two dimensions of the enclosure are used to compute the mode. This is not affected by the internal mounting of the PCB, which reduces the smallest dimension only.

$$f_f = \frac{1}{2\pi} \sqrt{\left(\frac{\pi c}{x}\right)^2 + \left(\frac{\pi c}{y}\right)^2} = 4.3GHz$$

where $c = 3 \cdot 10^8 m/s$, $x = 61.5mm$, and $y = 41.3mm$

The fundamental mode is well beyond the bandwidth of the AD8353 amplifiers (2.7 GHz), and will therefore not cause problems. The impedance of the decoupling capacitors between amplifiers has an impedance of $\sim 9.0\Omega$ at 4.3 GHz, which is a helpful but not significant factor in preventing resonance at the fundamental mode.

3.2 Passive Elements

3.2.1 Coupling Capacitors

The specific coupling capacitor used, the Murata GRM155R71H222K 2200pF, was chosen based on manufacturer S Parameters as having a resonant frequency near 150MHz and low Q. Since this capacitor appears repeatedly in the signal path, it is important that it does not contribute to accumulated error due to varying impedance across the band. Low series resistance and a low Q keep the resulting impedance flat so repeated series use will not affect system response significantly.

3.2.2 Power Filter

The power supply for the Line Driver needs to be extremely well filtered, since any noise coming into the first amplifier is significantly amplified both within the Line Driver and in later parts of the analog chain. A low pass topology with ferrites and three terminal capacitors is used. Ferrites dissipate some RF energy instead of blocking it, so some noise is absorbed instead of reflecting back into the unfiltered power supply. Three terminal capacitors are designed to have a higher Q by requiring that power runs the length of the capacitance surfaces, reducing some RF transmission which skips over a two terminal capacitor.

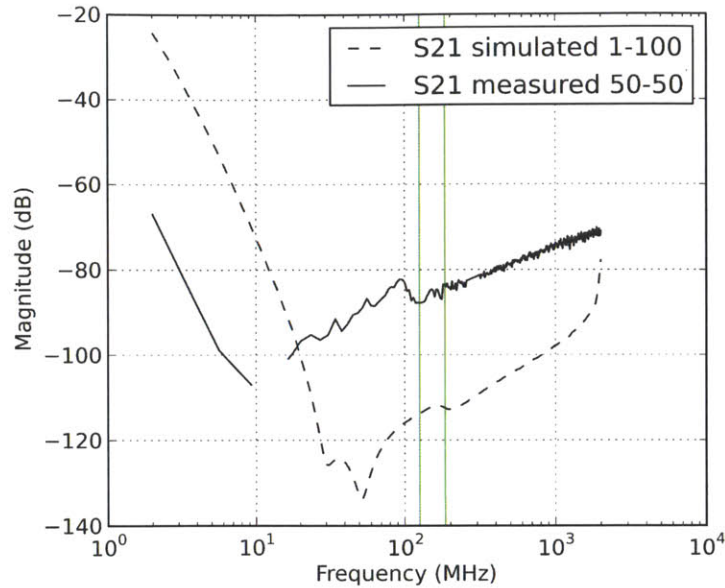


Figure 8: Line Driver Power Filter, S21

This filter was hand tuned for maximum effect at 100MHz. Ferrites and specialty capacitors are not available in many sizes, so the results are not as well targeted as they could be with other component types. It is assumed that the output impedance of the power supply is 1Ω , and that the impedance of the load is 100Ω , which generally matches load currents and voltages for components in the Line Driver. Measurements must be made at 50Ω because of the lab's VNA, so there is some error for that reason. Unlike most other components in this system, the ferrites and capacitors have higher value error ($\pm 25\%$ and $\pm 20\%$), so it is unsurprising that the results do not match simulation well.

3.2.3 Notch Filter

In the United States, the FM band (88.1-107.9 MHz) is the major band for high power consumer audio broadcasts. Even in relatively radio quiet locations, FM radio is still powerful enough that it can cause significant interference to the array by saturating the Line Driver amplifiers. A passive notch filter was added to reduce potential saturation. Adding the filter after the first amplifier keeps the noise figure low, while reducing the saturation risk as much as possible. The notch filter was added to the design shortly before mass production, so one of the goals was to keep the filter small enough to use the original cases. As such, a 6 element filter was the best topology that would fit.

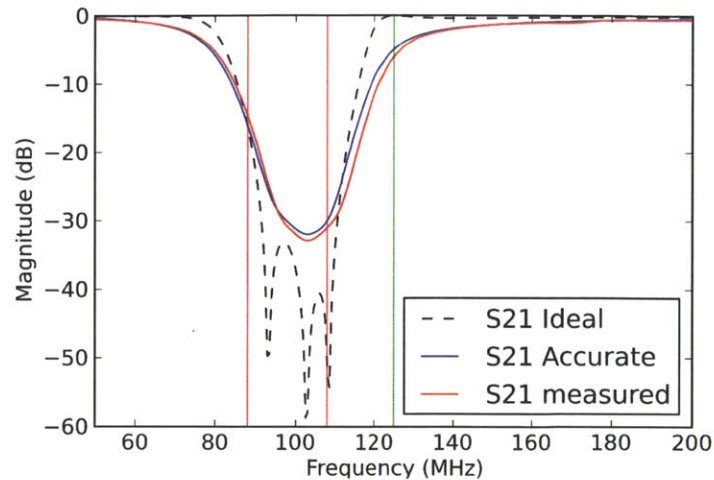


Figure 9: Line Driver Notch Filter, S21

The filter is optimized for maximum attenuation at 88.9-107.9 MHz and minimum attenuation at 125-185 MHz. After selecting a reasonable range of available RF components, Microwave Office was used to optimize using simple RLC component models. The results were later confirmed in Python by optimizing over S Parameter component models. The resulting filter does attenuate unevenly across the signal band, but in locations with FM interference the 20-30dB of attenuation in the notch can prevent array saturation. For reference, a simulation with ideal components is included.

3.2.4 RF Choke

A Mini-Circuits TCCH-80+ choke is used as the last step for applying a DC bias to the signal pathway. Unlike a “good” RF inductor, chokes have a low Q and maintain a fairly level impedance up to high frequency. This helps avoid complex reflections which would result from using a high order low pass filter directly. The choke may not be necessary now that the signal band has been narrowed.

3.2.5 Impedance Matching

Resistive impedance matching is used because it has a more even response across a wide band. The tradeoff is that there is a constant 6dB of attenuation for converting between 50Ω and 75Ω. This attenuation is used to absorb interference picked up by the RG6 cable, as well as any reflections from the Receiver input filter. For more narrow band applications, an LC impedance matcher at both ends of the RG6 cable can recover 12dB of gain with only minor redesign or soldering.

3.3 Active Elements

3.3.1 Amplification

Due to the large amount of gain required, the Analog Devices AD8353 amplifier[4] is used for gain in several places in this design. It has flat 19dB gain up to 2GHz when powered with 5VDC at 42mA. The AD8353 has a reasonable noise figure, 50Ω input and output, and low power use. Examination of the component characteristics leads to a maximum input power of -17dBm for any amplifier, which corresponding output power of 2dBm. The downside of the wide bandwidth is that any additional noise up to 2GHz will be amplified, and will contribute to saturation. Three AD8353 amplifiers are used, for a total gain of 51dB including the impedance match, but before considering the notch filter.

3.3.2 Noise Figure

The noise figure (NF) of a signal chain relates the signal to noise ratio (SNR) at the input and output. A high noise figure corresponds to a signal chain where the SNR is reduced significantly at the output, and is undesirable. The best possible case is that the SNR is equal at the input and output. The AD8353 has a gain of 19dBm at 5V/25C and a

maximum specified noise figure of approximately 7.5 dBm in the 125-185MHz band. The Line Driver's noise figure is calculated with an amplifier immediately after the antenna, followed by -5dBm for the notch filter, followed by a second amplifier. The noise figure is calculated via the noise factor (F) and Friss' formula.

$$\text{Noise factor: } F = \frac{SNR_{LN}}{SNR_{OUT}} = 10^{NF/10}$$

$$\text{Friss' formula: } F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1 G_2} + \dots$$

The resulting system noise figure is 0.39dB including the LNA and the first two Line Driver amplifiers. In general further amplification means that after the antenna LNA, the remainder of the signal chain contributes approximately 0.2dB to the Noise figure. Additional improvements in thermal noise are achieved digitally by averaging the signal, and thereby removing true noise.

3.3.3 Power Regulation

Component power requirements are 42mA at 5V for each amplifier and 100mA at 5V for the antenna bias power. A 5V linear regulator provides immunity from supply output resistance, as well as some measure of low frequency supply noise rejection (specified up to 1MHz in this case). Using a low dropout regulator allows a 6V supply to be regulated down to 5V, which reduces power loss. Switching regulators lose efficiency at low current, so with a 6V supply 83% (5V/6V) is a reasonable efficiency. The Microchip MCP1703 is used in its largest package, which allows heat to be dissipated more easily into the PCB ground plane. The ground plane will also be well connected to the metal case, so ambient outdoor temperature can be easily achieved. At $\theta_{JC} = 62^\circ C/W$ with a maximum operating temperature of $125^\circ C$, and an ambient temperature of $25^\circ C$, the maximum input voltage is:

$$V_{IN,max} = 5V + \frac{125^\circ C - 25^\circ C}{\theta_{JA} \cdot 226mA} = 12.14V$$

It is therefore possible to use a 12V input if necessary, although 6V is both sufficient and preferred to reduce power use.

3.4 Final Design

3.4.1 System Diagram

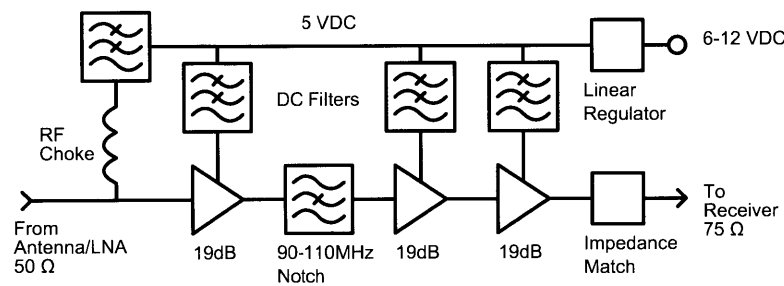


Figure 10: Line Driver System

3.4.2 Appearance



Figure 11: Line Driver v5

3.4.3 Usage Specifications

- Power: 6-12VDC, 230mA
- Input: 50Ω SMA
- Input Power: -49dBm max
- Input Bias: provides 5VDC, 100mA
- Notch filter: -20dBm, 90-110 MHz (as built)
- Gain: 47dB @ 125MHz, 51dB @ 185MHz
- Output: 75Ω F-type
- Output Power: -4dBm max

4 Receiver Design

4.1 Signal Chain

Each individual Receiver has circuitry to process 4 signals, and produces 8 outputs to the ADCs. This is the maximum density which could be achieved on a 6" wide PCB with single sided components, which fits nicely into a 4U PCB rack. Because the Receivers boards are intended to be placed in parallel, the ground plane of each PCB provides shielding between Receivers on the same rack.

4.1.1 Clock Splitter

The IQ demodulator used in the Receiver takes a clock input of twice the desired LO. This will be explained later, but for now valid LO frequencies are anything within the signal band of 125-185MHz, and therefore valid clock input frequencies are 250-370MHz. This doubled LO clock signal is referred to as "2xLO" as a reminder that double the actual LO frequency is being distributed to the Receivers.

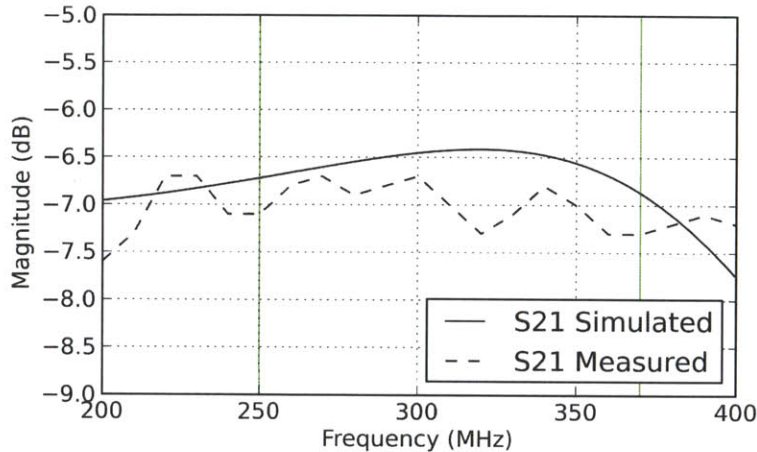


Figure 12: Receiver LO Splitter, S21

In order to split the 2xLO input for use on the four signals, a tree of lumped element Wilkinson power splitters with a center frequency of 310MHz is used, which is twice the bandpass center frequency. The resistive elements of the power splitters are not directly necessary, as each output is loaded by an identical device, but will help reduce any reflections due to the traces between the splitter and the demodulators. The overall attenuation of the splitter is 6.5-7.5dB within 250-370MHz, which is reasonably close to the ideal of 6dB. The test circuit was measured with a spectrum analyzer because the lab VNA was malfunctioning near 300MHz, so accuracy is affected.

4.1.2 Bandpass Filter

As described in Section 2, the KR electronics 2753 bandpass filter is used at the input of the Receiver to limit the signal band. There is no particular restriction on the filter range or quality due to IQ demodulation, so the steepness of the filter only reduces additional noise and total RF power in the system. The filter is placed first in order to reduce out-of-band power, and so that the resistive impedance matchers of the Line Driver and Receiver will absorb the resulting out-of-band reflections.

4.1.3 Attenuator

A Hittite HMC470LP3 digital attenuator is used to attenuate the signal before amplification[8]. The attenuator has a range of 1-32dB, including insertion loss, in 1dB steps. Attenuators are controller by a shared bank of switches, with bypass capacitors at each channel to prevent crosstalk. The wide range of attenuation allows for flexibility when operating in areas of high in-band interference. The attenuator is placed before any amplifiers in order to prevent saturation.

4.1.4 Amplification

A pair of Analog Devices AD8353 amplifiers provide additional gain before the IQ demodulator.

4.1.5 IQ Demodulator

An Analog Devices ADL5387 is used to demodulate the signal[5]. The ADL5387 takes in double the LO frequency and produces two appropriately phased LOs internally. It has a 50Ω differential input and differential outputs which must be loaded with an impedance of 200-450Ω, and a specified voltage gain of 4.3dB. The output must be transformed to 50Ω impedance for filtering and transmission to the ADC. Power gain is voltage gain modified by the difference in impedances, which in this case is 50Ω/450Ω or -9.5dB, for a total of -5.2dB.

Because the internal LOs are created from a higher frequency, there can be no assurance that the LOs of multiple IQ demodulators are in phase. Experimentally, identically clocked IQ demodulators have LOs that are either exactly in phase or 180° out of phase. This relationship is established when power is applied, and is maintained until either power or the double LO is interrupted. Different LO phase is equivalent to different signal phase, so array calibration must take into account a potential 180° phase difference. On the other hand, array phase calibration will also correct LO phase differences.

Errors introduced by IQ demodulation include IQ phase imbalance, which is specified as up to 0.2° variation from the proper 90°, and IQ magnitude imbalance of up to 0.1dB. IQ demodulators also have some inherent imaging, where the high sideband and low sideband bleed into each other. The ADL5387 has an image rejection specification of -65dB for sidebands 1.2MHz away from a 150MHz LO, but still needs to be quantified as the sidebands become further away. With the ADC phase imbalance, the phase is relative to other incoming signals, and can be corrected after an FFT. The IQ imbalance is relative to the LO, so the exact relationship between the LO and ADC clock would be necessary to correct it. Without high precision calibration hardware integrated into the receiver, the IQ imbalance can be considered an inherent error in the system. A method for quantifying IQ imbalance with a generated signal was developed for the Omniscop[15], and can be used to measure the exact imbalance and quantify potential error.

4.1.6 Differential Impedance

For the differential ports on the IQ demodulator, the textbook answer for determining differential impedance is frequently simulation. This is in no small part because differential impedance varies depending on whether the two traces are carrying inverted signals. For short traces which are definitely carrying inverted signals, the National Semiconductor LVDS Owner’s Manual[18] has good approximate formulas. In this case, edge coupled microstrips with a differential impedance of 100Ω are used. There is an inherent impedance mismatch at the output of the IQ demodulator, so exact matching is not necessary, and the demodulated signal is low enough frequency that reflections will have little effect. 100Ω is a convenient middle ground between 50Ω demodulator output impedance and the 450Ω transformer input impedance.

4.1.7 Low Pass Filters

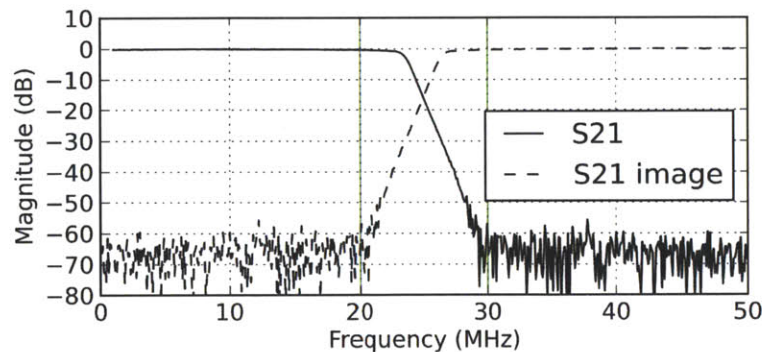


Figure 13: Receiver Output Filter S21

The ADCs sample an unimaged signal, so a low pass filter is needed at the output of the IQ demodulator to remove any demodulated signal further than 25MHz from the LO. With an ideal 25MHz low pass filter, the Omniscop would have an analysis bandwidth of 50MHz. In order to produce a feasible filter, the KR Electronics model 2999 low pass filter was custom made for the Omniscop. It maintains a passband up to 20MHz, and achieves 60dB of attenuation by 30MHz, allowing for 10MHz of cutoff transition. The low pass filter limits analysis bandwidth to 40MHz.

Component	Gain (dB)
Impedance Match	-6
Bandpass Filter	-1
Attenuator	-1
Amplifiers	+38
Demodulator Voltage Gain	+4.3
Demodulator Impedance (50Ω/450Ω)	-9.5
Total	24.8

Table 3: Receiver Gain

4.2 Final Design

4.2.1 Overview

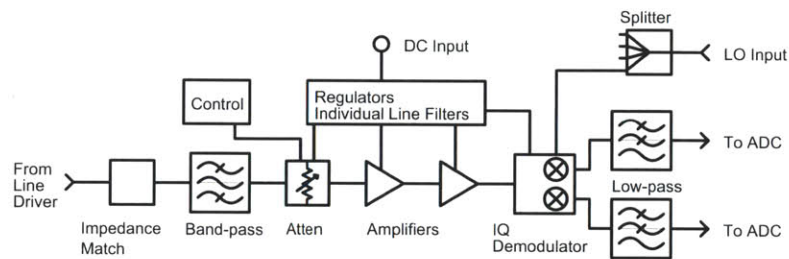


Figure 14: Receiver System

4.2.2 Appearance

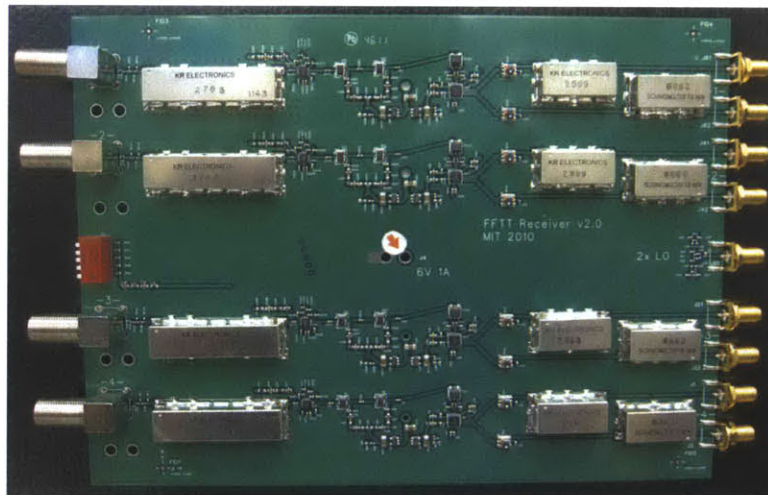


Figure 15: Receiver v2.0

4.2.3 Usage

- Power: 6VDC, 1.1A
- Input: 75Ω F-type
- Input Power: -29dBm max

- Input Bias: capacitively coupled
- 2xLO: 50Ω SMA
- 2xLO Power: 1-13dBm
- 2xLO Frequency: 200-400MHz
- Gain: 23dB IQ combined (as built), attenuated to -8dB in 1dB steps
- Output: 50Ω SMA
- Output Power: -3dBm max

5 Swapper Design

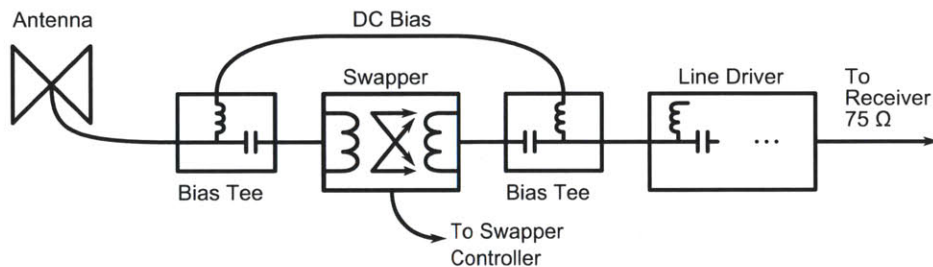


Figure 16: Swapper Signal Path

Analog signals are inverted with a Mini-Circuits ZMAS-1 Attenuator/Switch (“Swapper” module)[16], which consists of a 4 diode bridge between two transformers. The ZMAS-1 control input is supplied with $\pm 20\text{mA}$, which turns on two of the bridge diodes and incrementally connects the transformers with alternating polarity. The ZMAS-1 has good isolation between its ports, but has the disadvantage of requiring a negative current supply relative to its chassis/signal ground. There is a small amount of contamination (-40dB) between the control port and signal output port, so the control port input must be well filtered. The advantage of the purchased swapper module for this type of signal inversion is avoiding the difficulties of dealing with exactly matching diodes, resistances, and precise center tapped transformers, which are all required for good phase balancing. Swappers are placed between the antenna and line driver to counteract as much crosstalk and steady state interference as possible.

Because the need for inversion was discovered after the line drivers had been produced, the Swapper system is designed to work with the existing line drivers. The swapper’s inherent transformers require two bias-tees for passing DC bias power from the line driver to the antenna without crossing the swapper. The swapping mechanism should be integrated into future line drivers, resulting in fewer discrete components and significantly reduced hardware costs. The two hardware components developed are a module placed in the array to control several swapper modules (“Controller”), and a module to transmit inversion data from the ROACH to the Controller (“Transceiver”).

5.1 Structure

5.1.1 Swapper Driver

In order to properly supply the swapper with $\pm 20\text{mA}$, the ZMAS-1 was measured at DC and treated as a resistor and diode in series. The result is 7.69Ω and a 0.746V diode drop. The swapper is driven by $\pm 3.3\text{V}$ with additional resistance to reduce the resulting current to 20mA . Incremental current changes around 20mA have a slight effect on attenuation through the swapper, so adding extra resistance reduces sensitivity to supply voltage. Additionally it is much easier to produce a negative 3.3V rail from Omniscope-standard 6VDC . In the event that different cabling between the Controller and swapper changes resistance significantly, the load resistors on the Controller can be changed relatively easily without affecting other device properties.

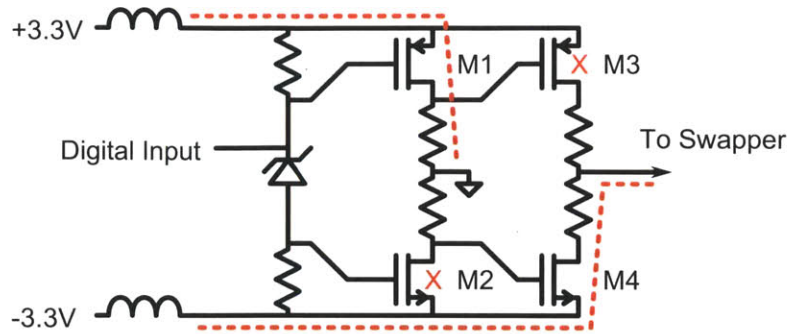


Figure 17: Swapper Driver

Control current noise is only somewhat attenuated (~20dB) by the swapper itself, so keeping digital noise out of the control current is still important, otherwise the purpose of the swapper system is defeated. In order to filter the Controller's power supply more effectively, the positive and negative rails have dummy loads to keep the supplies at constant current. The signal band can therefore be more heavily filtered on the rails with less concern for step response, since the step magnitude is reduced to the mismatch of the dummy load. The digital control input is less sensitive to noise due to the transistor characteristics at the low current involved.

5.1.2 Shift Registers

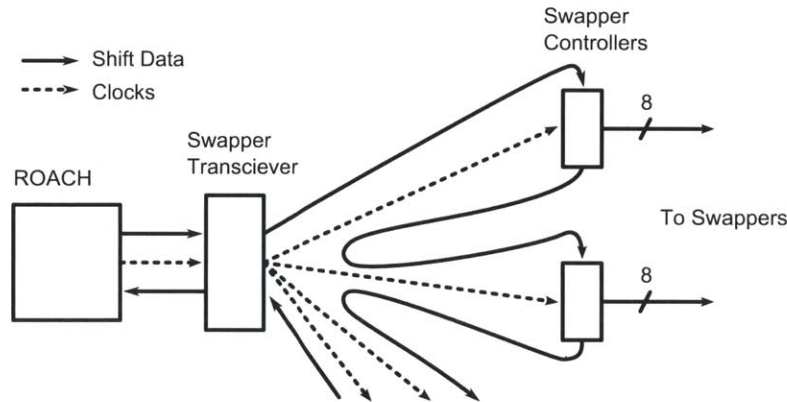


Figure 18: Swapper Data Path

The Swapper system behaves to the ROACH as a 32 bit shift register with a registered output. This 32 bit shift register is distributed into 4 Controller modules per ROACH, each of which has a monolithic 8 bit shift register chip. Each Controller drives 8 swappers, and is physically placed with the line drivers for a group of 4 antennas in order to keep the control cables short and free of interference. The Transceiver module is placed at the ROACH, and connects the ROACH and the Swapper Controllers appropriately.

During swapping one 512-sample FFT frame is discarded by the ROACH to avoid any transient signals resulting from the swapper's operation. There is therefore a 10us (512 samples / 50Msps) window for transitions. Total transition time begins at the ROACH register clock, and ends when the swapper outputs are no longer significantly affected by transients. In order to reduce clock delay, the register clock is distributed in a star topology in order to avoid retransmission delays between Swapper Controllers. Because the shift registers can be transmitted in advance, the shift signal is organized as a series of loops back through the Swapper Transceiver. The system is organized so most of the transition time can be used to allow transients from the swapper and driver circuit to settle, with very little time spend on control transitions.

5.2 Details

5.2.1 Controller Power Supply

The negative rail of for the swapper drivers is supplied by a Linear Technology LT1617 negative switching DC/DC converter, followed by a TI TPS7A3001 adjustable negative linear regulator. There is not a large selection of available products appropriate for the Controller's requirement of 160mA for 8 swappers, and the LT1617 is rated at only 100mA in this configuration, so two independent negative rails each power 4 swappers. The linear regulators are kept independent to avoid interfering with the feedback system of the LT1617. The linear regulator helps reduce the effect of output resistance within the filters necessary to remove switching noise from the LT1617. Although the switching frequency is well below the signal band (55kHz in simulation), tones on the control input of the swapper could have a modulating effect on the signal, so should be well filtered. The switching regulators convert +6V to -5V, and the linear regulators then generate -3.3V.

5.2.2 Transceiver to Controller Connection

LVDS over Cat 5 cable with 8p8c (RJ45) jacks connects the Transceiver and Controllers. CAT-5 is an inexpensive cable choice, even when purchased assembled, and has 4 differential pairs compatible with LVDS. This is exactly the number of data lines necessary for the shift register topology used. LVDS is designed for high speed signaling, but in this case is used at low speeds over long distance, which is also appropriate[18]. The maximum cable speed is extremely low (less than 100 kHz for the register clock), but the ability to withstand common mode offsets prevents any issues arising from differing ground planes between the digital electronics and the signal pathway in the antenna array. Differential signaling also reduces VHF interference which will inevitably be picked up en route to the Controller.

Fairchild LVDS transmitters, receivers, and repeaters are used. Repeaters are used at the Transceiver to resend shift data between Controllers, so the maximum length of an LVDS transmission is only the length of the longest Cat 5 cable. Fairchild LVDS chips have a guaranteed differential output voltage of 250mV at the transmitter and a required differential input voltage of 100mV. Using a Belkin specification for 24AWG Cat 5e UTP, which is 28.6Ω/1000ft, cable length can be at least 1000ft under pure DC analysis. It is unlikely that this distance is possible realistically, so field testing should be done to determine what length is functional, and at what clock frequency.

$$V_{ID} = V_{OD} \cdot \frac{100}{100+28.6 \cdot 2} = 159mV \geq 100mV$$

5.2.3 ROACH to Transceiver Connection

The ROACH has two banks of 8 digital GPIO pins. Each bank can either be all inputs or all outputs. The GPIO connector is a double row of 0.1" header pins with one row of pins grounded. 3.3V is supplied by the ROACH on one of the corner pins. 0.05" ribbon cable is used between the GPIO banks and the Transceiver, which is presumably the ROACH designer's intent since the impedance of the ribbon cable is 100Ω with every other wire grounded. The output impedance of the GPIO pins is not clearly specified by datasheet of the driver used <cite TI SN74AVCH4T245>, so the Transceiver end is terminated at 100Ω to reduce reflections. Termination is AC only, otherwise DC current into the terminating resistors could combine to violate the absolute maximum of the driver chips depending on what loads are placed on unused GPIO pins. The ribbon cable is split between the Transceiver and the ROACH so that the input and output signals can be separated to the two banks. If a GPIO bank is not available for input, the shift data return signal can be ignored, with the understanding that additional checks may be necessary during signal processing.

5.2.4 Timing

The critical timing window for the Swapper system is making sure the register clock leads to a control signal transition within a single discarded FFT frame. Standard Cat 5 cable propagates at ~0.6c, so a 100m cable takes 560ns to propagate the register clock. Cable propagation and LVDS hardware propagation can be mitigated by sending the register clock pulse in advance of the FFT frame which will be discarded. Since the ROACH clock is 50MHz, the register clock offset can be calibrated in 20ns increments. With a reasonable margin for error, 8-9us of the 10us frame time can be used to allow the control output to settle.

5.2.5 IQ Channel Selection

Although crosstalk between most of the analog chain can be mitigated by swapping, IQ pairs are not swapped relative to each other. ADC crosstalk must therefore be mitigated by other methods. Crosstalk between I and Q results in uncorrectable signal error, effectively an IQ phase imbalance that changes with signal amplitude. If IQ pairs are sent to separate ADCs, the ADC cable crosstalk problem is solved at the cost of combining I and Q within the X-Engine, which requires phase analysis between ADCs on separate ROACH boards. If IQ pairs are sent to the same ADC, ADC channels must be chosen to minimize some metric of crosstalk between the IQ pairs.

ADC channel selection can be optimized to minimize the sum of total IQ crosstalk, or to minimize the worst case crosstalk between IQ pairs. Both cases can be easily solved with linear optimization routines. Blossom V[9] is a fast solver for minimum total crosstalk (min-cost perfect matching). GLPK[2] can be used if MATLAB is not sufficient for minimizing worst case crosstalk, and its syntax is intended for linear optimization. It has not been determined which optimization method is best for the Omniscope, nor whether to signal crosstalk or noise correlation is the better starting metric.

5.3 Final Design

5.3.1 System Diagram

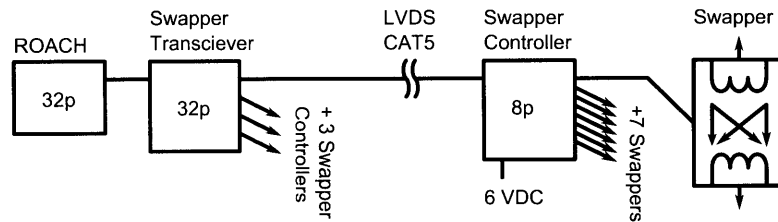


Figure 19: Swapper System

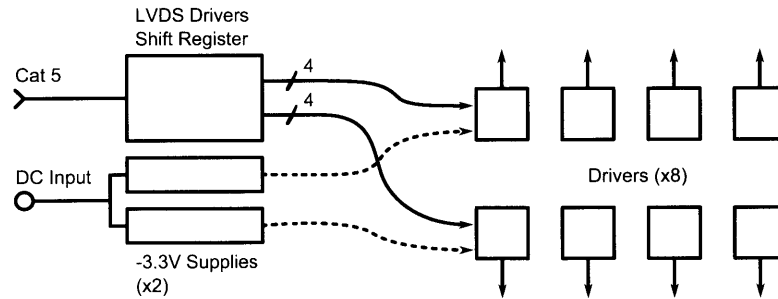


Figure 20: Swapper Controller

5.3.2 Appearance

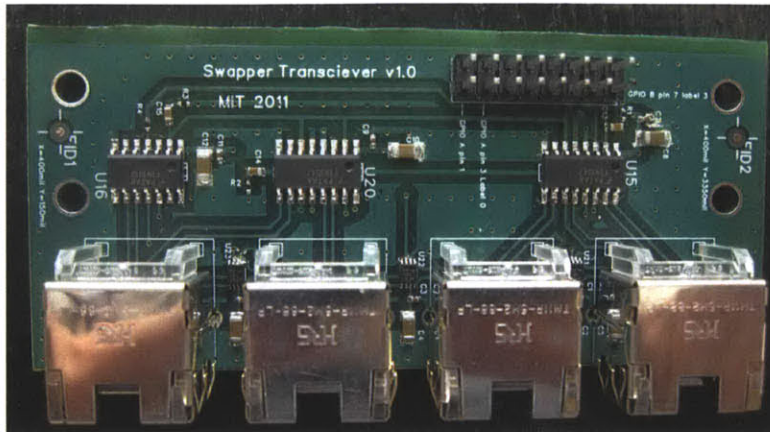


Figure 21: Swapper Transceiver v1.0

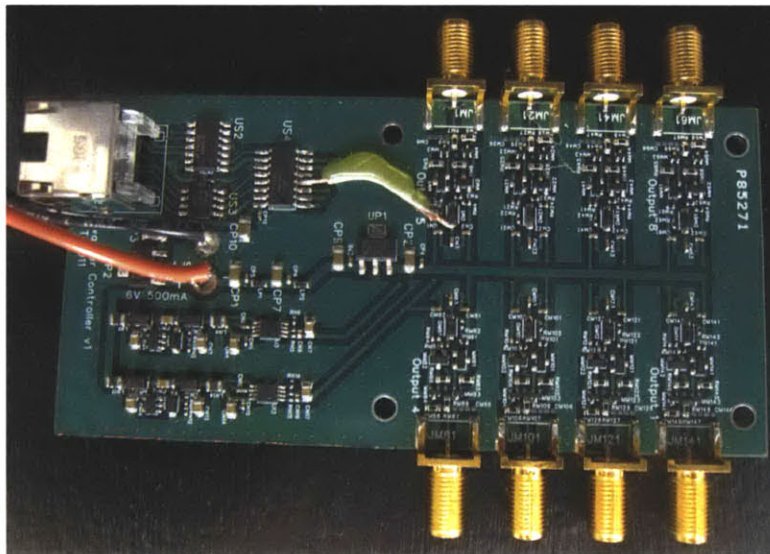


Figure 22: Swapper Controller v1.0

5.3.3 Usage

- Power: 3.3VDC (Transceiver)
- Power: 6VDC, 400mA (Controller)
- Cat 5 length: 1000ft (untested)

6 Hardware Performance

S-Parameters are measured with an Anritsu MS2024A Vector Network Analyzer. The MS2024A is very inexpensive for a VNA, and comes with some limitations that affect measurements. Output power is restricted to high (~ 0 dBm) and low (~ 25 dBm), which means that attenuators must be used to avoid saturation in most circuits with amplifiers. Port impedance is fixed at 50Ω , so matching pads must be used for 75Ω ports. When extra adjustment hardware is

added, the resulting measurement is adjusted to account for the losses from the added components. Assuming a good impedance match, these corrections are direct multiplication or division of S-Parameters. It is not possible to measure the phase of a 50-75Ω matching pad, but as a fully resistive devices the group delay can be assumed to be flat.

6.1 Line Driver v5.0 (Notch Filter)

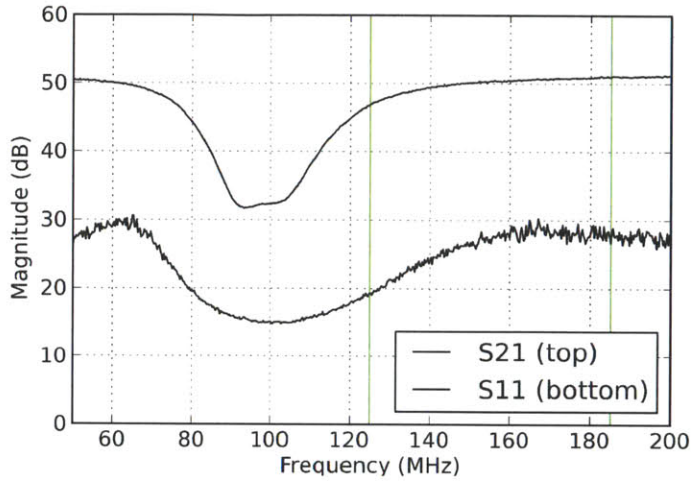


Figure 23: Line Driver v5.0, S Parameters, 50-200MHz

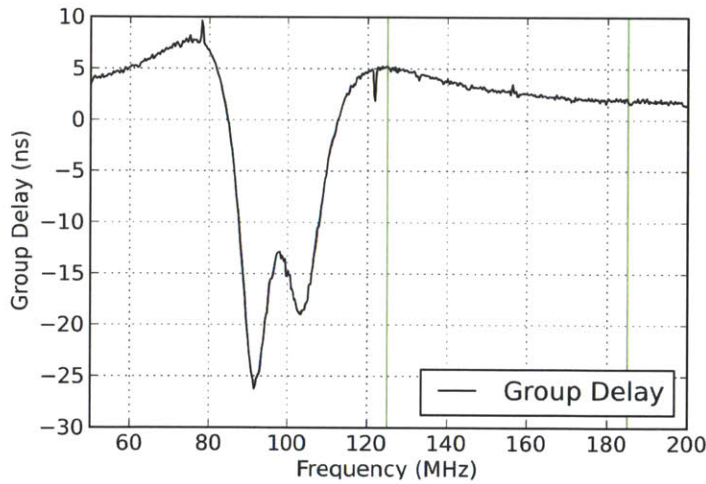


Figure 24: Line Driver v5.0, Group Delay, 50-200MHz

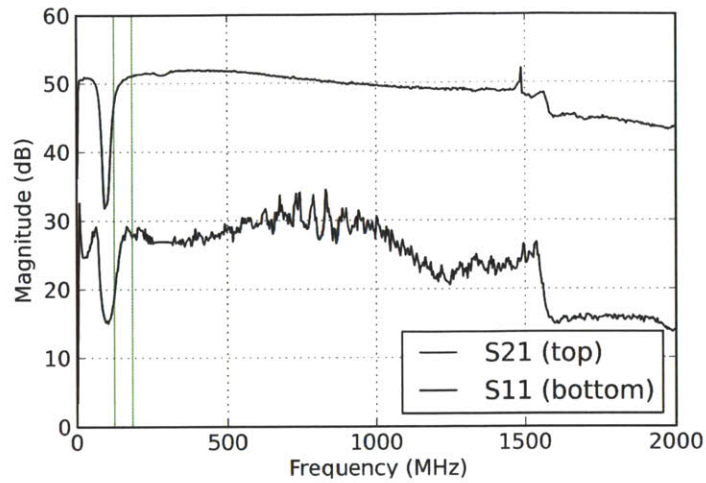


Figure 25: Line Driver v5.0, S Parameters, 2-2000MHz

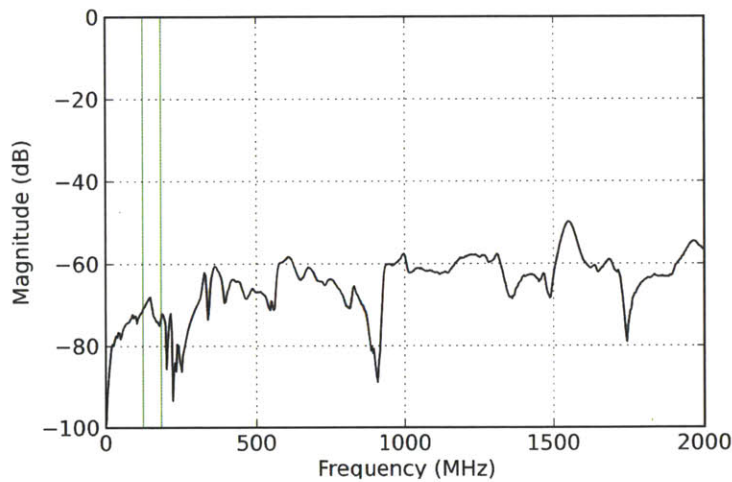


Figure 26: Line Driver v5.0, Power S21, 2-2000MHz

S21 was measured at high power with 3x 20dB attenuators at the input and a 75-50Ω matching pad at the output. S11 was measured at low power with no attenuation. Because the bias-tees available were not capable of handling 226mA for a line driver, the effect of power supply noise was measured by directly injecting signal at the power input and measuring signal output (“Power S21”). There is inaccuracy due to the lack of impedance control in the power supply wiring. Group delay is calculated from S21 with a 0.6ns adjustment for the additional matching pad at the output. The attenuators have a group delay of roughly zero.

6.2 Receiver v2.0

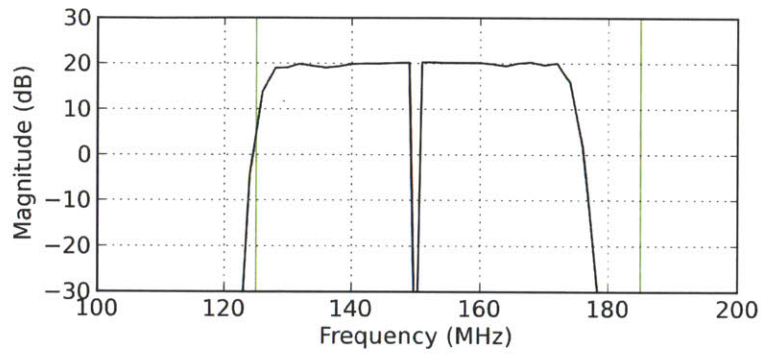


Figure 27: Receiver v2.0, S21, 150MHz LO

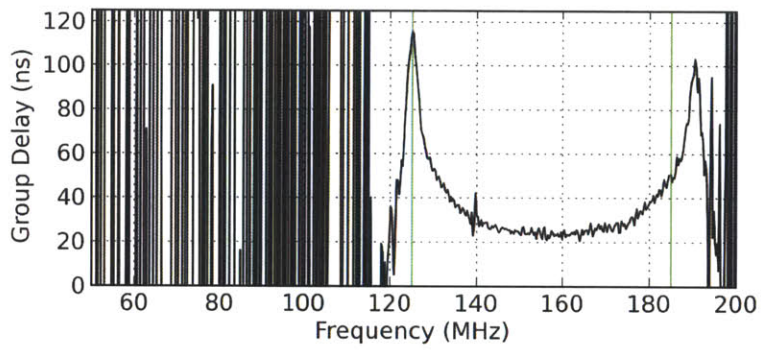


Figure 28: KR 2753 Bandpass Filter, Group Delay, 50-200MHz

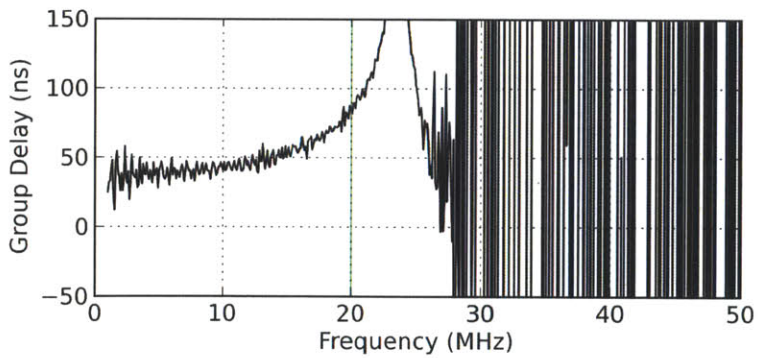


Figure 29: KR 2999 Low Pass Filter, Group Delay, 1-50MHz

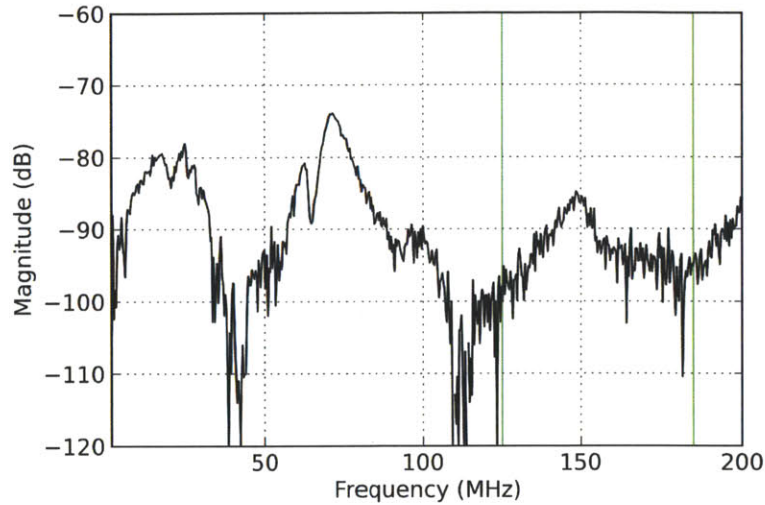


Figure 30: Receiver v2.0, Power S21, 2-200MHz

S21 was measured with a spectrum analyzer to the Q output of the receiver, since the VNA cannot handle different input and output frequencies. The attenuator is set to its minimum attenuation. Observed power is 3dB less than total IQ output power, since half of the power goes to the I output as the LO and signal phase shift relatively. Maximum receiver gain is therefore 23dB. Group delay does not apply well to demodulation, but for a rough measure the group delays of the filters are included since they are the most significant source of uneven group delay. Power supply interference is measured as for the line driver.

6.3 Swapper v1.0

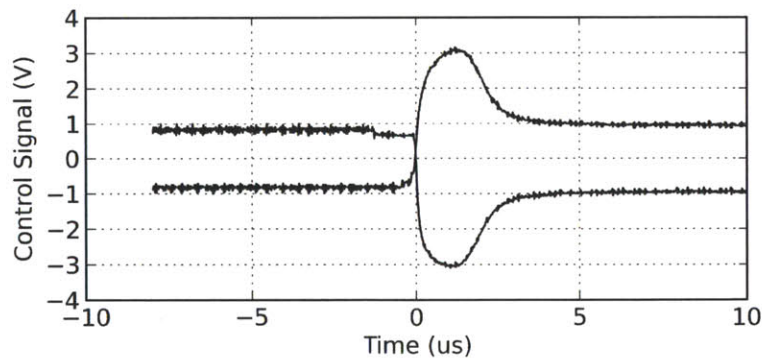


Figure 31: Swapper v1.0, Transitions

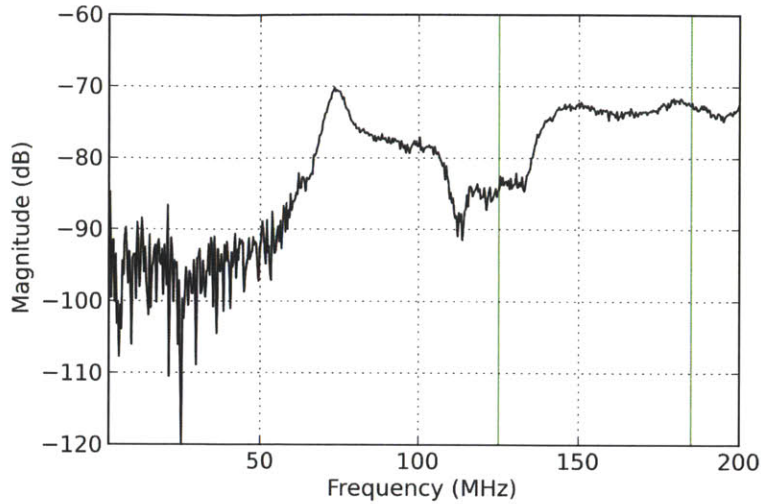


Figure 32: Swapper v1.0, Power S21, 20200MHz

A Swapper Transceiver and Swapper Controller were connected to 8 Swappers, and the Controller output was measured with an oscilloscope set to $1M\Omega$ impedance. Both transition directions are shown. The measured DC voltage magnitude is approximately 0.9V before the transitions and 1.0V after the transitions, indicating that the output voltage settles after the transition. Ideally these voltages would be the same, and the difference is the result of a mismatch between the dummy load current and the control current into the Swapper. The mismatch itself is not critical, but the slow settling of the control voltage (and thus current) may have a slight affect on signal magnitude. This mismatch can be fixed by replacing the driver output resistors so that the control current is closer to 20mA.

7 Clock Distribution

This section is recommendation about how to distribute clock signals within the processing hub.

7.1 ADC/ROACH Clock

The ADC clock is 50MHz, and will be generated by a signal generator using a 10MHz GPS reference. The clock will be converted from analog to digital as necessary, and be distributed digitally to the ADCs directly, most likely as LVDS via an LVDS splitter. The ROACH board associated with each ADC will clock itself from one of the ADC data clock lines coming in over the Z-DOK connector.

7.2 2xLO Clock (IQ Demodulator)

Device	Gain (dB)	Total Power (dBm)
PLL Valon 5007	N/A	7-9
Amplifier Mini-Circuits ZHL-1A-S	+16	23 - 25
4-way splitter Mini-Circuits ZFSC-4-1-S+	-6.5	16.5 - 18.5
1m SMA cable	?	?
Bandpass Filter KR Filters 2979 w/SMA	-1.5 ±0.5	14.5 - 17.5
8-way splitter Mini-Circuits ZBSC-8-82-S+	-10	4.5 - 7.5

Table 4: LO Distribution

The 2xLO signal is 250-370MHz, and will be generated by a PLL using a 10MHz GPS reference (the same as above). The 2xLO is amplified and split to each receiver board. Bandpass filters at each block of receiver boards help reduce harmonics and any interference picked up en route. Constant phase imbalance from these components results in a phase error identical to cable length mismatch, and thus can be calibrated out similarly. The amplifier or PLL output power can be adjusted depending on cable losses. The table lists components necessary for a recommended 2xLO distribution network. Other suitable Mini-Circuits amplifiers are the ZHL-1-2W with 3dB of input attenuation or the ZHL-2-12. A clean power supply may be needed for the amplifier.

8 Conclusion

8.1 Performance

Overall signal gain is the sum of LNA, Line Driver, and Receiver gains. The resulting 90dB is slightly short of the original 100dB goal. In addition, some loss is expected in the RG6 cable between the antennas and the processing hub. Some extra gain can be obtained by exchanging the resistive impedance matching in the current Receiver with an LC circuit, for 6dB of additional Receiver gain. The maximum output power of the Receiver leaves 2.5 unused ADC bits, so for future designs, an additional 10-15dB of gain immediately before or after the IQ demodulator would improve gain while increasing ADC range usage.

The most significant group delay variation is the Receiver bandpass filter. If group delay is not flat enough, more shallow cutoff would reduce the group delay variations at the edge of the signal band.

The most likely source of signal error for the system is the IQ crosstalk within each ADC board, which cannot be solved with swapping. Two possible solutions are:

1. Despite the disadvantages of up/down conversion, it results in a single ADC channel per polarization, so swapping would completely solve first order crosstalk without IQ phase imbalance and IQ crosstalk issues.
2. The signal pathway converts from differential at the IQ demodulator to single ended for ADC input, then differential within the ADC, and is a major cause of crosstalk. If demodulation results in a differential signal, future designs should strongly favor placing the demodulator and ADC on the same PCB to avoid unnecessary conversions.

If saturation is still problematic despite additional filtering, signal power and noise levels would be much easier to manage with narrow band components. Avoiding wide band design will keep out-of-band noise down and allow more gain and signal power without additional filtering. Alternatively, adding a single pole filter after each amplifier would gradually reduce response without much added complexity.

8.2 Cost

Device	Cost per polarization
Antenna	\$54.25
Bias Tees + Swapper	\$167.85
Line Driver	\$33.55
RG6 Cable (100m)	~\$30
Receiver Filters	\$87
Receivers	\$85.80
Swapper Transceiver + Swapper Controller	(not yet manufactured)

Table 5: Device Costs

Exact costs listed here are the result of producing or purchasing sufficient hardware for the 128 polarization array. 128 Line Drivers and 32 Receivers were manufactured in China by Burns Industries, and are undergoing testing at the time of writing. The most significant reducible cost is the introduction of the Swapper system. Some of the Swapper system has not been mass produced, so exact costs are not available, but even just the RF hardware is very expensive relative to the rest of the signal chain. Incorporating swapping into the line driver will significantly reduce cost for similar designs, assuming appropriate discrete components can be found. Digitizing signals at the antenna would remove the need for a swapping system, which would also solve the problem.

8.3 Deployment



Figure 33: West Forks Array Deployment

As mentioned in the introduction, small arrays of 16 polarizations have been deployed in Greenbank, West Virginia and West Forks, Maine. The West Forks deployments used hand soldered Receivers (v1.0) and Line Drivers (v3.0). These small arrays were capable of detecting the sun and several Orbcomm satellites, which is no small feat for a new telescope architecture. Since then, the Swapper system and the Line Driver notch filters have been added, which should greatly increase the sensitivity of the analog chain. Significant improvements have also been made to the digital processing system. The 128 polarization Omniscope is scheduled to be deployed this spring. If successful, the 128 polarization array will be a major milestone in the development of the Omniscope, and a significant step towards creating the most accurate 3D map of our universe to date.

References

- [1] Murchison Widefield Array, 2011. <http://www.mwatelescope.org/>.
- [2] GNU Linear Programming Kit, 2012. <http://www.gnu.org/software/glpk/>.
- [3] Analog Devices. ADS5272, 2009.
<svn://hardware/development/datasheets/AnalogDevices-CASPERADC-ads5272.pdf>.
- [4] Analog Devices. AD8353, 2012.
<http://www.analog.com/en/rfif-components/rfif-amplifiers/ad8353/products/product.html>.
- [5] Analog Devices. ADL5387, 2012. <http://www.analog.com/pr/ADL5387-complementary>.
- [6] Chomerics. EMI Shielding Theory, 2012. http://www.chomerics.com/products/documents/emicat/pg192theory_of_emi.pdf.
- [7] FCC. 104.1 MHz FM, 2012.
<http://transition.fcc.gov/fcc-bin/fmq?list=0&facid=26897>.
- [8] Hittite. HMC470LP3, 2012. <http://www.hittite.com/products/view.html/view/HMC470LP3>.
- [9] V. Kolmogorov. Blossom V. <http://pub.ist.ac.at/~vnk/software.html>.
- [10] G. Kompa. *Chapter 3 - Methods of Microstrip Analysis*. Artech House, 2005.
- [11] KR Electronics. 2753, 2011.
<svn://hardware/development/datasheets/KRElectronics-2753Bandpass.pdf>.
- [12] Laird Technologies. Shielding Effectiveness Calculator, 2012. <http://www.lairdtech.com/ad/#>.
- [13] A. Liu and M. Tegmark. A Method for 21cm Power Spectrum Estimation in the Presence of Foregrounds. *Phys. Rev. D*, 83(103006), 2011. [arXiv:1103.0281v2 [astro-ph.CO]].
- [14] A. Liu and M. Tegmark. How well can we measure and understand foregrounds with 21cm experiments? *MNRAS*, 419(3491-3504), 2012. [arXiv:1106.0007v3 [astro-ph.CO]].
- [15] A. Lutomirski. *Quantum Money and Scalable 21-cm Cosmology*. PhD thesis, Massachusetts Institute of Technology, Sep 2011. Retrieved from Omniscopes svn.
- [16] Mini-Circuits. ZMAS-1, 2012. <http://www.minicircuits.com/pdfs/ZMAS-1.pdf>.
- [17] NASA. Wilkinson Microwave Anisotropy Probe, 2012. <http://map.gsfc.nasa.gov/>.
- [18] National Semiconductor. LVDS Owner's Manual, 2008.
http://www.national.com/en/interface/lvds/lvds_owners_manual.html.
- [19] A. Perko. The Omniscopes: Mapping the Universe in 3D With Neutral Hydrogen. Master's thesis, Massachusetts Institute of Technology, Jun 2011. Retrieved from Omniscopes svn.
- [20] Samtec. QSE Series, 2012.
<http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=QSE>.
- [21] N. Sanchez. On the Instrumentation of the Omniscopes. Master's thesis, Massachusetts Institute of Technology, Jun 2011. Retrieved from Omniscopes svn.
- [22] M. Tegmark and M. Zaldarriaga. Omniscopes: Large Area Telescope Arrays with only $N \log N$ Computational Cost. *Phys. Rev. D*, 82(103501), 2010. [arXiv:0909.0001v2 [astro-ph.CO]].
- [23] UC Berkeley. CASPER, 2011. <https://casper.berkeley.edu/>.
- [24] UC Berkeley. PAPER, 2011. <http://astro.berkeley.edu/~dbacker/eor/>.

A Background Knowledge

Below is a list of topics which you may need to familiarize yourself with, and which will not be explained fully in this thesis.

Most of the people working on the Omniscope come from a physics or signal processing background. If you, the reader, are one of those people, then many of the concepts implied by this thesis may be unfamiliar to you. If you will be working with RF circuitry, you will need a general idea about most of these concepts at some point anyhow. One good starting point is Pozar's *Microwave Engineering*, which is intended for actual (non-redshifted) microwave design, but covers many of the RF topics. Any MIT 6.002 course material is good for the basics of RLC circuits. If you are not up to speed on Fourier transforms and frequency space, Oppenheim & Willsky's *Signals & Systems* is highly recommended. Be sure to read the other Omniscope theses which precede this one, as some knowledge of the Omniscope is also implied. Wikipedia is, of course, an excellent starting point, and is fairly reliable when it comes to math.

- FFT / Fourier Transform
- Nyquist Frequency
- IQ Demodulation
- Electrical Impedance
- Quality Factor (Q)
- TEM Impedance
- S Parameters
- Group Delay
- Differential Signaling
- Noise Figure
- PCB / Gerber / mil = 0.001"
- Microstrip

A.1 TEM Impedance

TEM Impedance is arguably the most important among the concepts listed above for understanding the analog chain of the Omniscope. Any time a signal is transmitted down a wire or across a PCB, impedance must be considered at least briefly. A review of the relevant basics of TEM Impedance and its relationship to power transmission is included here.

TEM impedance, which is usually simply referred to simply as the "impedance" of a wire or trace, is related to the admission that electrical signals actually take time to travel from one end of a wire to the other. In its simplified form it is an extension of basic electrical impedance methods. Electrical engineers would like to assume that a potential applied to one end of a wire is immediately present at the other end, and in many cases this is perfectly fine. Unfortunately the assumption breaks down at high frequencies and long distances, both of which are present in the Omniscope. More accurately, signals propagate down wires as transverse EM waves between two conductors. For single ended signals, one conductor "carries" the signal, and the other is grounded. For differential signals, two conductors "carry" the signal, with the possibility of a third grounded conductor. The impedance of a wire, Z , is the square root of the ratio of effective continuous inductance and capacitance between the two conductors, $Z = \sqrt{L/C}$. Impedance is a continuous property of a wire, like physical diameter. Wire impedance is usually calculated with approximate formulas which yield functional, but not exact, results.

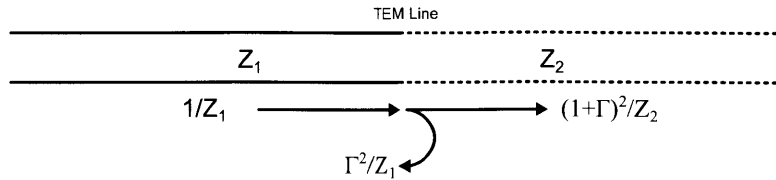


Figure 34: TEM Impedance Mismatch Power

When a signal propagating along a wire with impedance Z_1 encounters a new impedance Z_2 , some amount of the signal is reflected back from the interface between the two impedances, and the remainder is transmitted. This is exactly the same principle as light hitting glass, where an EM wave encounters a change in impedance. The fraction of EM wave magnitude reflected is $\Gamma = (Z_2 - Z_1)/(Z_2 + Z_1)$, and phase can be ignored for two wires with completely real impedance. As such, normalized signal power starts as $1/Z_1$, and Γ^2/Z_1 power is reflected. Because the field magnitude at the interface must match, there is also a $1 + \Gamma$ wave propagating forward, so $(1 + \Gamma)^2/Z_2$ power is transmitted forward into the new impedance. Sources and loads can be treated similarly, with resulting reflections from mismatches. The goal of tracking impedances in the Omniscope is to transmit as much power as possible through the analog chain, which requires impedance matching along the signal path. Additionally, if signals reflect back and forth, uneven frequency response will result from reflections interacting destructively or constructively depending on phase.

B Schematics and PCBs

B.1 Line Driver v5.0 Schematic

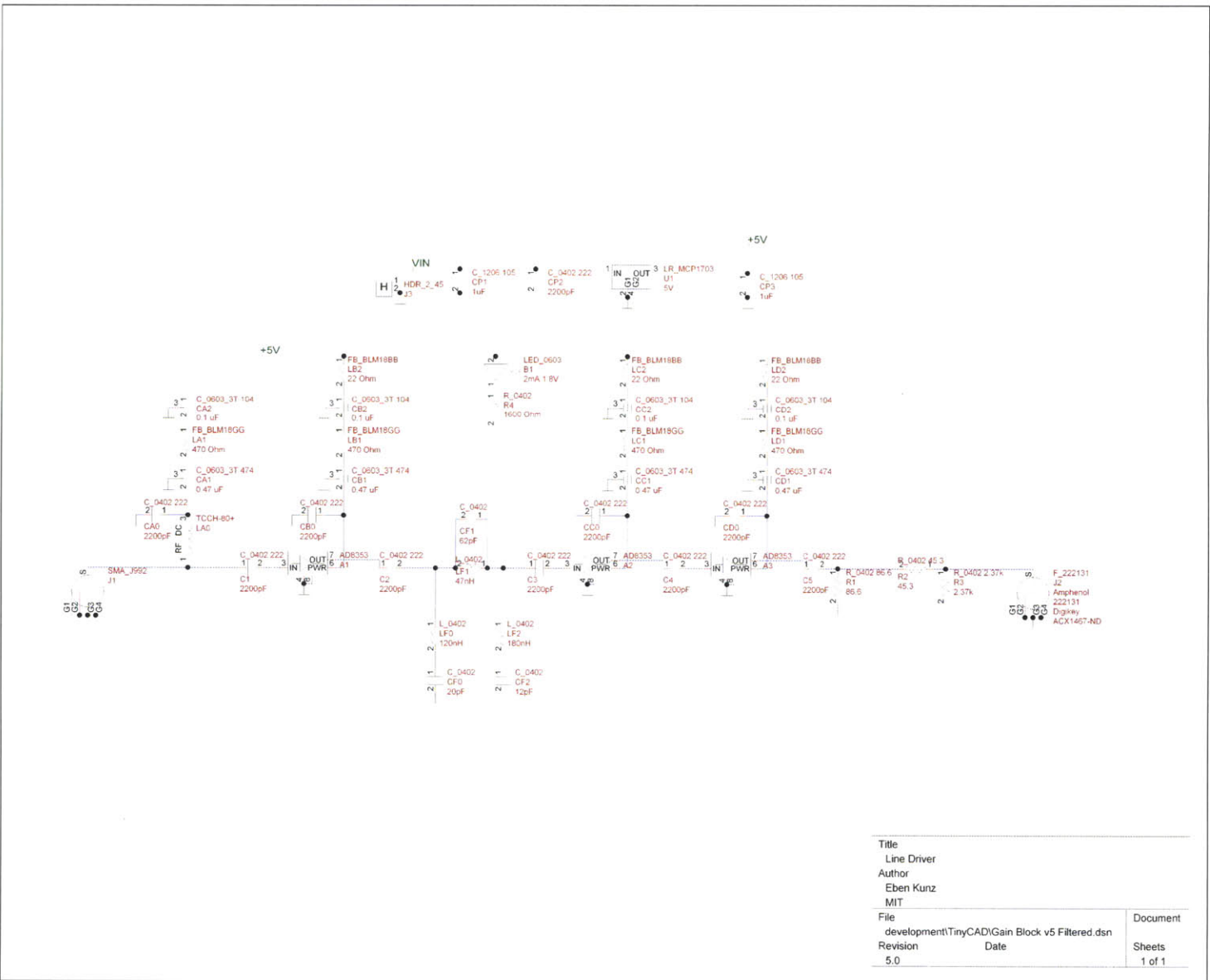


Figure 35: Line Driver v5, Schematic

B.2 Line Driver v5.0 PCB

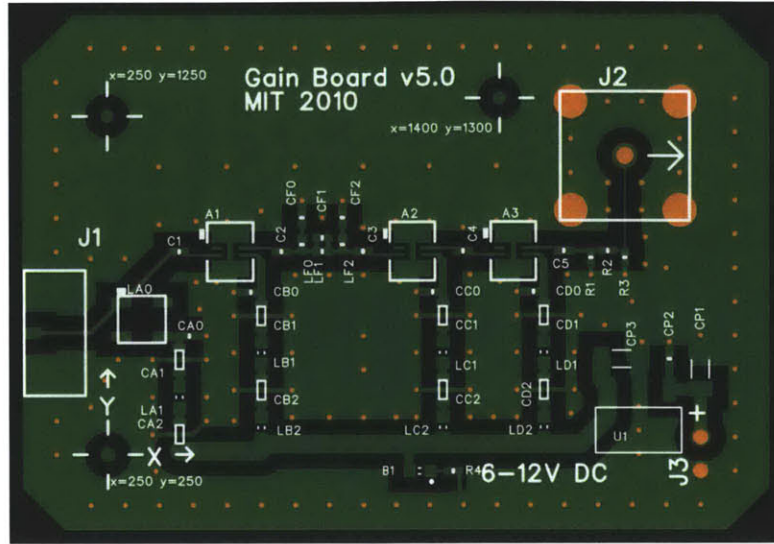


Figure 36: Line Driver v5, PCB

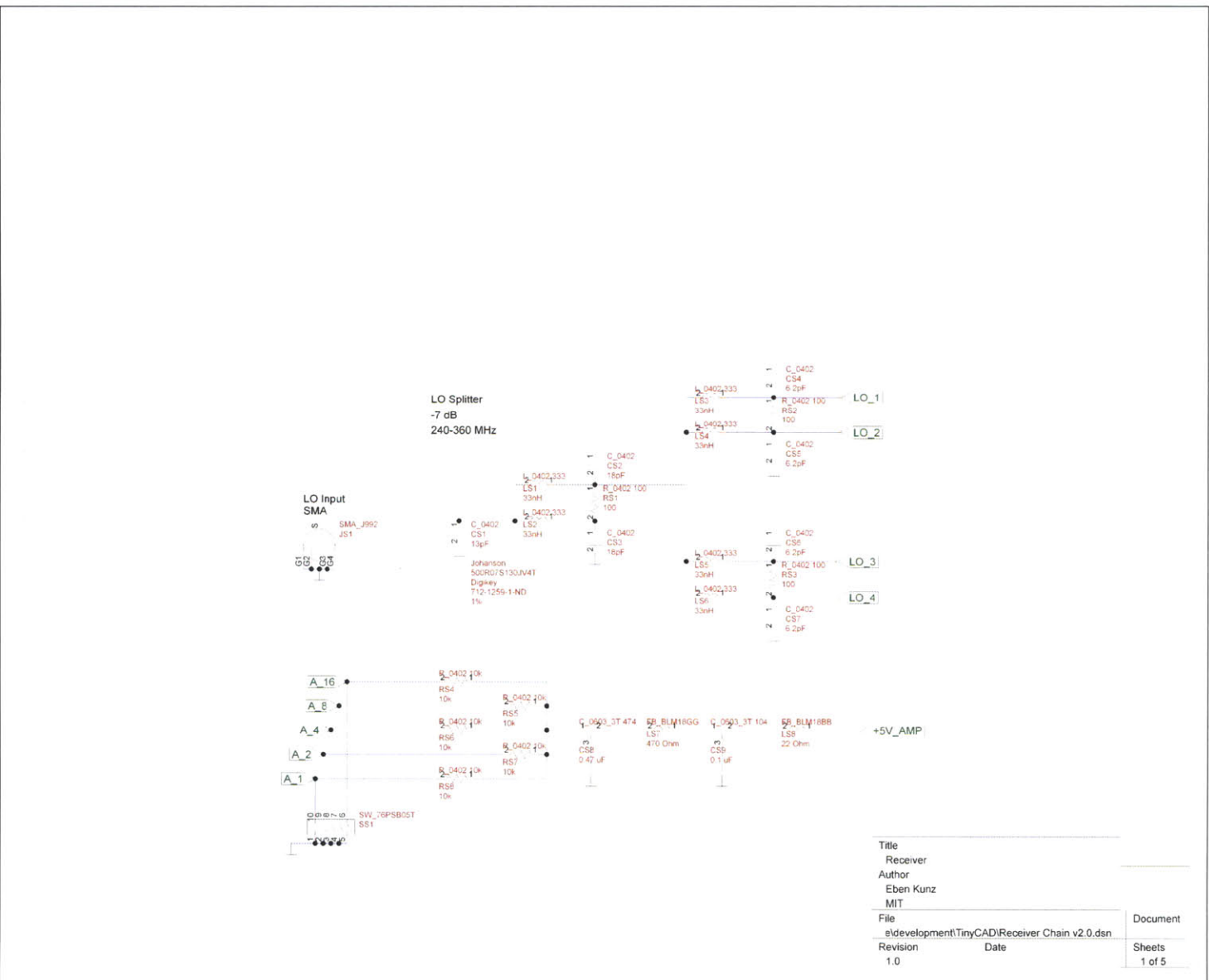
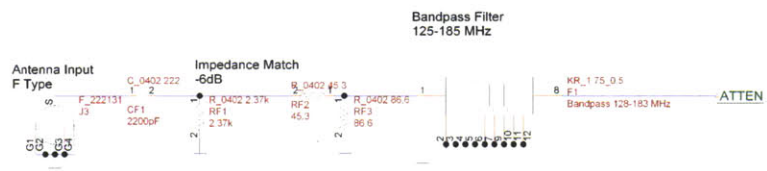
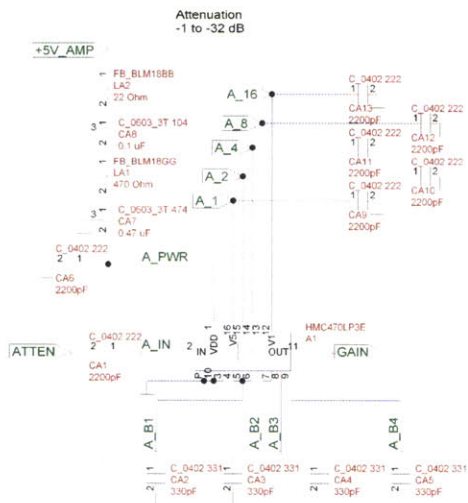


Figure 37: Receiver v2.0, Schematic 1 of 5

Figure 38: Receiver v2.0, Schematic 2 of 5



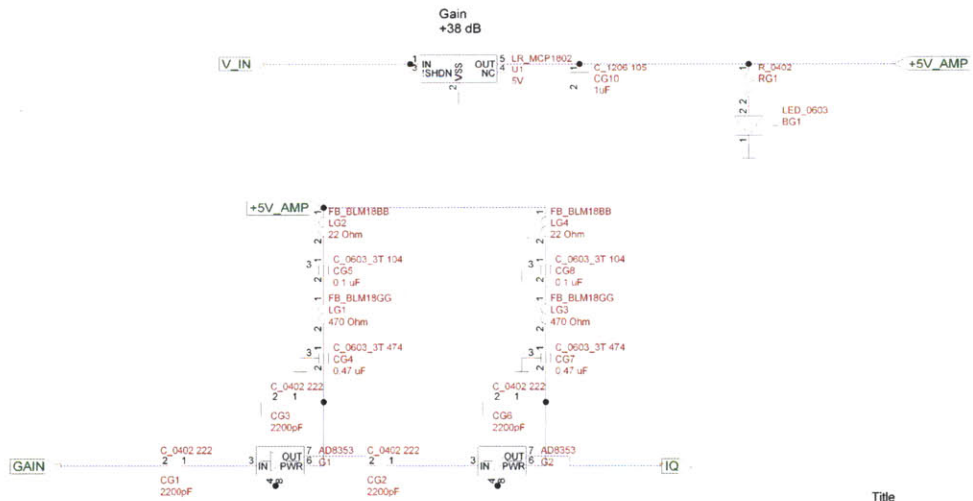
Title Receiver		Document Sheets 2 of 5
Author Eben Kunz MIT		
File e:\development\TinyCAD\Receiver Chain v2.0.dsn	Date	
Revision 2.0		



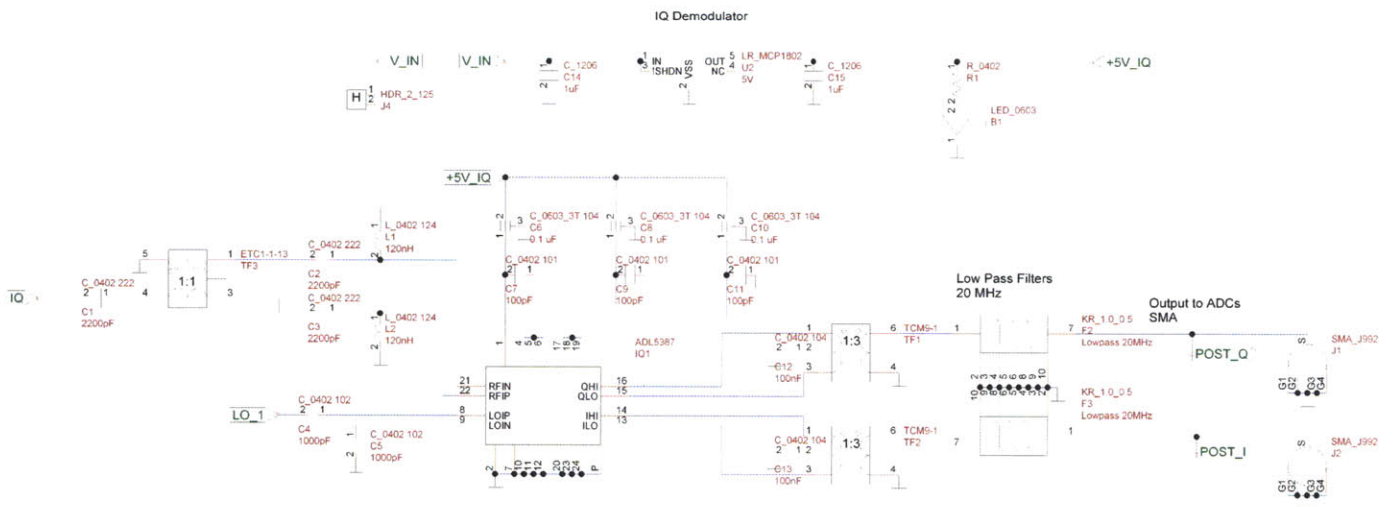
Title	Receiver
Author	Eben Kunz
File	MIT
Revision	2.0
Date	
Document	3 of 5

Figure 39: Receiver v2.0, Schematic 3 of 5

Figure 40: Receiver v2.0, Schematic 4 of 5



Title		Receiver
Author		Eben Kunz
MIT		
File		e/development/TinyCAD/Receiver Chain v2.0.dsn
Revision	Date	
2.0		
Document		4 of 5



Title		Receiver	
Author		Eben Kunz	
File		_e\development\TinyCAD\Receiver Chain v2.0.dsn	
Revision	Date	Document	
2.0		Sheets 5 of 5	

Figure 41: Receiver v2.0, Schematic 5 of 5

B.5 Schematic v1.0 Schematic

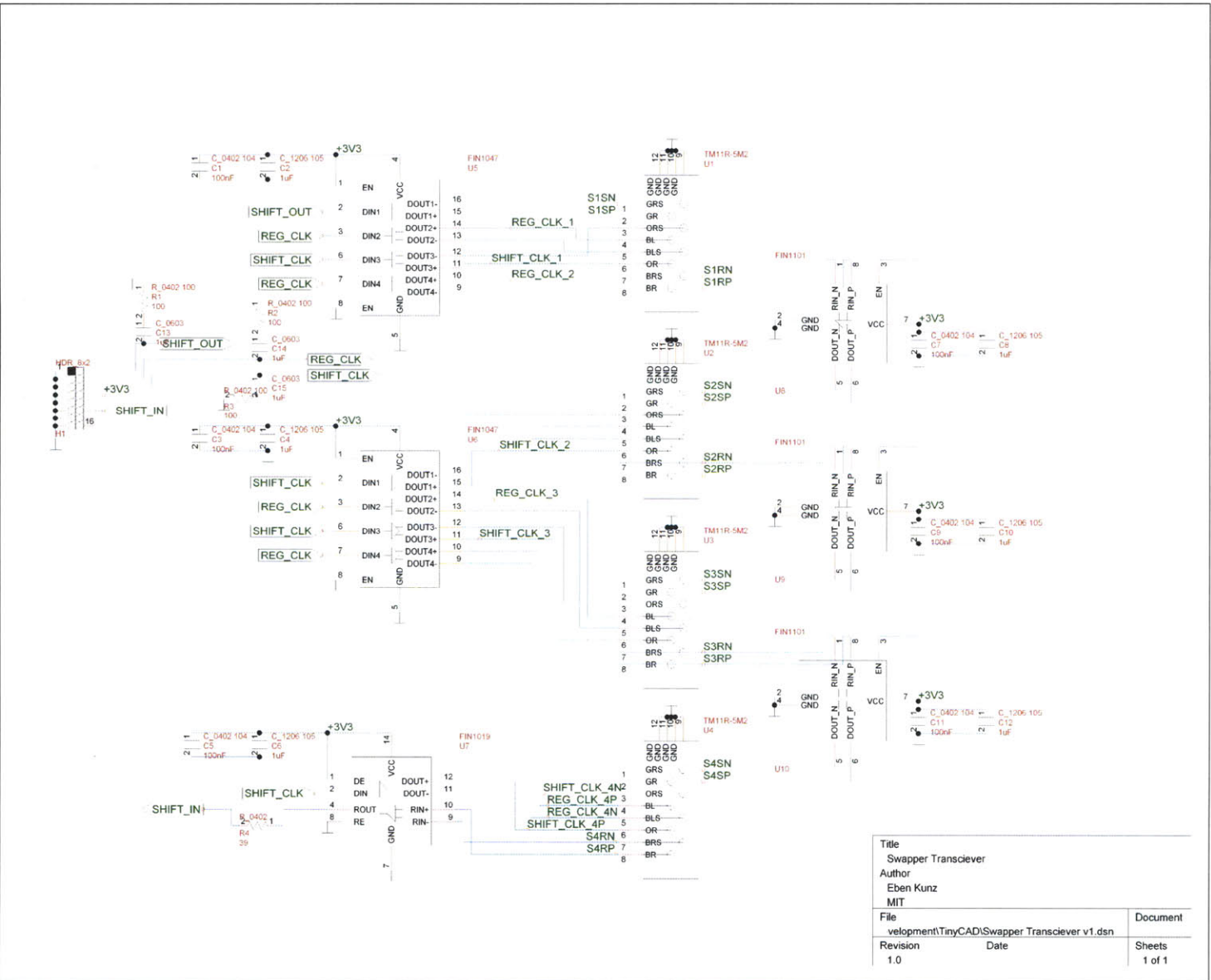
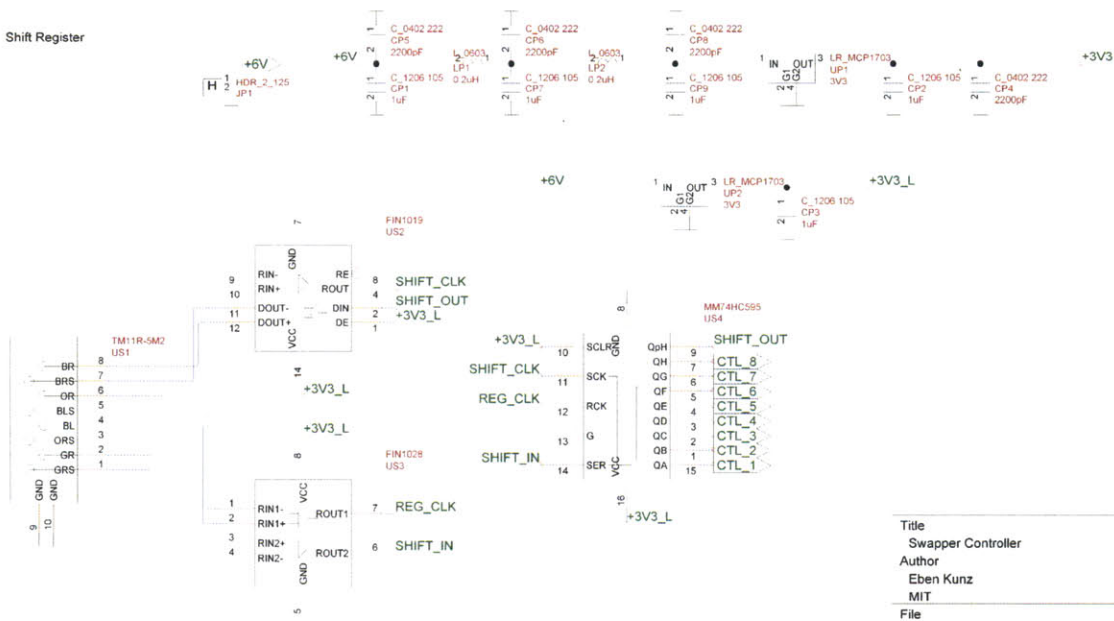


Figure 43: Swapper Transceiver v1.0, Schematic

Title		Swapper Transceiver	
Author		Eben Kunz	
MIT			
File	Document		
velopment/TinyCAD/Swapper Transceiver v1.dsn			
Revision	Date	Sheets	
1.0		1 of 1	

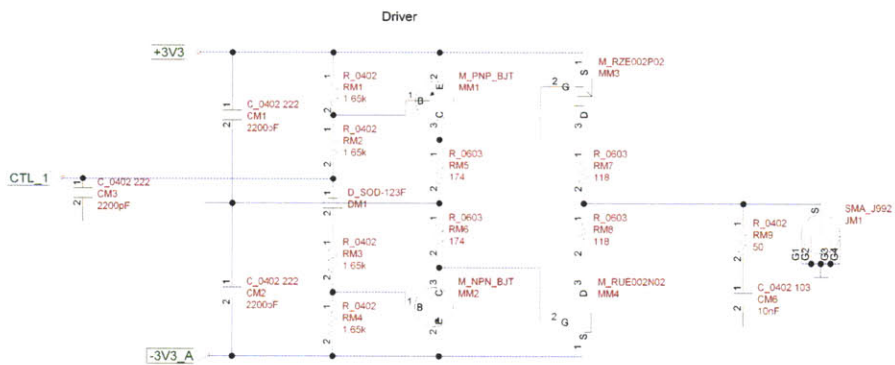


Title		Swapper Controller	
Author		Eben Kunz	
File		velopment\TinyCAD\Swapper Controller v1.dsn	
Revision	Date	Document	Sheets
1.0		1 of 3	1 of 3

Figure 44: Swapper Controller v1.0, Schematic, Logic

Figure 45: Swapper Controller v1.0, Schematic, Power Supply





Title		
Swapper Controller		
Author		
Eben Kunz		
MIT		
File		Document
velopment\TinyCAD\Swapper Controller v1.dsn		
Revision	Date	Sheets
1.0		3 of 3

Figure 46: Swapper Controller v1.0, Schematic, Driver

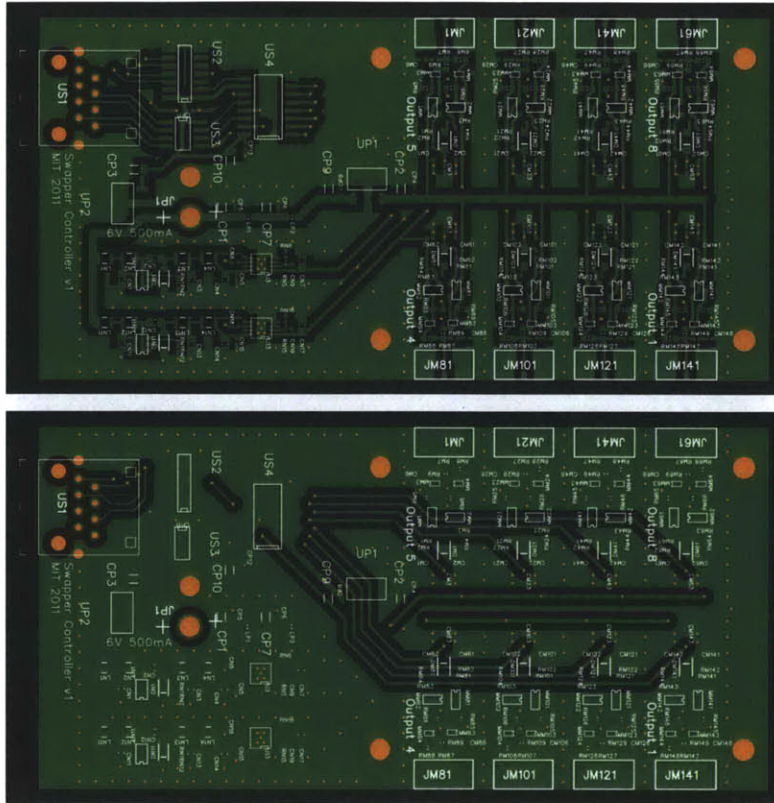


Figure 48: Swapper Controller v1.0, PCB (Top/Bottom)