Body Powered Thermoelectric Systems

by

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Abstract

Great interest exists for and progress has be made in the effective utilization of the human body as a possible power supply in hopes of powering such applications as sensors and continuously monitoring medical devices [1]. This report furthers into the area of thermal energy harvesting, which focuses on using the temperature differential generated between the human body and the ambient environment to generate power. More specifically, a body-powered, thermoelectric-based power supply and system will be introduced and examined, with hopes that this technology will be utilized alongside low-power, medical monitoring applications in order to achieve self-sufficiency. This report also analyzes the performance of existing thermoelectric-based body-powered energy harvesting applications and compares that with the new design introduced in this work. The new designs were able to output upwards of $25\mu W/cm^2$ or, equivalently, $280\mu W$ for the entire heat sink system. Additionally, this report details the physics associated with thermoelectric modules, addresses the issues with modern thermoelectric heat-sinks, introduces two new types of wearable, conformal heat sinks, quantifies the performance of the body-powered thermoelectric supply, tests a flexible EKG processing board, and analyzes future paths for this project.

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Lastly, I cannot begin to comprehend the impact my family has had in the development of this thesis as well as in the development of my character. Yet, I will attempt to document it here nonetheless. My father, Raghu, my mother, Sandhya, and my sister, Keertana, have been there for me day in and day out. They are the smartest and most loving people I know.

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-Krishna
May 15th, 2012

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Overview

The utilization of energy harvesting in running low power, bio-monitoring applications has become more prevalent with the advent of new circuit design techniques and technologies. Thermoelectric generators (TEGs) are of particular interest in body-worn energy harvesting due to their ability to generate power from a temperature gradient between the ambient and the skin [2]. Apart from the ability to harvest energy from arbitrarily small temperature differences, the absence of moving parts is another appealing factor in utilizing such a device for energy harvesting. As with all heat engines a temperature differential is required to generate power, in this case an effective heat-sink is required to maintain a temperature differential across the module. This thesis not only addresses main issues with existing types of heat-sinks in wearable applications, but also introduces a new type of thin, wearable, conformal, and comfortable heat-sink which aims to solve the issues of maintaining a temperature differential across the body. Additionally, this 2-D heat-spreading technique is applied in not only the design of a flexible TEG, but also in an ultra-low power Electrocardiograph (EKG) acquisition and processing unit which, due to its power-hungry nature, provides a foundation for self-sufficiency. Ultimately, such a stand-alone, body-powered, EKG system may be used to continuously monitor patients within a care center or be deployed around the world and aid in monitoring the vitals of soldiers, all while avoiding the need for battery replacement.

1.2 Thermoelectric Generators

1.2.1 Seebeck Effect

Thermoelectric generator (TEG) behavior is characterized by the Seebeck Effect, which details the conversion of a temperature gradient across a conductor into a voltage [4, 6]. More specifically, when considering a single electrically conducting pipe, say, with a temperature gradient across its length, conduction charge carriers (either holes or electrons) will flow away from the hot side of the pipe towards the cold side. This net flow of charge yields an electric potential build-up called the Seebeck voltage. This voltage, ΔV, is defined as follows:

$$\Delta V = -S\Delta T, \tag{1.1}$$

where S is the Seebeck coefficient and ΔT is the temperature differential across the conductor.

In order to utilize this Seebeck voltage, one cannot simply connect probes across this conductor and expect a usable voltage. Due to the probe itself developing a Seebeck voltage, an inherent thermocouple is formed between this conducting pipe and the probe. If, however, the probe and the pipe were made of materials with differing Seebeck coefficients, a net voltage may be expected from the system. In general, a thermocouple relies on differing Seebeck coefficients to generate a voltage from a temperature gradient, as illustrated in Figure 1.1.

The Seebeck voltage across a thermocouple containing two differing conductors then becomes

$$V = \int_{T_1}^{T_2} (S_{Metal1}(T) - S_{Metal2}(T))dT \tag{1.2}$$

where $S_{Metal1}(T)$ and $S_{Metal2}(T)$ are the respective, temperature-dependent Seebeck coefficients of the two metals composing the thermocouple, and T_1 and T_2 are the cold and hot side temperatures.

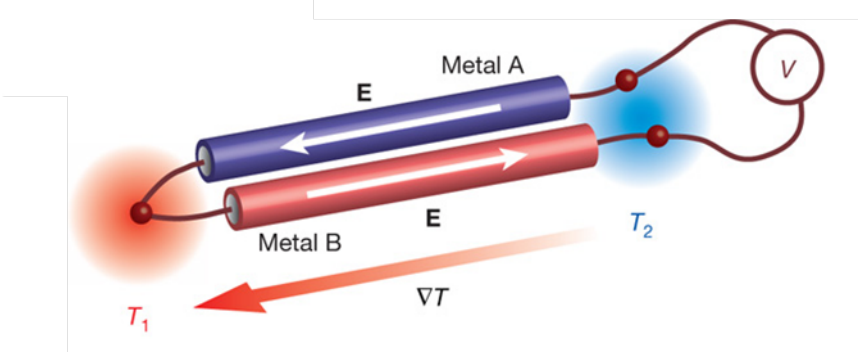


Figure 1.1: The Seebeck Effect, when viewing a single thermocouple [7].

This principle may be applied to the TEG, where the two conductors of the thermocouple are doped n-type and p-type semiconductors. Notice that, now, when a temperature gradient is applied, holes (h+ in Figure 1.2) in the p-type and electrons (e-) in the n-type diffuse away from the hot source. This is apparent when examining the polarity of the Seebeck coefficient for n-type and p-type materials, where p-type have a positive coefficient and n-type a negative coefficient. And, since holes moving in the one directions is equivalent to electrons moving in the other, a closed circuit is formed between the thermocouple and the load. By arranging hundreds of thermocouples in this electrically-series, thermally-parallel pattern, the Seebeck voltage across individual thermocouples is added linearly, as shown in Equation 1.3.

$$V = N\alpha_{couple}\Delta T \tag{1.3}$$

Here, V is the open-circuit voltage across the TEG, N is the number of p-n thermocouples, α_{couple} is the Seebeck coefficient, and ΔT is the temperature differential.

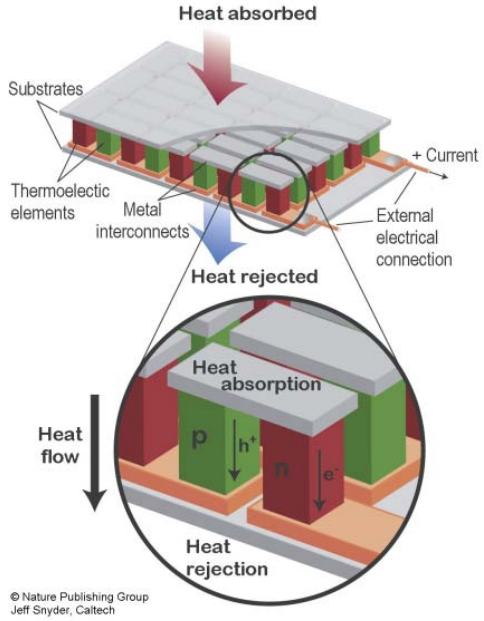


Figure 1.2: The internals of a TEG, focusing on a single thermocouple upon applying a temperature gradient [5].

1.2.2 Thermoelectric Composition and Materials

A typical TEG module, shown in Figure 1.2, contains two ceramic layers surrounding a patterned semiconductor layer. The ceramic top and bottom surfaces are required in part for structural stability

as well as for ceramic's inherently low electrical conductivity and high thermal conductivity. These properties are important in not only providing electrical insulation within the semiconductor layer, but also to ensure maximum heat transfer from one side of the ceramic material to the other due to its high thermal conductivity.

Further inspection of the semiconductor layer, see Figure 1.2, reveals doped n-type and p-type semiconductor material. Each module contains numerous thermocouples, which contain a single n-type and p-type semiconductor connected with an electrical junction. The two-terminal thermocouples are arranged in an electrically-series, thermally-parallel pattern, where one thermocouple's n-type block is connected to another's p-type block. More specifically, all p and n blocks see the same hot and cold side temperatures resulting in every thermocouple being in a thermal series configuration. However, the two terminals of the n block connect to differing but adjacent, p blocks.

This pattern is repeated hundreds of times per module, resulting in a few hundred n-type and p-type blocks.

Modern TEGs are typically created using bismuth telluride (Bi_2Te_3) due to its economic feasibility and relatively high efficiency at low temperatures [8]. High efficiency at low temperature gradients is critical for body-wearable applications, where the gradient is generally on the order of 2-4 degrees Celcius. Lead telluride ($PbTe$) and Uranium Dioxide (UO_2) are other researched alternatives [10, 11]. This work primarily utilizes Bi_2Te_3 modules.

1.3 Heat Sink Design

1.3.1 Background and Current, State-Of-the-Art Research

In order to maintain a working potential across a TEG, a heat sink is added to the system to ensure a finite heat flow through the module. Cold-side cooling may be accomplished in many ways. However, convection cooling utilizing the ambient air flow is the most common technique, especially for body-powered applications, where other means of cooling are difficult to incorporate.

Dimensional and material properties of the heat sink should be taken into careful consideration while designing a power-optimized TEG and heat sink system. This concept is further explored in Chapter 2. Current research in body-powered, TEG-based systems target low power applications with the intent of powering watches or other small applications. Figure 1.3 shows some examples of TEG-based wearable applications.

The head band in Figure 1.3 generates 2.5mW of power, translating into a power density of 20 $\mu W/cm^2$. The watches in the same figure generate 150 to 200 μW of power at 0.8 to 1.2V open-

Figure 1.3: Current TEG-based wearable applications

circuit voltage. Such power values may be used in running many micro-power applications including those targeted towards human vital monitoring, such as heartbeat sensors and pulse oximeters [9].

1.3.2 Wearable, Low Profile, 2-D Heat-Spreader

One of the major drawbacks of utilizing the TEG-based applications in Figure 1.3, apart from their minimal power output performance, is the relative thickness of the system as well as the weight of the system. In particular, the thickness of the system is on the order of tens of millimeters, with the headband being about 30mm and weighing about 2 pounds. Such a thickness is essential for this design due to the utilization of the typical, 3-D heat-spreading technique, where cooling is attained through extending as far away from the hot source as reasonably possible, thereby increasing the surface contact area with the ambient coolant. The watches also follow this trend and extend 20mm away from the cold-side. This poses many problems in ensuring comfortableness of the system when worn. Apart from this issue, the relatively small contact surface of the heat sinks and the lack of conformity pose issues in maintaining proper contact between the hot source and the TEG, which in turn results in output power fluctuations.

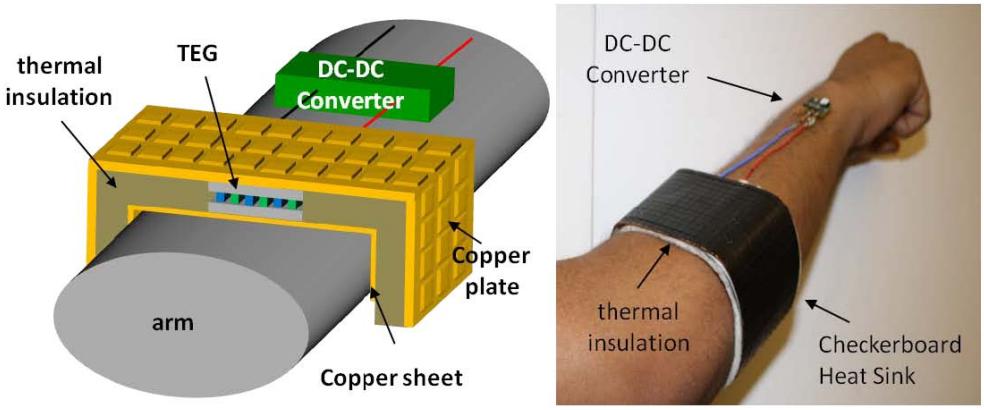


Figure 1.4: The wearable, wristband heat sink ensures that the system remain comfortable and effective. A model and image are shown [41].

The designed 2-D heat-spreading wristbands, shown in Figure 1.4, take these issues into account. Firstly, by limiting heat flow in only two dimensions (ie only along the contour of one's arm), a low profile is maintained. Additionally, by utilizing the large available surface area of the arm, the heat sink successfully maintains a working temperature differential comparable with that of current research. However, rather than extending more than 20mm away from the hot source, the 2-D wristbands have a thickness of under 5mm, which includes the thickness of the TEG. Additionally, a byproduct of utilizing a large surface area is the increased contact provided between the hot body and the hot-side of the TEG. Tests show that moving or rotating the arm yields minimal contact loss. The design choices and characterization of these heat sinks is further analyzed in Chapter 2. A comparison of the performance, variations, and dimensions of the systems in this work as well as in current research is summarized in Table 1.1. Notice that multiple cold-side groove patterns have been explored and tested. The groove patterns are illustrated in Figure 1.5 and their appropriate performances are listed in Table 1.1.

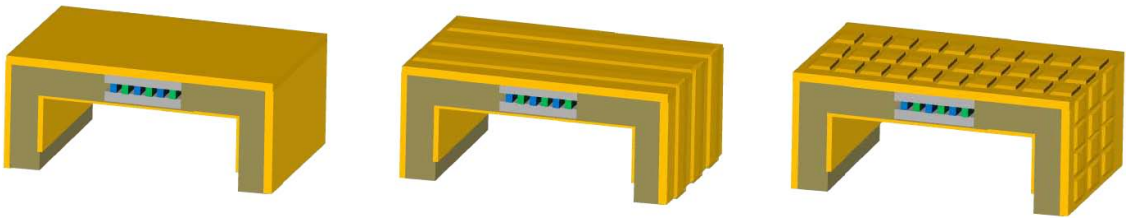


Figure 1.5: The flat(left), length-grooved(middle), and checker-board(right) heat sinks are illustrated.

1.3.3 Flexible, Stretchable TEG

The concept of 2-D heat-spreading extends beyond the wristband heat sink system introduced in Section 1.3.2. The design of a flexible TEG system, shown in Figure 1.6, allows for further leniency when approaching the concept of a universal energy harvesting system. More specifically, the dimensions of the wristband heat sink limited its use to those with appropriate arm widths. However, by designing a flexible heat sink, a wider range of individuals may comfortably wear the harvester. In addition, by cutting each individual TEG module into arrays with a width of two elements and placing them on interconnected "islands", a more uniform heat distribution across the cold-side heat sink is expected.

The design illustrated in Figure 1.6 parallels that of the wristband heat sink. However, the TEG module in the wristband is cut into arrays. These arrays, in turn, are coupled with a cold-side copper heat sink and a hot-side copper sheet for better contact in order to form islands. The hot-side copper sheet also contains electrical traces to series-connect the arrays. The various components of each

Name	**Open Circuit Voltage (mV)**	**Load-matched, optimum power(μW)**	**Power Density ($\mu W/cm^2$)**	**Heat sink system dimensions (L, W, H)**	**Reference**
Miniaturized thermoelectric generator for human body applications	150	0.0003	≈0.00173	≈4.5cm x 4.5cm x 2cm	[12]
Flexible Thermoelectric Generator for Wearable Biometric Sensors	160	0.00418	≈ 0.00019	0.7cm x 0.3cm x 500nm (thin-film)	[13]
Wearable Head-Band	–	2500	≈ 17	≈ 3cm x 30cm x 5cm	[14]
Seiko Thermic wristwatch	3000	30	≈ 26	≈ 5.5cm x 5.5cm x 2cm	[15]
Coin-size coiled-up polymer foil thermoelectric power generator	750	10	≈ 1.1	1cm x 1cm x 1cm	[16]
Checkerboard, wearable wristband heat sink	91	280	25.0	25.2cm x 6.4cm x 0.1cm	This work
Length, wearable wristband heat sink	82	215	19.4	25.2cm x 6.4cm x 0.1cm	This work
Flat, wearble wristband heat sink	80	190	17.6	25.2cm x 6.4cm x 0.1cm	This work
Flex TEG	20	11	0.13	17cm x 5cm x 0.1cm	This work

Table 1.1: Summary of TEG and heat sink system performance

island are thermally bonded using thermal paste. Each island is interconnected to adjacent islands through the utilization of flex traces [46]. These flex traces enable 1-D stretching along the length of the circuit. Notice from Figure 1.6 that the flex traces are bent in such a way as to allow the TEG islands to compress and expand. Initial tests of the designed flex TEG yielded stretching up to 30% of the original length. Each flex TEG contains three individual TEG modules, which were cut into arrays. This yielded matching thermal impedances between the modules and the heat sink. Current design shows a 20mV open-circuit voltage and approximately 40 μW of power. The design and performance of the flex TEG are further explored in Chapter 2.

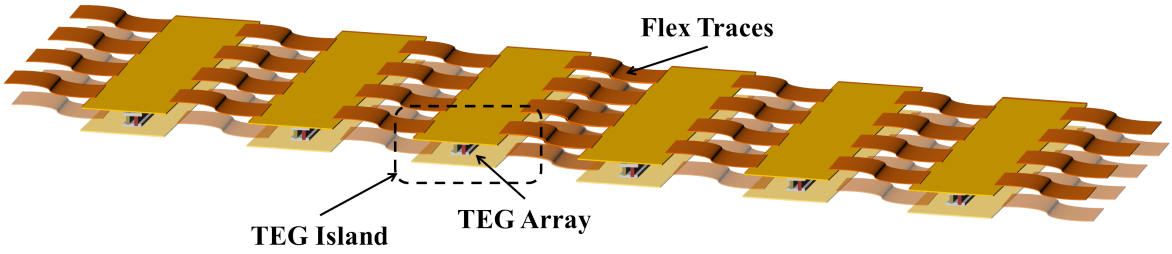


Figure 1.6: A model of the flex TEG is shown.

1.4 Applications

1.4.1 Motivation and Goal

Figure 1.3 showed some example systems utilizing body-powered TEG systems as the main supply. Applications targeted towards medical monitoring are of particular interest due to their power hungry nature and packaging advantages. This work details the creation of a body-powered, EKG acquisition and processing unit. A model of the system is shown in Figure 1.7. The overall system rests on the user's chest and contains not only 2-D heat-spreading TEG arrays for power, but also the EKG probes and processing circuitry.

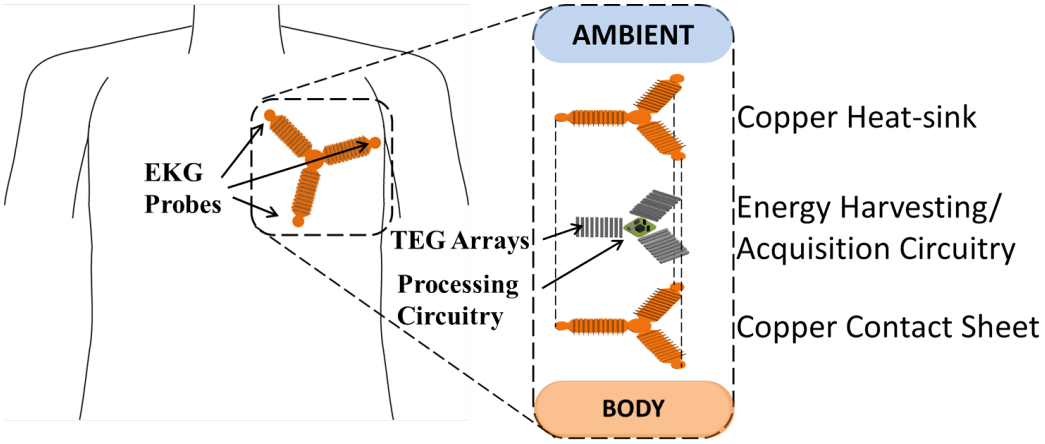


Figure 1.7: A model of the body-powered EKG acquisition system containing the various layers is shown.

1.4.2 EKG System

Overview

A high-level diagram of the processing circuitry as well as the TEG supply and receiver is shown in Figure 1.8. The processing circuitry contains a boost converter, EKG front-end circuitry, an 8-bit analog-to-digital converter (ADC), an ultra-low power Digital Signal Processor (DSP), and a wireless transmitter. The objective is to acquire one's EKG waveform from the front-end circuitry, digitize the signal using the ADC, perform simple processing in the DSP, and transmit the compressed data to a receiver connected to one's computer. In doing so, power is supplied to these blocks using only the body-powered TEG arrays. These sub-blocks will be individually analyzed in more detail below.

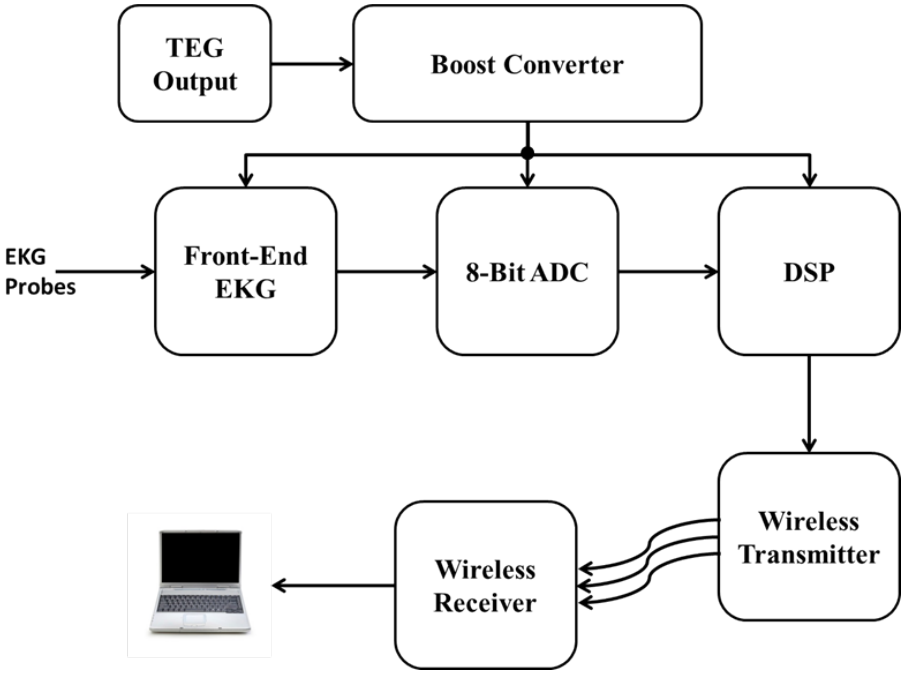


Figure 1.8: A high-level block diagram representation of the EKG acquisition system is shown.

Introduction to EKG

An EKG (Electrocardiography) is a tool to measure the health of ones heart. The various states of polarizations of the heart during a cardiac cycle yield measurable electrical signals on one's skin. The interaction between the four chambers of the heart results in a two-phase pumping action, known as diastole and systole. During the diastole phase, blood fills up the heart and during systole, this blood rushes to the bodys organs [9]. Each phase requires a unique set of actions to be performed by the four chambers of the heart. A byproduct of these actions is a noticeable potential difference

between differing parts of the body.

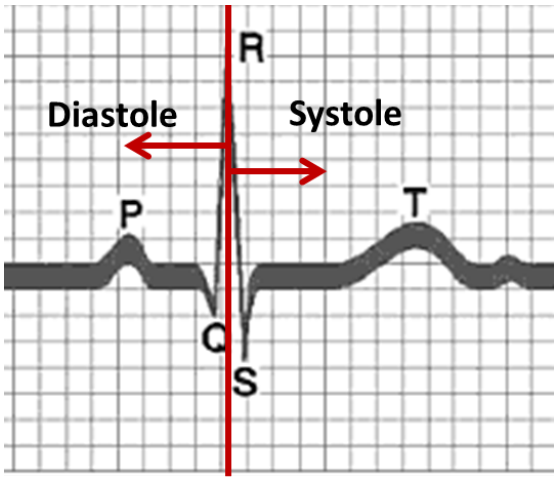


Figure 1.9: A sample EKG waveform with the two phases is highlighted.

A typical EKG waveform, shown in Figure 1.9, amplifies the difference in voltage between electrodes placed on the skin. Conducting gel is used to ensure proper contact and a stronger signal. The electrode locations are based on the dipole-like nature of the heart. Experimentation led to further accuracy in probe placement [18]. By strategically placing these probes and amplifying the resulting electrical difference, various stages of the EKG pulse may be observed. More specifically, every period of a pulse contains noticable P, Q, R, S, and T waves. These waves are generated due to some combination of the aortic and mitral valves opening or closing. By observing the duration and magnitude of these various waves, such medical issues as cardiac murmurs, seizures, arrhythmias, and cardiac dysrhythmias may be detected [24].

DC-DC Converter

The necessity of a DC-DC Converter becomes evident when handling sub-volt input supplies, which are prevalent in TEG-based applications. DC-DC Converters provide a means of using, say, a 100mV input voltage to drive analog and digital circuits by first boosting this input to an approximately usable 2.0V. By doing so, issues such as subthreshold leakage in digital circuits and inadequate linear range in analog circuits are avoided [31].

A simple, synchronous boost converter topology is shown in Figure 1.10, with the Supply providing a low input voltage and the Load seeing a higher output voltage. By varying the pulse width of the switch, current storage in the inductor and the following "discharge" into the capacitor produce

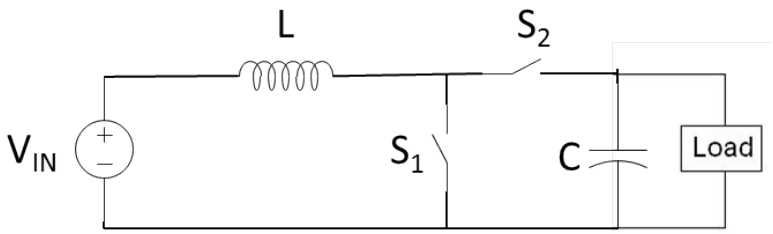


Figure 1.10: A basic boost, DC-DC Converter topology contains an inductor, switch, diode, and capacitor.

a dependent output voltage. More specifically, a boost converter's transfer functions is as follows:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}, \tag{1.4}$$

where V_{out} and V_{in} represent the high output voltage and low input voltage, respectively, and D is the duty cycle of the switch. With a duty cycle approaching one (switch is always closed), the inductor current continuously builds up and results in a V_{out} approaching 0V. As the switch opens, the current in the inductor is dumped onto the capacitor. The presence of the diode ensures that no back-current flows upon charging the capacitor.

Although functional, imperfections in the form of finite resistance in the inductor and capacitor as well as a non-zero voltage drop across the diode result in such a design being infeasible for high efficiency, low power applications. Modifications and additions have been made to this base design in order to ensure proper operation with a higher efficiency. Techniques such as cascading a boost converter followed by a buck converter yield better control over the output [32]. Additionally, incorporating digital control of the switch in both stage yield higher efficiencies and lower leakage. Table 1.2 shows the current state-of-the-art boost converters and their efficiencies.

The modified boost converter topology used in this research, which incorporate the modifications detailed above, is shown in Figure 1.11. The circuit contains multiple blocks serving to either control the output, or generate reference and clock signals. In this case, the $START$ block utilizes a mechanical actuator (switch $S1$) and at least a 35mV input voltage, V_{TH}, in order to begin generating the reference voltages and clock signals. The $STORAGE$ block takes the V_{TH} input and also a supply input, V_{DD}, in order to boost the output voltage, V_{STO}, up to a value higher than needed. The $DC-DCBUCK$ lastly bucks this V_{STO} down to output V_L. The presence of the buck

Name	Input Voltage (V)	Output Voltage (V)	Peak Efficiency (%)	Reference
Batteryless Thermoelectric Energy-Harvesting Interface Circuit	35mV	1.8V	58%	[32]
EnOcean ECT310	20mV-250mV	4V	30%	[33]
20mV Input Boost Converter	20mV	1V	50%	[34]
LT Ultralow Voltage Step-Up	20mV - 1V	2.2V	60%	This work, [35]
50mV Input Low Power Boost Converter	50mV	1.8V	60%	This work

Table 1.2: Summary of current research in ultra low power boost converters

converter ensures more accurate control of the output voltage, since

$$\frac{V_{out}}{V_{in}} = D, \tag{1.5}$$

rather than being inversely proportional to the duty cycle in the case of the boost converter.

EKG Front-End Circuitry

Current research in acquiring an analog EKG signal is detailed in Table 1.5. A majority of the work, including this work, relies on a two-stage amplifier topology. However, some of the front end amplifier research in Table 1.5 include work done on larger subsystems as well.

The Ultra Low Power EKG from Table 1.5 for this work utilizes a three probe, EKG front-end topology, shown in Figure 1.12. The probes, labeled Z_{left}, Z_{right}, and Z_{gnd}, are generally located on the left hand, right hand, and leg, respectively. However, for packaging convenience, the probes may be placed as shown in Figure 1.7. This front-end topology aims to not only amplify the differential voltage generated between the Z_{left} and Z_{right} probes, but also uses the Z_{gnd} probe to feedback and reject 60Hz common mode noise (shown in Figure 1.12 as v_{60Hz}). Due to the inherent high-impedance nature of the human body, 60Hz noise is especially prevalent. By using the Z_{gnd} probe as an active ground which feeds back into the body, a much cleaner differential voltage is observed [25].

A circuit-level schematic of the topology in Figure 1.12 is shown in Figure 1.13. The Signal Amplifier block contains two gain stages, with the first stage (composed of amplifiers M_1 and M_2

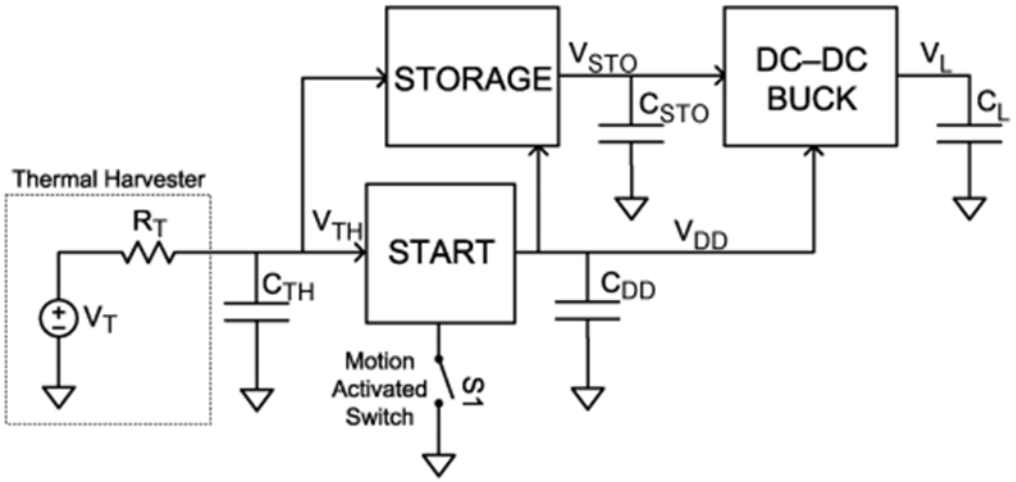


Figure 1.11: A 35mV input boost converter [32] is shown. Further discussion will continue in Chapter 4.

in Figure 1.13) performing differential amplification of the V_{in+} and V_{in-} probe inputs. The second gain stage, composed of amplifier M_3, further gains this differential signal. The output of the first stage passes through amplifier M_4, capacitor C_{11}, and a super buffer before being fedback through the body. This feedback path contains an integrator in the form of the C_{11} capacitor. The various amplifiers are designed as simple transconductance amplifiers with pmos current mirrors and nmos biasing transistors. Specifications for the front-end layout are shown in Table 1.4. The specifications were rendered in Cadence, using 600nm AMI CMOS processing. The layout characteristics are further explored in Chapter 4.

Analog-to-Digital Converter (ADC)

The interface between the DSP and the analog real world occurs through the ADC. By converting an analog waveform such as an EKG output into, say, an 8-bit digital bus, further processing of the data may occur using a microcontroller or Field-Programmable-Gate-Array (FPGA).

The Successive-Approximation-Register (SAR) ADC is generally the ideal choice for low power, high efficiency, and medium to high resolution applications and will be utilized in this work[36]. Table 1.5 shows the performance of current SAR ADC. Appendix B of this work looks further into the design and testing of a SAR ADC in 90nm processing.

Name	**Processing Technology**	**Operating Voltage (V)**	**Power (μW)**	**Reference**
Analog CMOS Processing Chip for ECG	0.35μ	3.3V	72.6μW	[26]
Sub-threshold Mixed-Signal ECG SoC	0.13μ	0.8V	2.6μW	[27]
Flexible SoC for Biomedical Signal Acquisition	0.35μ	3.3V	66μW	[28]
Micropower EKG	0.5μ	1.5V, 3V	2.1μW	[29]
Sensor Interface for Biomedical Applications	0.18μ	600mV, 1.2V, 1.8V	2.5 μW	This Work, [30]
Ultra Low Power EKG	0.6μ	2.1V	10μW	This Work

Table 1.3: Summary of current research in front-end, analog EKG circuits.

Table 1.4: A list of specifications for the extracted front-end schematic, designed in 600nm processing.

Common mode rejection	-60.89 dB
Differential Gain	42.96 dB
CMRR	103.825 dB
Noise	6.133 μV
Bandwidth	2.2 kHz
Power	4.587 μW

DSP and Transmitter

The DSP and Wireless transmitter used in this work are a part of the Chipcon family. The CC1111 is a system-on-chip (SoC) with a built-in microcontroller unit, memory, an RF Transmitter, and a USB controller. The microcontroller contains an 8051 core and various sleep modes. In addition, a supply passes through a voltage regulator before entering the SoC. Complete peripherals of the CC1111 are shown in Figure 1.15.

1.5 Power Management and Efficiency

The measured power budget from the wristband heat sink is approximately 300 μW at steady state. A major source of system optimization comes in the form of trade-offs between on chip processing plus compression and packet size transmission. More specifically, the issue of finding a balance between continuous data transmission with minimal on-chip processing and maximum on-chip processing with

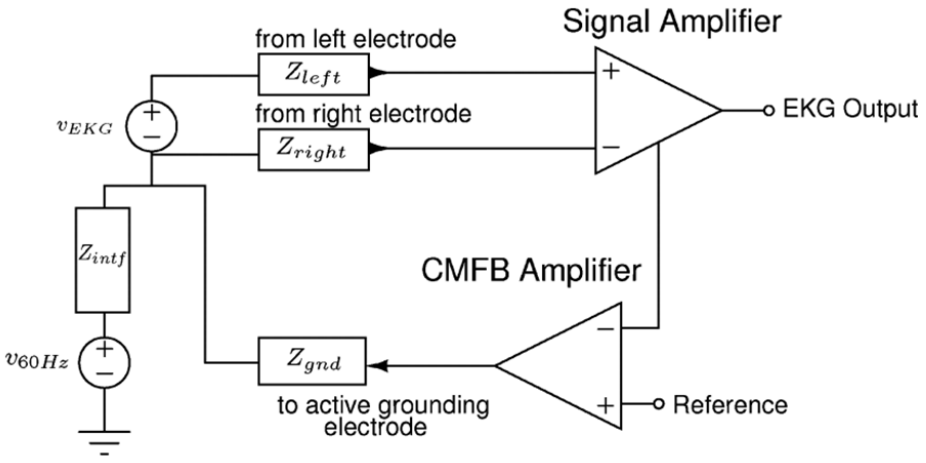


Figure 1.12: A sample EKG front-end topology is shown [19].

Name	**Analog Input Range (V)**	**Digital Output Resolution**	**Power Consumption**	**Reference**
SAR ADC for Distributed Sensor Networks	0 - 1V	8-bit	31 pJ/sample	[20]
12-bit Rate-resolution SAR ADC	0 - 1V	12-bit	200nW at 500 S/sec	[21]
Low Power SAR ADC for Bio-medical Applications	0 - 1V	8-bit	7.75 μW at 500 kS/sec	[22]
0.5V, 1 μW SAR ADC	0 - 1V	8-bit	0.85 μW at 4.1 kS/sec	[23]
8-bit Ultra-low Power SAR ADC	0 - 1.8V	8-bit	2 pJ/sample at 1.25 MHz	This work

Table 1.5: Summary of current research in front-end, analog EKG circuits.

minimal packet size transmission will be further explored in Chapter 4.

1.6 Thesis Organization and Contributions

The need for conformal, low-profile TEG-based heat sink systems is essential for maintaining comfortableness in not only energy harvesting but also in medical monitoring. By applying the concept of 2-D heat-spreading to create flexible TEGs and flexible EKG processing modules, patients and soldiers are better suited to using such self-sustaining applications. This thesis hopes to produce a viable alternative for heat sink design as well as body-powered applications of any sort. Chapter 2 begins by delving into the theory behind heat sink optimization through thermal impedance match-

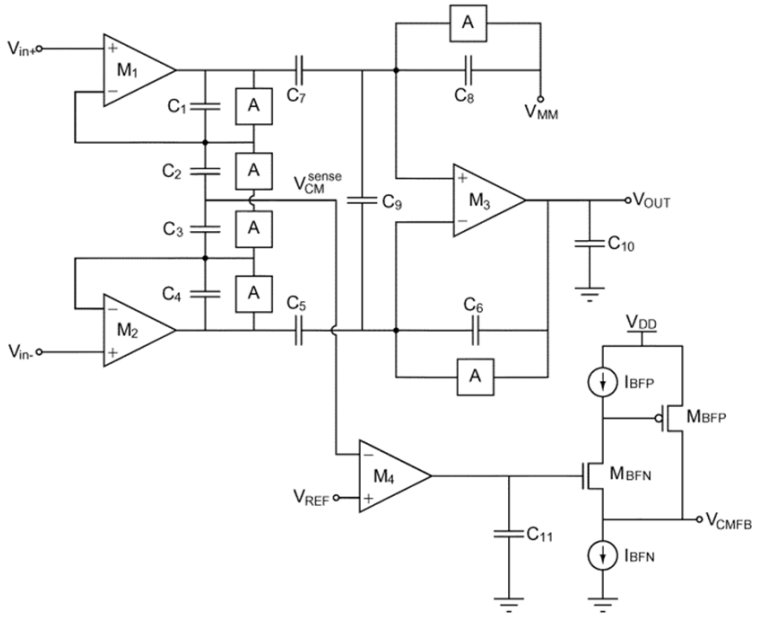


Figure 1.13: A detailed schematic of the three-probe EKG front-end circuit [19].

ing. This concept will be applied in determining the dimensional and material characteristics of the heat sink for the TEG. Additionally, the same concept will be applied in the design of the flexible TEG. Moving on, Chapter 3 will characterize not only the wristband heat sinks from Figure 1.5, but also the flexible TEGs. Both simulation data as well as experimental results will be shown. Chapter 4 applies the 2-D heat-spreading technique to the design of a flexible EKG patch, placed around the heart. Lastly, Chapter 5 concludes and provides possible future paths for this thesis.

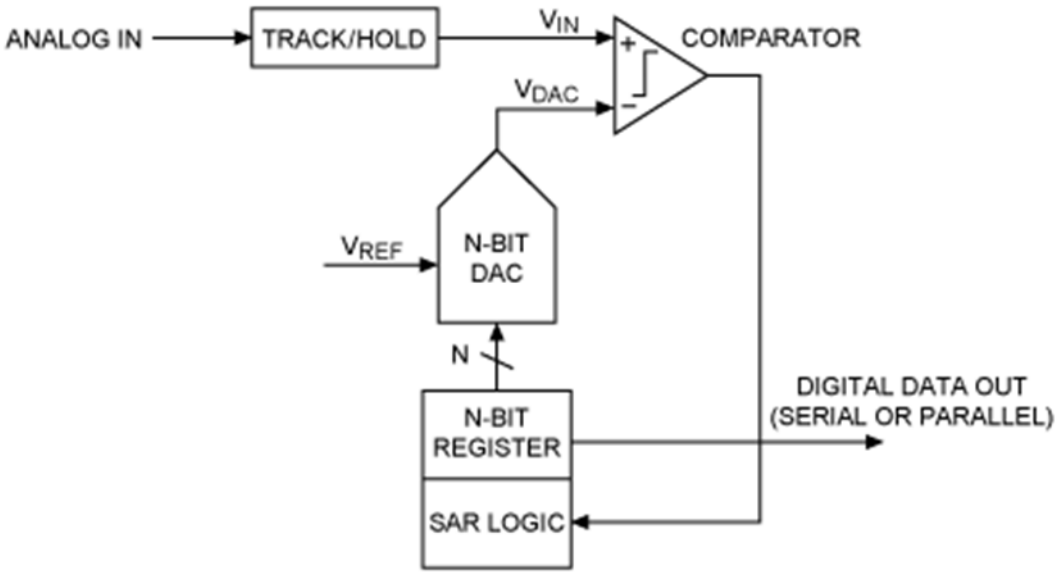


Figure 1.14: A simple Successive-Approximation-Register(SAR) ADC contains a comparator, SAR logic block, track/hold circuitry, and a DAC array.

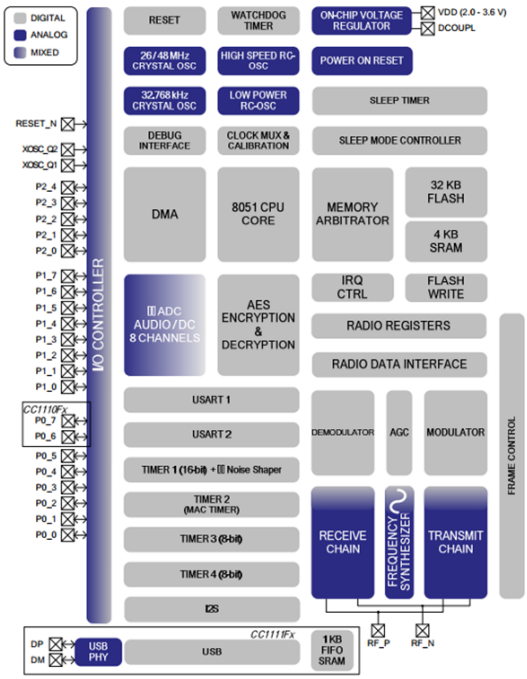


Figure 1.15: The CC1111 features and contents.

Chapter 2

Thermal Impedance Optimization and the Wristband Heat Sink System

2.1 Motivation and Organization

Current wearable, TEG-based systems, due to their minimal contact with the skin and large thickness, maintain a high profile when worn, which translates to a lack of comfortableness. Additionally, the minimal surface contact area poses issues when the body is in motion, yielding differing hot-side contact. This chapter introduces the theoretical models and experimental results obtained for the 2-D wristband heat sink. The chapter begins with an overview to the concept of thermal circuits, which is essential for setting up the theoretical models. Next, in Section 2.3, the thermal model of the 2-D heat sinks are introduced, taking into consideration the various approximations made to simplify the analysis. Additionally, the concept of heat sink optimization shall be applied in order to ensure a maximum power output in a "heat sink-limited regime". In Section 2.4, experimental setups and results for the various heat sinks will be detailed, with design limitations in mind and exploration into powering various load applications. Lastly, Section 2.5 will conclude by providing possible avenues for improvement and set a foundation to Chapter 3.

2.2 Introduction to Thermal Circuits

The integral form of Fourier's Law of thermal conduction yields a relationship between the heat flux through a body and the temperature difference across the body such that

$$\frac{\Delta Q}{\Delta t} = -kA\frac{\Delta T}{\Delta x} \tag{2.1}$$

where $\frac{\Delta Q}{\Delta t}$ is the heat flux, ΔT is the temperature difference, k is the thermal conductivity, A is the cross sectional area, and Δx is the length of the object. Ohm's Law is the electrical analogy to this expression and states that

$$i = \frac{\Delta V}{R} \tag{2.2}$$

where i is charge per time or current, R is the resistance, and ΔV is the voltage difference across the element. By studying Equations 2.1 and 2.2, it becomes apparent that the equivalent electrical analogy to thermal heat flux is current and the equivalent analogy to temperature difference is voltage. Notice also that the thermal resistance of a material is defined as

$$R_{thermal} = \frac{\Delta x}{kA}. \tag{2.3}$$

These principles may be applied to characterize thermal environments where multiple materials of differing characteristics are involved. For example, Figure 2.1 shows two separate materials within a composite slab where the heat flux, $\frac{\Delta Q}{\Delta t}$ or equivalently $\dot{Q}$, is conserved but a temperature difference exists between each material[38].

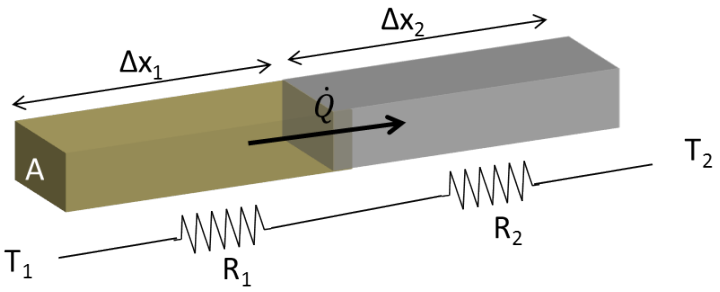


Figure 2.1: A composite slab containing materials of differing thermal conductivites.

The equivalent resistances, R_1 and R_2 are

$$R_1 = \frac{\Delta x_1}{k_1 A} \tag{2.4}$$

$$R_2 = \frac{\Delta x_2}{k_2 A} \tag{2.5}$$

and, with series resistances in mind, the relationship between the heat flux and temperature difference is

$$\dot{Q} = \frac{T_2 - T_1}{R_1 + R_2} \tag{2.6}$$

This example shows that a clear parallel exists between the electrical and thermal domains and the behavior of temperature gradients and heat fluxes is analogous to voltage and current.

2.3 Theoretical Analysis of 2-D Wristband Heat-Sink

2.3.1 Thermal Model

Similar to the composite slab, the TEG and wristband heat-sink system may be modeled as a series of resistances connected between two temperature sources, in this case that of the ambient and the skin. Figure 2.2 shows not only a cross-section of the various materials composing the system, but also the equivalent thermal circuit.

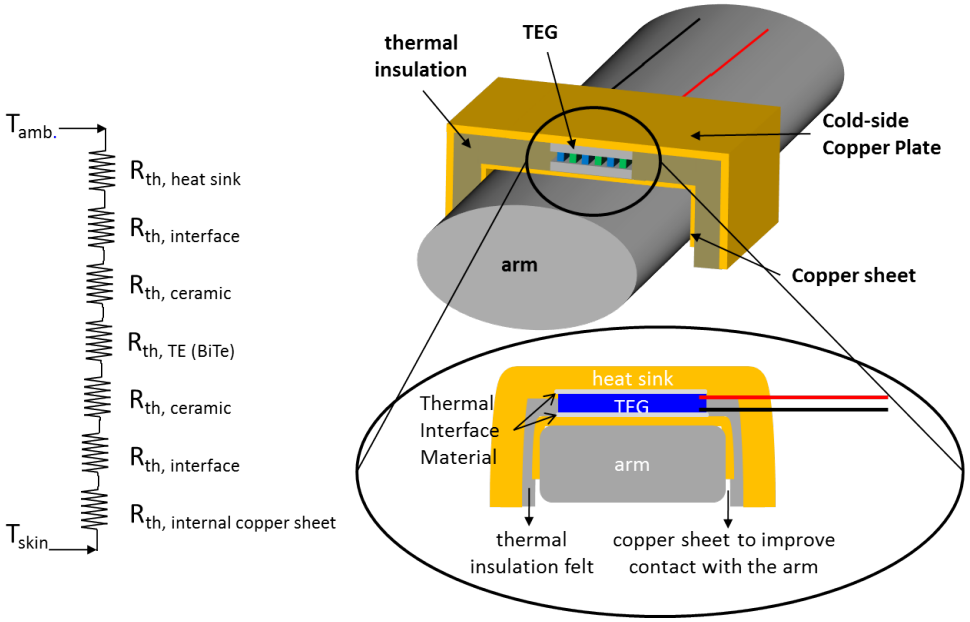


Figure 2.2: Thermal model of the TEG and wristband heat-sink system.

The wristband heat-sink system contains not only the top copper plate utilized for cold-side dissipation but also a thin copper sheet in contact between the hot-side of the TEG and the skin. The purpose of the cold-side copper sheet was experimentally determined to provide a better contact

between the rigid TEG module and the skin, and will be explored further in Chapter 3. The system also contains thermal interface material (TIM) in order to thermally adhere the copper with the hot and cold sides of the TEG. Lastly, the TEG itself is comprised of two ceramic plates sandwiching the Bi_2Te_3 elements. Each of these various layers is modeled by individual resistances beginning with $R_{th,heatsink}$ for the cold-side copper plate, then $R_{th,interface}$ for the TIM, $R_{th,ceramic}$ for the hot-side TEG ceramic, $R_{th,TE(BiTe)}$ for the TEG elements, $R_{th,ceramic}$ and $R_{th,interface}$ for the cold-side, and finally $R_{th,internal\ copper\ sheet}$ for the hot-side copper sheet.

Imperfect contact between any material boundary may be modeled with an appropriate interface conductance (or convection coefficient), h [39]. The relationship between the convection coefficient and thermal resistance is

$$R_{th,contact} = \frac{1}{Ah}, \tag{2.7}$$

where $R_{th,contact}$ is the thermal resistance of the contact surface, A is the cross sectional area (ie orthogonal to the heat flux), and h is the convection coefficient. In this case, a boundary exists between the cold-side heat-sink and the ambient environment. Revisiting the thermal circuit in Figure 2.2, the resistance of the heat-sink, $R_{th,heatsink}$, may be subdivided, as shown in Figure 2.3 into not only the thermal resistance of the copper plate, $R_{th,plate}$ but also the resistance attributed to the convection coefficient, $R_{th,cc}$.

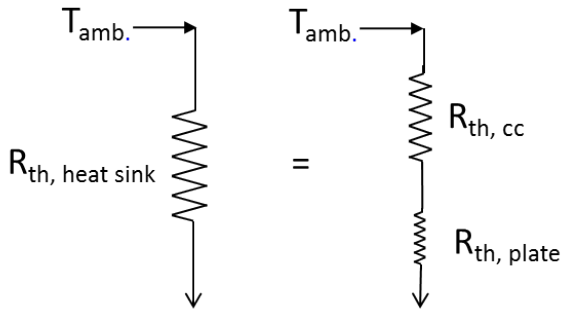


Figure 2.3: The heat-sink thermal resistance is composed of the plate and the boundary resistance.

Due to the relatively high thermal conductivity of copper, the heat-sink resistance is primarily composed of the interface component only. Thus,

$$R_{th,heatsink} = R_{th,cc} \tag{2.8}$$

Additionally, the thermal model in Figure 2.2 may be further simplified to contain only the $R_{th,heatsink}$ (or equivalently $R_{th,cc}$), and $R_{th,TEG}$. From Table 2.1, this is due to the relatively high thermal con-

ductivities of the copper sheet, ceramic plates, and TIM (ceramic-filled silicone) which, in turn, yield very low thermal resistances for these various components.

Material	**Thermal Conductivity** (W/mK)	**Specific Heat Capacity** (J/kgK)	**Density** (kg/cm^3)
Copper	350	385	8920
TIM	2.3	1714	2530
Ceramic	35	880	3698
Bi_2Te_3	1.6	154.4	7740

Table 2.1: Material properties used in calculating thermal resistances.

The various thermal resistances are quantified in Figure 2.4. The resistances are plotted with respect to the length of the Bi_2Te_3 elements. This is done to allude to the heat-sink optimization issue which will be discussed in the next section.

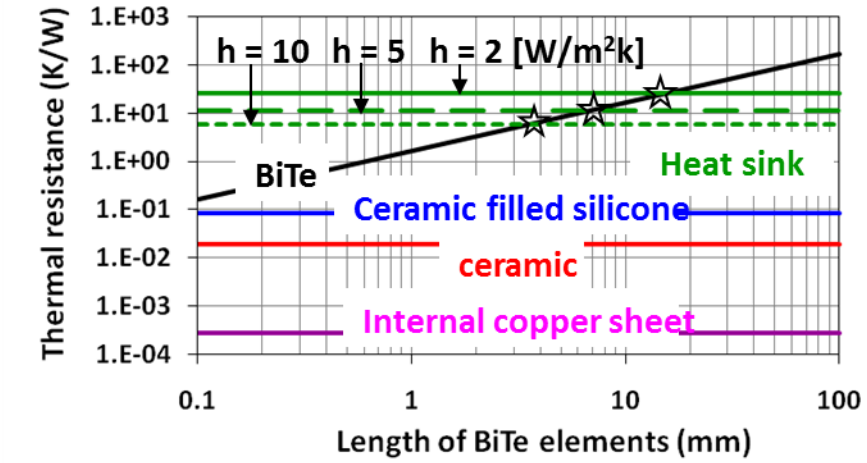


Figure 2.4: Simulation of thermal resistances of the various components of the heat-sink system as a function of BiTe element length.

Notice, in Figure 2.4, the linear relationship between the thermal resistance and the length of the Bi_2Te_3 elements. In addition, the heat-sink impedance varies inversely with the convection coefficient, h. Lastly, the relative resistances of the ceramic filled silicone (TIM), the copper sheet, and the ceramic places are more than two orders of magnitude below that of the heat-sink or TEG. As a result, they are ignored for simulation purposes.

To conclude, the original thermal model of the system from Figure 2.2 may be simplified to two resistances, as illustrated in Figure 2.5. The heat-sink resistance, dictated by the copper-air boundary, is a function of the convection coefficient, h, and the TEG impedance is dictated by the

length of the elements, L_{BiTe}.

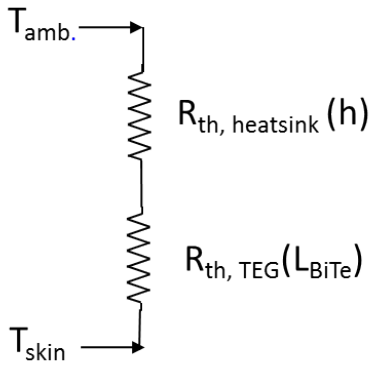


Figure 2.5: The simplified thermal model of the heat-sink system, for power optimization.

2.3.2 Power Optimization of the TEG and Heat-Sink System

Given a constant supply, V, an internal source impedance, R_{int}, and a load impedance, R_{load}, as shown in Figure 2.6, the maximum power delivered to R_{load} occurs when

$$R_{load} = R_{int} \tag{2.9}$$

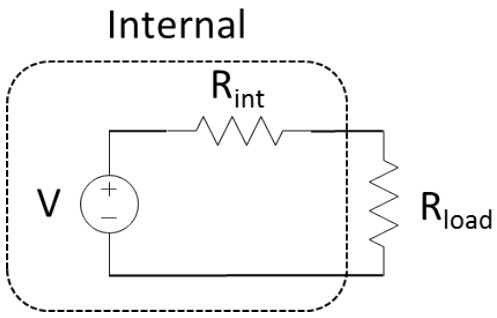


Figure 2.6: A voltage source with an internal impedance and load to show power optimization.

Similarly, from Figure 2.5, the heat-sink impedance may be viewed as an internal impedance and the impedance of the TEG may be the load. For optimum power from the TEG and assuming with a fixed heat-sink impedance, these impedances must match [40].

Thus far, optimization has occurred only within the thermal domain. However, operation of the TEG system in the electrical domain must be introduced before proceeding further. Figure 2.7 shows the system in entirety.

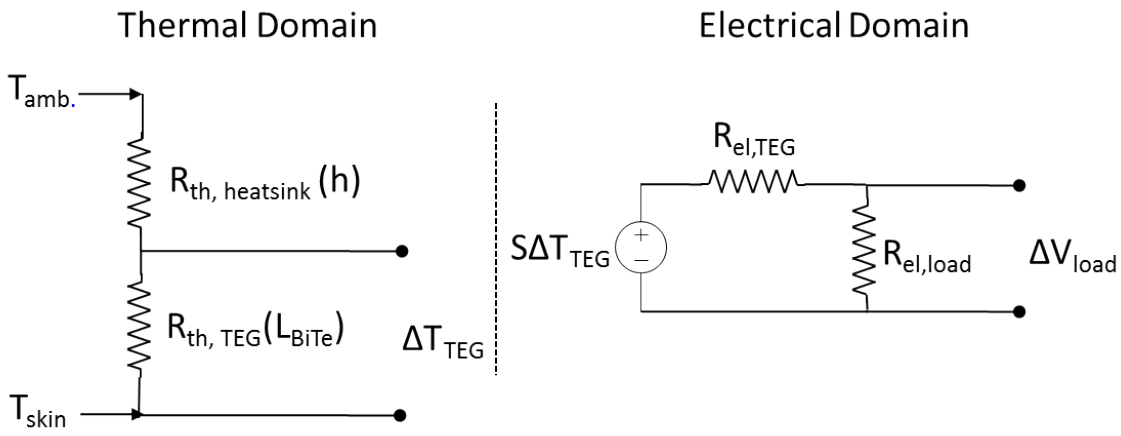


Figure 2.7: Thermal and electrical domains of the TEG and heat-sink system.

The conversion between the thermal and electrical domains is shown with a simple voltage supply, $S\Delta T_{TEG}$, where S is the Seebeck coefficient of the module. Due to the changing nature of $R_{el,TEG}$, which is directly proportional to the module length, and of $R_{th,TEG}$, which is inversely proportional to the module length, power optimization must occur within the electrical and thermal domains combined. More specifically, utilizing very long BiTe elements yields a large ΔT_{TEG}. However, $R_{el,TEG}$ will be significantly large, thereby providing a low output power to the load. On the other hand, making the elements short provides a small $R_{el,TEG}$. However, ΔT_{TEG} becomes small, yielding a small supply voltage. Approaching this more analytically, a "voltage-divider" exists between the ambient to skin temperature differential and the temperature drop across the TEG. If we assume

$$\Delta T = T_{skin} - T_{amb.} \tag{2.10}$$

Then,

$$\Delta T_{TEG} = \frac{R_{th,TEG}}{R_{th,heatsink} + R_{th,TEG}} \Delta T \tag{2.11}$$

$$\Delta V_{load} = S\Delta T_{TEG} \frac{R_{el,load}}{R_{el,TEG} + R_{el,load}} \tag{2.12}$$

$$= \frac{R_{el,load}}{R_{el,TEG} + R_{el,load}} \frac{R_{th,TEG}}{R_{th,heatsink} + R_{th,TEG}} S\Delta T \tag{2.13}$$

The power delivered across the electrical load, $R_{el,load}$, is thus,

$$P_{el,load} = \frac{\Delta V_{load}^2}{R_{el,load}} \tag{2.14}$$

$$= \frac{1}{R_{el,load}} \left(\frac{R_{el,load}}{R_{el,TEG} + R_{el,load}} \frac{R_{th,TEG}}{R_{th,heatsink} + R_{th,TEG}} S\Delta T \right)^2 \tag{2.15}$$

$$= \frac{R_{el,load}}{(R_{el,TEG}+R_{el,load})^2}\frac{R_{th,TEG}^2}{(R_{th,heatsink}+R_{th,TEG})^2}(S\Delta T)^2 \tag{2.16}$$

From the material characteristic values from Table 2.1 and 2.2, a sweep of the power density may be performed given a particular TEG length.

Material	**Thermal Conductivity** (W/mK)	**Seebeck Coefficient** $(\mu V/K)$	**Electrical Conductivity** $(1/\Omega/m)$
BiTe [42]	1.47	240	73700

Table 2.2: Material properties for BiTe.

The results of the simulation for multiple convection coefficients are shown in Figure 2.8.

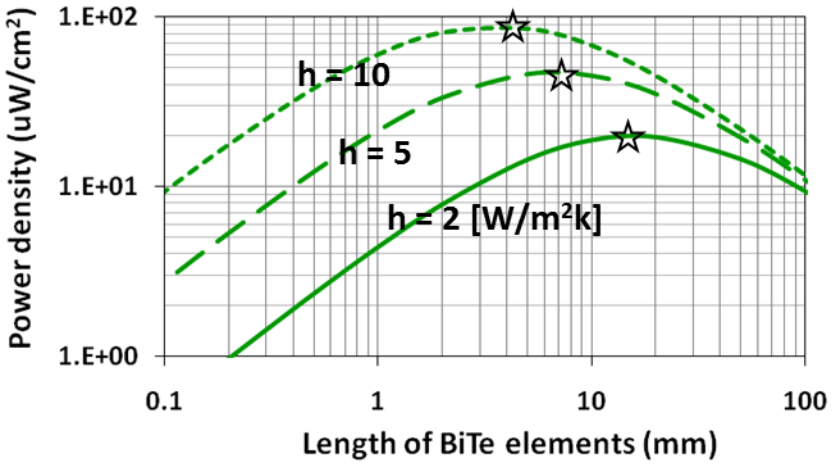


Figure 2.8: Output power density of the TEG given particular lengths of the BiTe elements [41].

The maximum power density, indicated with a star in Figure 2.8, is achieved when the thermal resistance of the heat-sink equals that of the TEG. This is equivalent to saying that the same temperature differential exists between the heat-sink and the TEG [43, 44]. Notice also that this optimization step, that is, matching the resistances of the TEG and heat-sink, occurs in a heat-sink limited regime. More specifically, only upon optimizing the heat-sink design to provide the highest convection coefficient, h, should thermal resistance matching occur. This is explored further in the next section.

2.3.3 Convection Coefficient Maximization and Simulation Results

The convection coefficient, or heat transfer coefficient, as introduced earlier, is used to model heat transfer between materials of differing phases [45]. It is characterized as follows

$$h = \frac{Q}{A\Delta T}, \tag{2.17}$$

where Q is the heat flow, A is the surface area, and ΔT is the temperature difference. Since the power output from the TEG, from Equation 2.16, is inversely proportional to ${R_{th,heatsink}}^2$, minimizing the heat-sink impedance should be the first priority. Since the heat-sink resistance density is inversely proportional to the convection coefficient, from Equation 2.7, it is desirable to make h as large as possible. The only controllable means of doing so is to increase the surface contact area, A.

Three different designs with varying surface areas were explored, both through simulations as well as through experimentation. We focus now on the simulation results and explore the experimental results in Chapter 3. The three patterned designs for the cold-side heat-sink are shown in Figure 2.9. The thickness was maintained at 1mm for all designs. This ensured that the system was low-profile

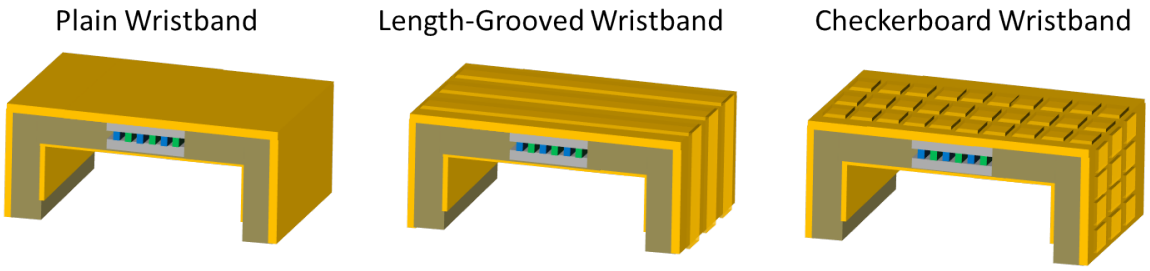


Figure 2.9: Patterned designs for maximizing the convection coefficient.

and comfortable when worn. Additionally, the surface area in contact with the arm was held constant with dimensions of 29 cm x 6 cm. However, the cold-side surface area was modified through the utilization of unidirectional length grooves as well as bidirectional checkerboard grooves.

With grateful assistance from Dr. Katey Lo, finite-element analysis was performed on the three designs in order to accurately characterize the temperature distribution on the cold-side. The design assumed a temperature differential of $10°C$, with the skin temperature at $33°C$ and the ambient temperature at $23°C$. Natural air convection, with $h = 5W/m^2K$, was applied to the cold-side copper heat-sinks. The results are shown in Figure 2.10.

The checkerboard wristband, with an increased surface area, did yield a lower thermal resistance as seen with the lower temperature differential. Studying just the plain wristband system, it can be seen from Figure 2.11 that less than half the temperature between the ambient and the skin drops

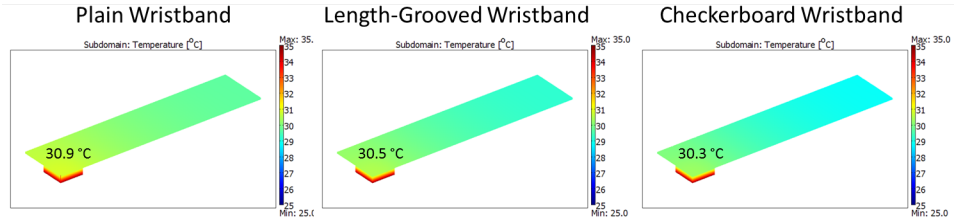


Figure 2.10: Finite-elements results for the differing surface areas.

across the TEG, yielding the conclusion that a better heat-sink with an increased surface area and better convection coefficient was necessary. Figure 2.11 takes advantage of the symmetric nature of the TEG and heat-sink system by simulating only one quarter of it. Similar temperature behavior is expected throughout the entire system.

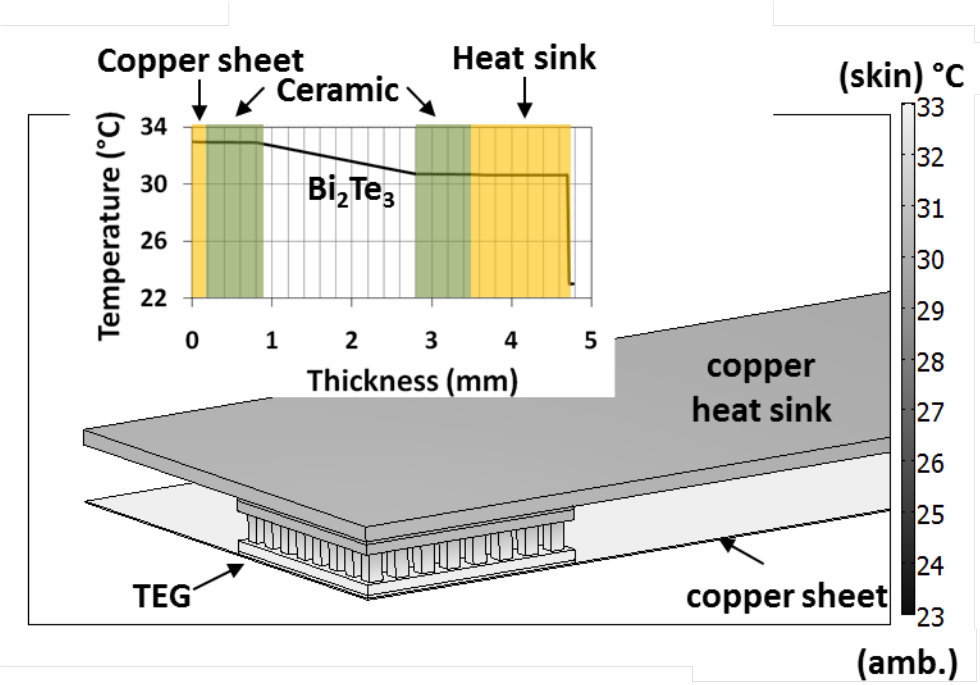


Figure 2.11: The temperature distribution of the plain heat-sink design.

Initially, the temperature gradient across the TEG will be maximal due to the smaller effective heat-sink impedance. However, at steady-state (which, experimentally, was approximately 7-10 minutes after wearing the heat-sink), the performance was greatly hindered due to the poor convection coefficient of the heat-sink.

Exploring the geometry of the various groove patterns, analyses have been performed relating the open-circuit output voltage to the pitch of the grooves. The pitch, illustrated in Figure 2.12, is the length of the protruding copper in between the machined grooves.

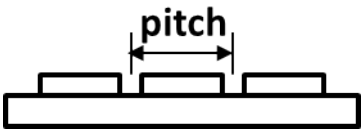


Figure 2.12: The pitch of the length-grooved heat-sink.

By increasing the pitch, the relative surface area in contact with the ambient is decreased. As a result, a lower output voltage is expected. Indeed, this is what is observed and shown in Figure 2.13.

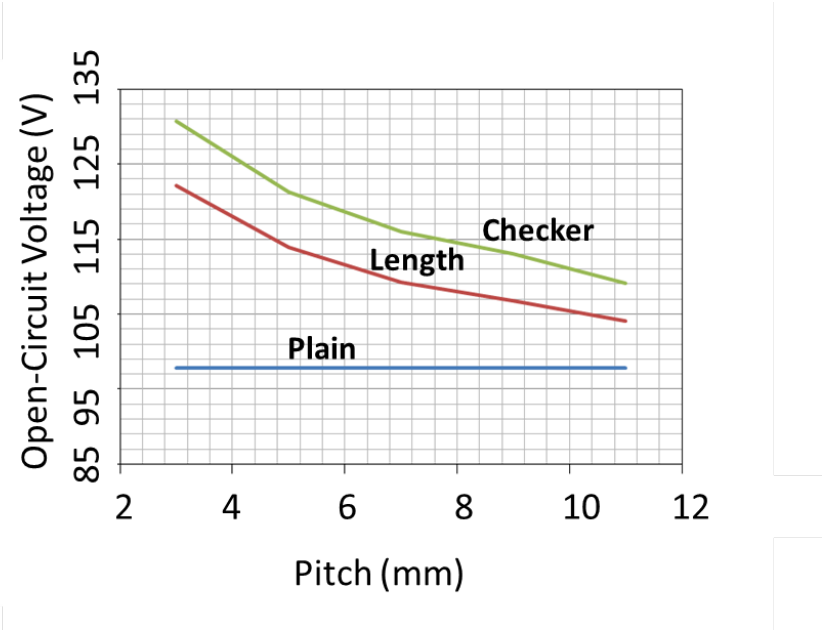


Figure 2.13: The output voltage was reduced by increasing pitch due to a decrease in surface area.

2.4 Experimental Procedure and Analysis

2.4.1 Fabrication

The prototypes in Figure 2.9 were fabricated utilizing copper with 1 mm thickness. The length and width were standardized for all designs to be 29.2 cm x 6.4 cm. Upon cutting the copper plates to this dimension, patterned grooves were made to one side. In order to generate the various groove patterns, a milling machine was used. The end-mill bit dimension, which controls the diameter of the grooves, was held constant at 0.5 mm for all variations of patterns. The pitches were varied from 5 mm to 9 mm. However, structural limitations of the copper led to a practical limit of pitch to 5 mm only. Surpassing this limit frequently led to the patterned copper plate snapping off into multiple pieces when being shaped. The shaping of the flat copper plate into a circular wristband was done

with a roller. The plates were fed into the roller multiple times, with each pass curving the plate more and more. The rolling was complete after the left and right ends of the plate were roughly 3 cm apart. However, the circular shape of the cold-side copper plate posed issues with regards to contact with the TEG, as shown in Figure 2.14.

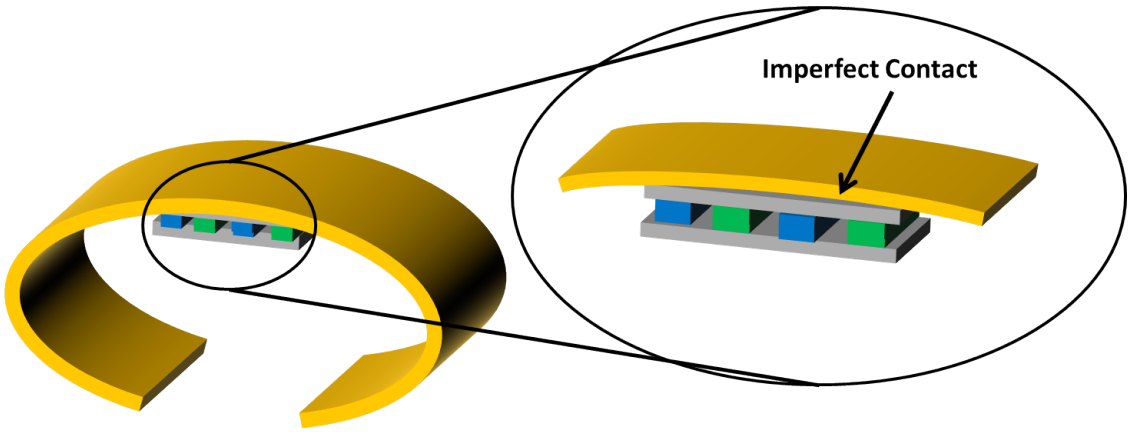


Figure 2.14: The completing of the rolling process yields circularly shaped wristband, with imperfect contact between the TEG and cold-side plate.

The large spacing between the ceramic and copper would require extensive use of the thermal interface material. This posed issues by adding to the thermal parasitic resistances and yielding a lower power output from the TEG. Rather, before the TEG was mounted to the heat sink, a press was used to flatten the area surrounding the contact region, as shown in Figure 2.15.

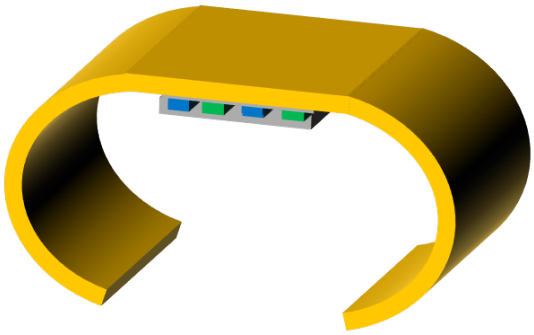


Figure 2.15: The press flattened the contact area surrounding the cold-side of the TEG.

A small aluminum block with dimensions slightly larger than that of the TEG was used as the foot-print for the press. The result was a much flatter surface which required less thermal interface material to thermally connect the TEG and copper.

Upon cutting, grooving, shaping, rolling, and pressing the copper plate, thermally insulating felt was appended to the underside of the plate using a strong bonding adhesive. The flat area of the

heat sink where the TEG rests, was left exposed with no insulating material.

Recall from Figure 2.2 that the thermally insulating felt was required to constrain heat flow through the TEG. Tests were performed to characterize the material and ensure an adequate thermal impedance. Figure 2.16 shows the set up to characterize the felt.

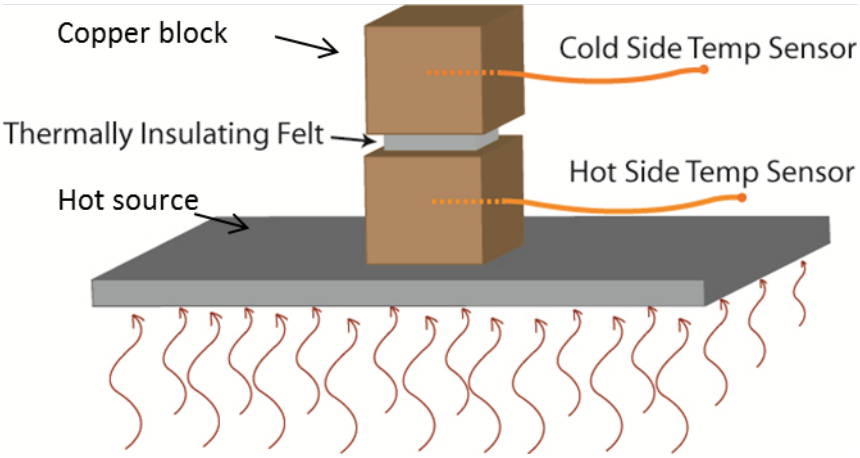


Figure 2.16: Test set up to characterize the thermally insulating felt.

The felt is placed in between two copper blocks, where one block is in contact with a hot source (hot plate). Thermocouple temperature sensors are placed in small holes drilled in the blocks. Thermally conducting paste is applied to provide the best thermal contact possible. The sensors are placed inside the blocks to ensure as accurate a temperature measurement for the hot and cold sides as possible. The results of this test, as well as a test replacing the hot source with a human arm itself, are shown in Figure 2.17.

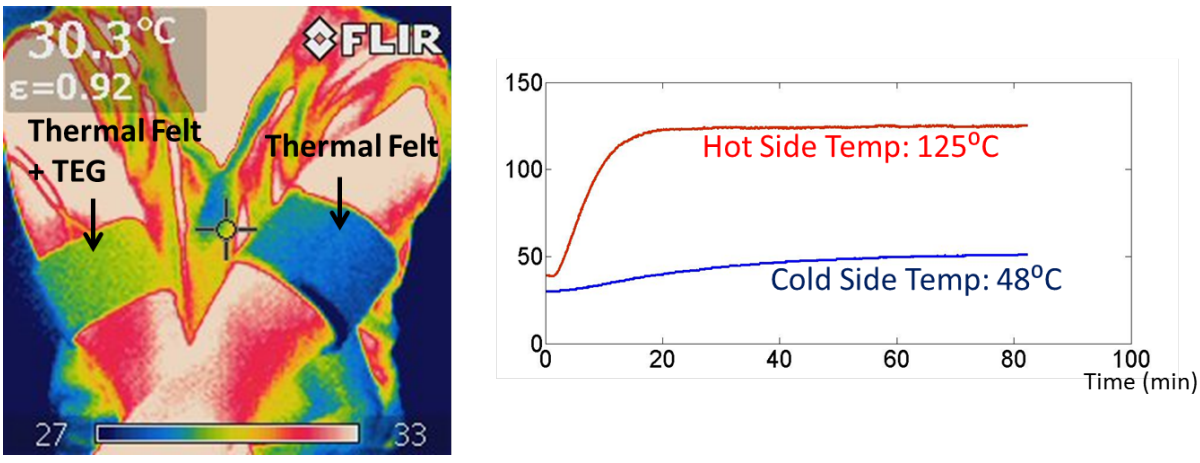


Figure 2.17: Characteristics of the thermal felt when placed on the arm, left, and on the hot plate, right.

The IR image in Figure 2.17 contains two heat sinks, with one containing the felt plus TEG and

the other replacing the TEG with more felt. Not only does this show that the heat flux is indeed constrained to pass through the TEG with the felt providing thermal isolation, but also that 2-D heat spreading is being utilized as seen with the even temperature distribution on the cold side copper of the felt plus TEG-based heat sink. The insulating properties of the felt are further characterized in the hot and cold side temperature plot in Figure 2.17. Here, with a hot side temperature of 125°C in the bottom copper block, a cold side temperature of 48°C is maintained in the top block. The test was performed over the course of 85 minutes, giving adequate time to attain steady state behavior.

Upon adhesively bonding the thermal felt to the cold side copper plate, a thin layer of TIM (thermal interface material) was used to thermally connect the TEG with the copper. A second layer of TIM was applied to the hot side ceramic, which in turn was connected to a thin copper sheet. This hot side copper sheet spread along the underside of the felt and TEG and ensured a higher thermal contact between the skin and hot side, even when the arm was in motion.

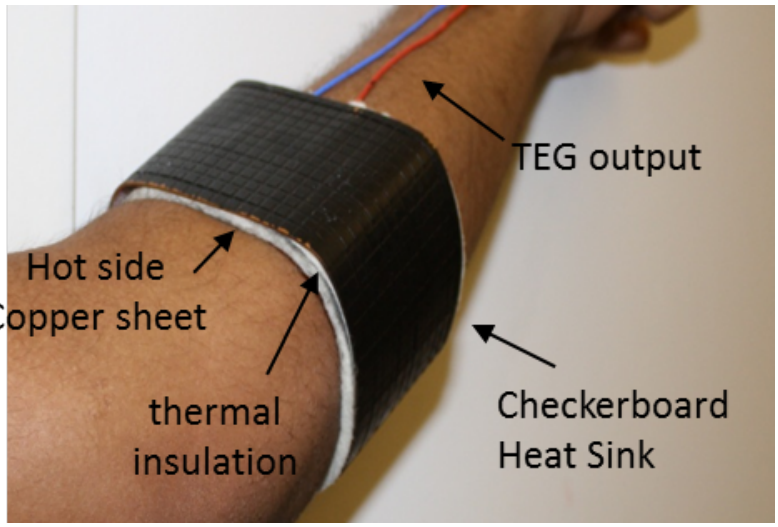


Figure 2.18: The completed checkerboard heat sink is shown.

A fabricated design for the checkerboard heat sink is shown in Figure 2.18. The cold side copper plate was painted black in order to more accurately characterize the temperature distribution using an IR camera. Copper's high reflective index would have yielded an incorrect temperature measurement. By painting the heat sink black, the effective index decreases and results in the IR image from Figure 2.17.

2.4.2 Tests and Results

Open-Circuit Voltage and Optimum Power Characterization

Tests were performed comparing the plain, length grooved, and checkerboard heat sinks. These tests were performed in controlled ambient temperature settings with minimal air flow for natural convection. In all cases, the heat sinks were placed on the upper forearm, similar to that shown in Figure 2.18. All voltage measurements to characterize the output of the TEG were done with a voltage data logger, capable of 1 mV resolution. Additionally, the hot and cold side temperatures were measured with temperature sensors, similar to that used in Figure 2.16, with 0.5°C resolution.

The first series of tests performed were transient experiments, measuring the output voltage of the various heat sinks plus TEG systems. The results are shown in Figure 2.19.

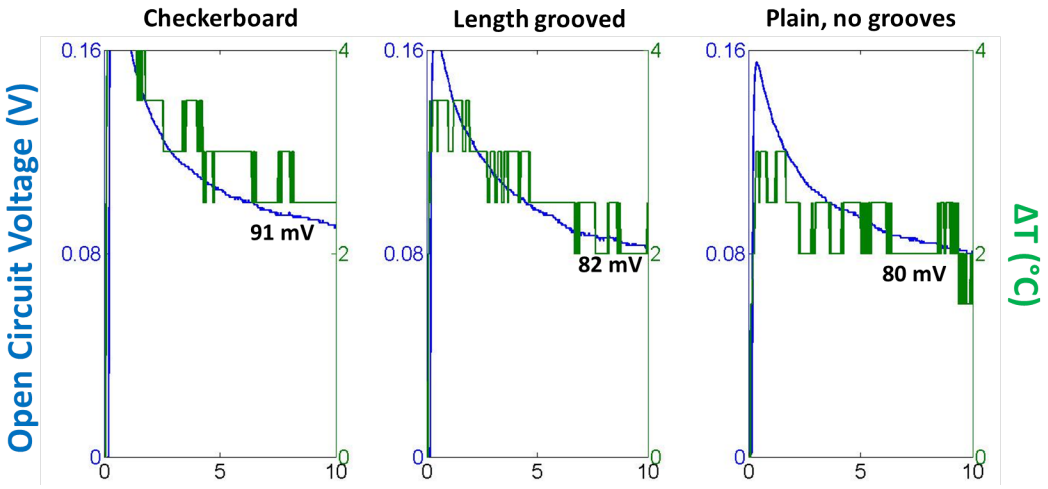


Figure 2.19: The output voltage for the various heat sinks plus TEG systems as a function of time.

The trend of results in Figure 2.19 match that of the simulations introduced in Section 2.3. In particular, due to the larger surface area in contact with the cold side ambient of the checkerboard heat sink, a higher open-circuit voltage is expected. The length grooved was predicted to do slight worse than the checkerboard but better than the plain. This prediction is matched in the experimental results in Figure 2.19 as well.

The optimum power output from the TEG given an electrical load match is shown in Figure 2.20. Notice that other designs, besides the checkerboard, length, and plain were tested. More specifically, the $\frac{1}{2}$-dense checkerboard design was included, which doubles the length and width spacing between adjacent grooves. Additionally, grooves along the width of the heat sink were also made. The output behavior of the width and length heat sinks are expected to be the same due to the constant spacing of the grooves yielding the same effective cold-side surface area.

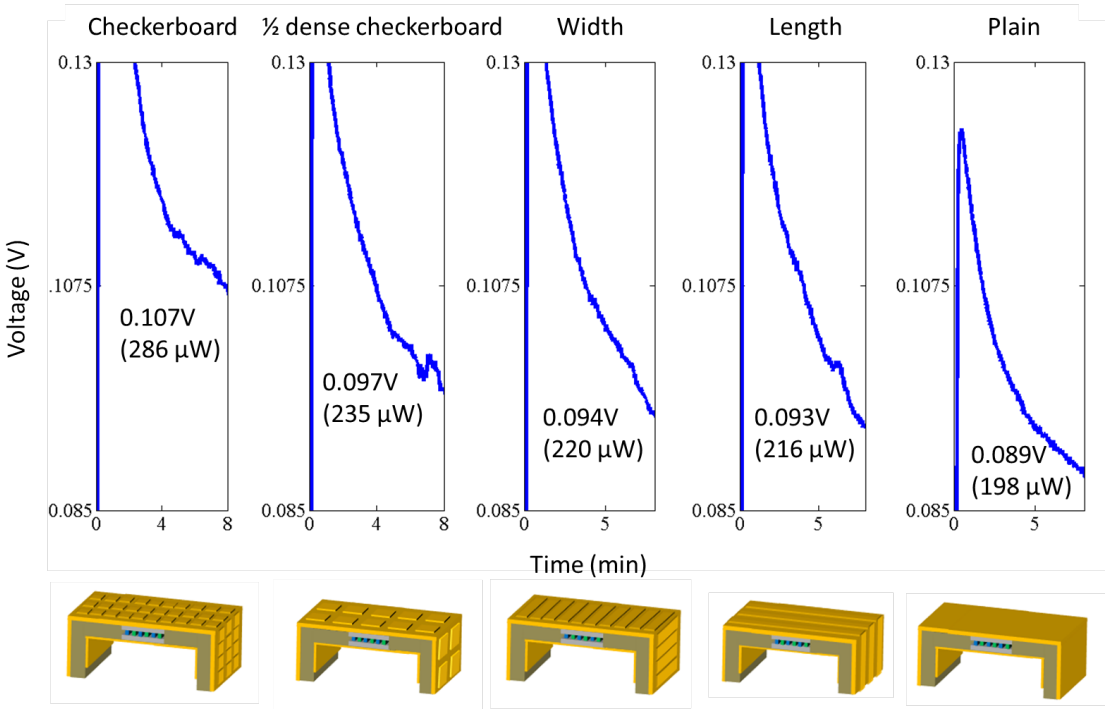


Figure 2.20: The optimum power output was measured by connecting a 10Ω resistor as the output electrical load.

For the power experiments, the load impedance was fixed at 10Ω. Thus, with this fixed load, the voltage across the load was measured with the data logger, and the power was calculated based on the following.

$$P = \frac{V^2}{R} \tag{2.18}$$

Notice, again, that the performance trend matched the predicted model introduced in the previous section, with the checkerboard heat sink providing the maximum power density of $25\mu W/cm^2$ at 3.5°C, the length grooved following at $19.4\mu W/cm^2$ with 3°C, and the plain at $17.6\mu W/cm^2$ with 2.5°C. In all cases, the tests were run for approximately 8 minutes.

Field Test

The checkerboard heat sink system was used as the power supply for various load applications, such as DC/DC converters, wireless transmitters, and laser diodes.

To begin, more characterization of the checkerboard heat sink system was done beyond that shown above. More specifically, a field test was performed, where the TEG output was connected to a 20mV input threshold DC/DC Converter, which was a part of the EnOcean Thermal Energy Harvesting Kit, as shown in Figure 2.21 [33].

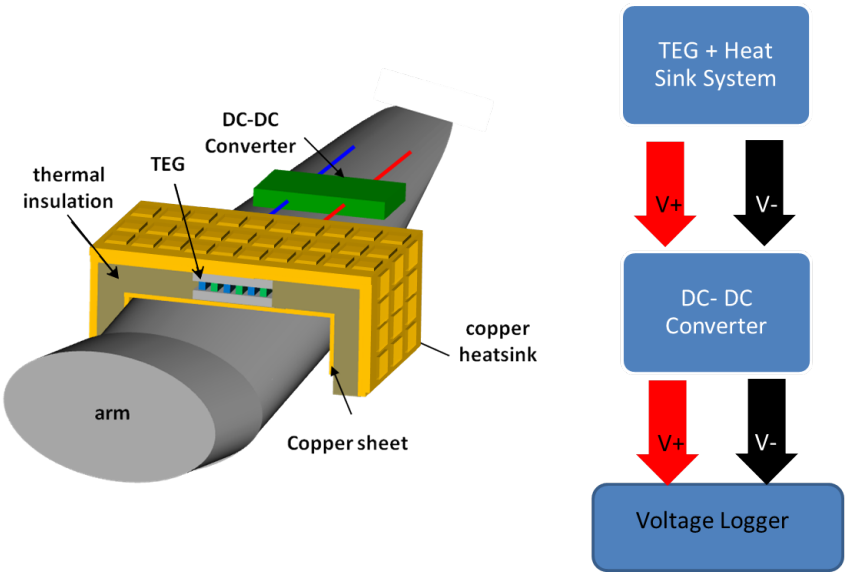


Figure 2.21: The setup for the field test used a commercial DC/DC Converter as well as a voltage logger.

The DC/DC converter is a completely stand-alone unit, requiring no external transformers or capacitors. The start-up voltage for the device is 20mV and the boosted output, open-circuit voltage is approximately 4.15V. The maximum efficiency of the device is approximately 35%. Figure 2.22 shows an 80-minute field test, where the output of the checkerboard heat sink plus TEG was connected to the input of the DC/DC Converter. The hot and cold side temperatures of the heat sink were recorded as well as the input and output voltages of the DC/DC Converter.

Figure 2.22 also shows the states of the ambient environment during the 80 minutes (ie "Walking Outdoors", "Walking Indoors", etc.). During the "Walking Outdoors" phase, a relatively high air convection is observed, thereby yielding a higher average output voltage from the TEG. On the other hand, during the "Sitting Indoors" phase, not only was the effect of air convection minimal, but the cold-side ambient temperature was hotter. This yielded a slightly lower output voltage. Yet, even with these fluctuations in the input, the DC/DC Converter's output was relatively constant at 4.15V. Although a higher ripple was observed during the "Walking" phases, the overall average was maintained above 4V at all times.

Output Loads and Applications

The output of the DC/DC Converter and TEG, as it was providing a consistent voltage above 4V, was connected to various loads including LEDs as well as the EnOcean wireless transmitter and receiver system.

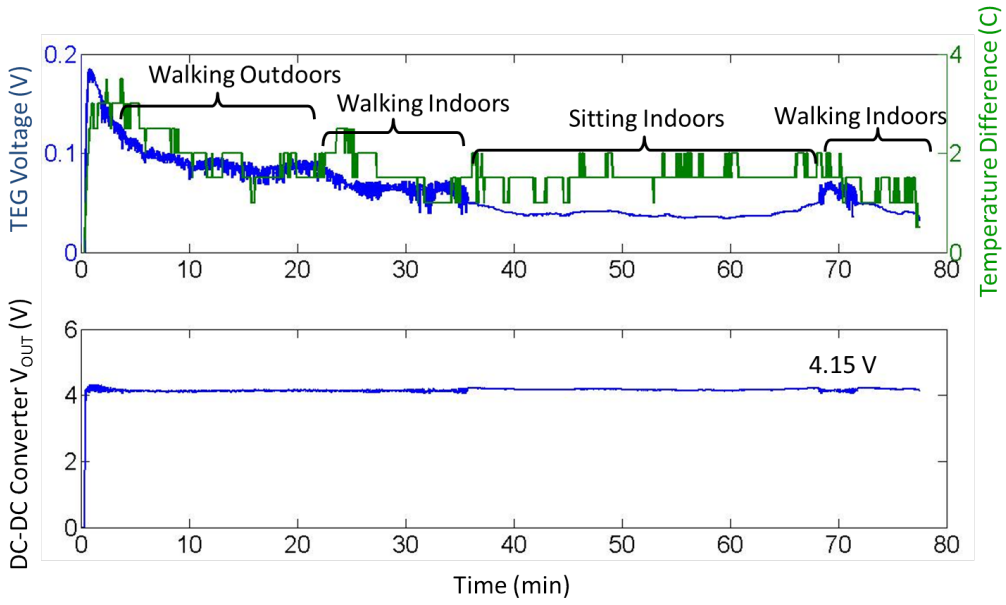


Figure 2.22: The data collected from the 80-minute field test shows not only the TEG output (also the DC/DC Converter input), but also the ΔT of the TEG and the output of the DC/DC Converter.

LED Load To begin, a simple LED load was connected, as shown in Figure 2.23 and its optical characteristics were studied. From Figure 2.23, the LED is visibly illuminated at steady-state (or 10 minutes after the heat sink was worn). In this case, the checkerboard heat sink was used as the power supply.

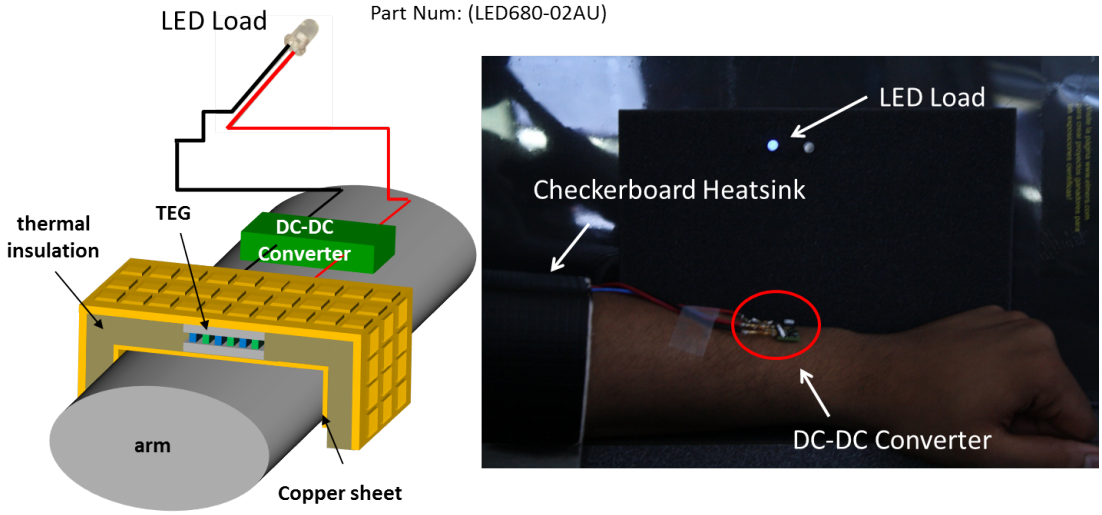


Figure 2.23: A model and image of a body-powered LED system are shown.

Figure 2.24 shows quantified results of the test. The power output from the LED was measured using an optical power meter interfaced with MATLAB in order to record the transient data. The

voltages from both the DC/DC Converter as well as the TEG were recorded with the data logger. Lastly, the temperature differential was recorded using the temperature sensors.

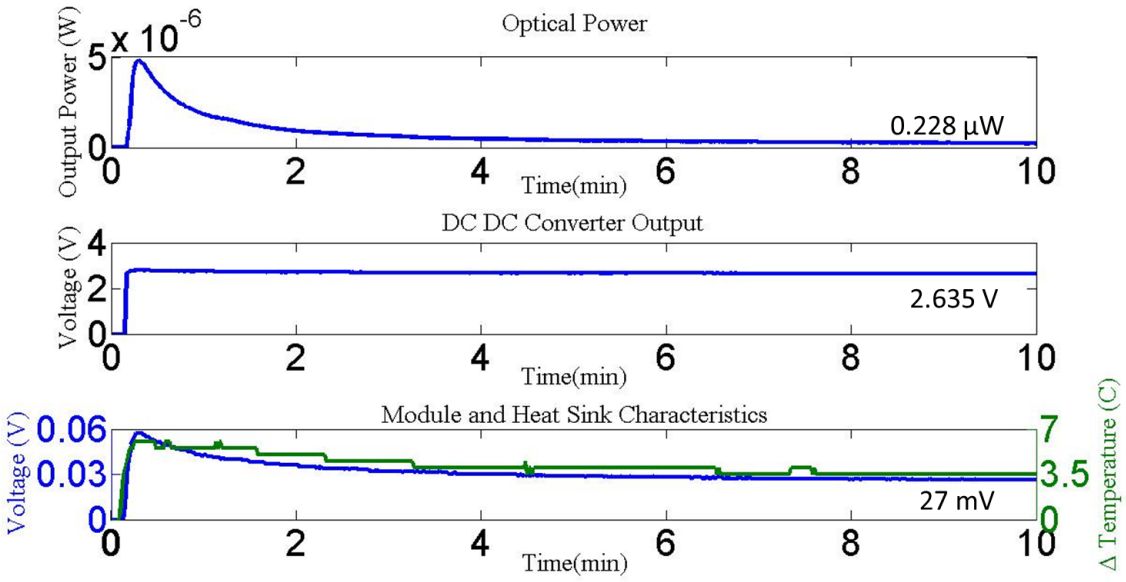


Figure 2.24: The quantitative characteristics of the LED-loaded DC/DC Converter output are shown, along with the DC/DC Converter output as well as the TEG voltage output and temperature differential.

The steady-state power output was approximately 0.228μW, with the DC/DC Converter's output and LED input at 2.635V. Due to the finite resistance of the LED, a voltage drop from 4V to 2.6V is observed at the output.

Wireless Transmitter Load The STM110 and the EVA120 boards from the EnOcean Wireless Transmitter were powered from the output of the DC/DC Converter. These two boards combined provide wireless data transmission of not only on-board analog and digital sensors, but also optical sensors [33]. Tests were conducted characterizing the wireless abilities of the TEG plus checkerboard heat sink power supply. The setup is shown in Figure 2.25.

The output of the TEG plus heat sink was connected to the DC/DC Converter due to the fact that the EVA120 and STM110 required a 4V supply for operation. The EVA110 receiver board was simply powered by an external supply and serially interfaced with the computer. Software enabling communication with the receiver board was provided with the kit. The interface is shown in Figure 2.26.

The interface in Figure 2.26 not only records the data from the various sensors, but also the time between transmissions and the average time of all transmission. The rate at which the recordings occur is proportional to the power supplied to the board. Figure 2.27 shows a sweep of the input

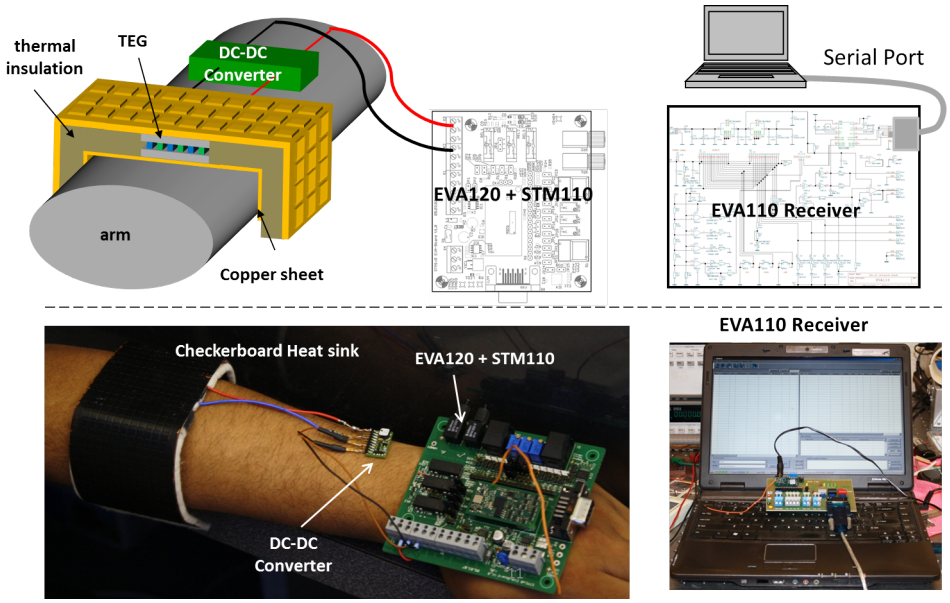


Figure 2.25: A model and image of the test setup used to characterize the wireless transmission abilities of the TEG and checkerboard heat sink source.

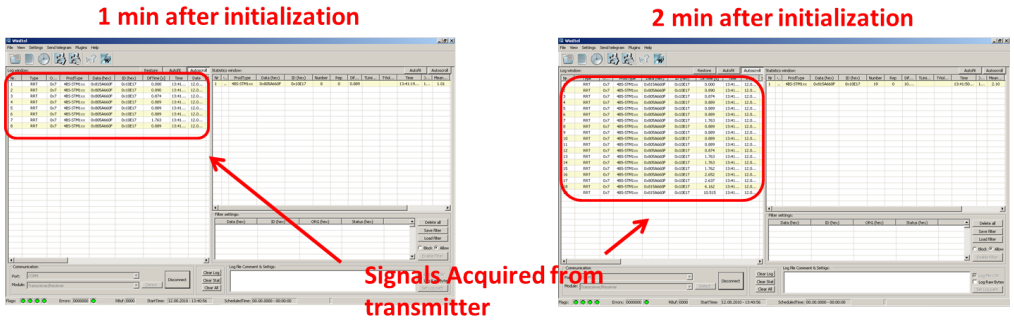


Figure 2.26: The user-interface provided with the EnOcean kit records any incoming transmissions from the EVA120+STM110 transmitter board. Screenshots of two different times after beginning communication with the board are shown.

power into the DC/DC Converter, which in turn was connected to the transmitter board. The average rate of transmission is plotted given a particular input power level.

As the power level inputted into the DC/DC Converter is increased, the mean wireless transmission time decreases until eventually reaching the maximum rate of transmission. The TEG and checkerboard heat sink yielded approximately a 7 second mean transmission time.

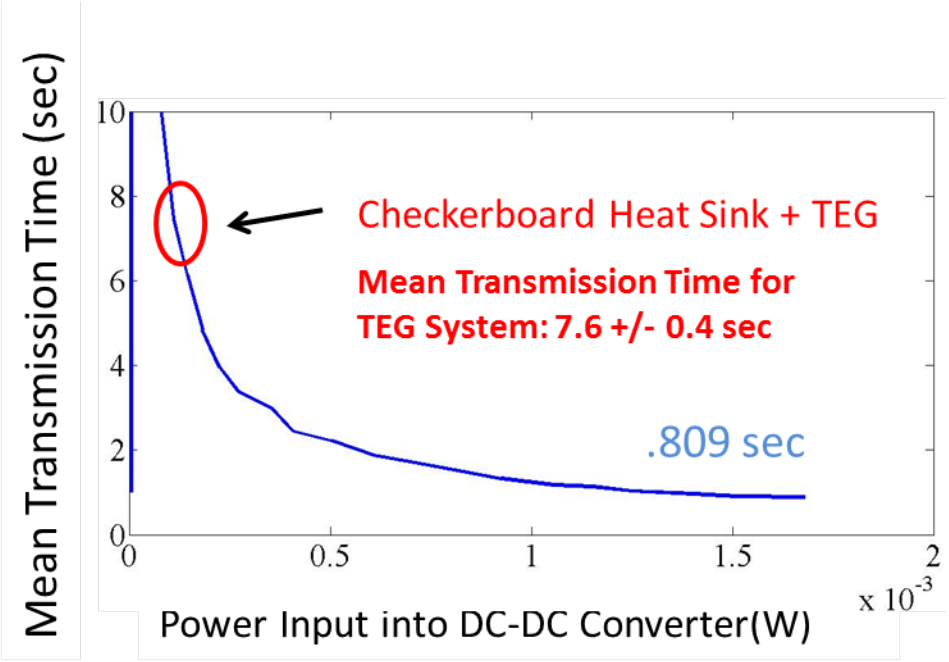


Figure 2.27: A power sweep was conducted with the appropriate mean wireless transmission time plotted for each input power level.

2.5 Conclusion

The motivation for the work done in this chapter stemmed from the lack of any reasonable body-powered, TEG-based supplies. By placing a constraint on the maximum thickness of the heat sink, the system is ensured to be low profile and comfortable. Theoretical analysis and heat sink optimization were used to create a foundation for the experimental design. The results of the experimental designs matched well with those predicted in the theoretical models. More specifically, the performance of the different variations of heat sinks (checkerboard, plain, length grooved, etc.) was proportional to the surface area in contact with the ambient environment. As a result, the checkerboard heat sink provided the best performance due to its high surface contact area. When worn around the upper forearm, the checkerboard heat sink provided approximately $290\mu W$ of power at steady state. The results of the 80-minute field test showed that the DC/DC Converter was able to steadily output 4V, even with fluctuations on the input. With this TEG and heat sink supply as well as the DC/DC Converter, different loads were tested and characterized. The first test connected a simple LED to the output and the optical properties were characterized. Next, the wireless transmitter board, as part of the EnOcean kit, was connected. Its wireless properties and functionality were characterized.

Although the performance of the wristband heat sinks was competitive with state-of-the-art heat

sinks currently in the market, issues with contact still remained. More specifically, movement of the arm yielded fluctuations in the hot side contact between the TEG and the arm. Additionally, the rigid nature of the heat sink made each wristband unique to the individual's arm. This meant that an individual with a smaller forearm will be unable to maintain a good contact with the wristband meant for someone with a bigger forearm. The next chapter aims to target these issues with the introduction of the flexible TEG.

Chapter 3

Flex TEG

3.1 Motivation

Apart from the relatively rigid nature of the designed wristband heat-sinks, one of the biggest disadvantages with such a system is the uneven temperature distribution. As illustrated in Figure 2.10, a temperature gradient forms from the cold-side copper directly above the hot source and the ends of the copper, which is approximately 14 cm away. In addition, experimentation of the designed heat-sinks revealed issues with maintaining contact between the arm and hot side of the TEG. Although the hot-side copper sheet was intermediately placed to mitigate this, contact still remained an issue. With these issues in mind, however, work began in creating an integrated TEG and heat-sink system which was more form-fitting than the original heat-sinks or any wearable TEG-based energy harvesters currently available. Apart from integrating the TEG with the heat-sink, work has been done in adding bio-sensors as well as processing circuitry onto the flex printed circuit board substrate. The design for a flex EKG processing system with on-board electrodes and circuitry will be introduced in Chapter 4.

3.2 Theoretical Analysis of the Flex TEG

3.2.1 Design and Composition

The design for the flex TEG was based on stretchable circuits research done by Professor Mary Boyce and Chris Boyce, of the Mechanical Engineering Department at MIT [46]. In the patent, they introduced patterned, flex strips which aided in remaining conformal when the board was put under mechanical stress. Figure 3.1 shows some of these patterns, which are foundational for the design of

the flex TEG. Notice that unidirectional as well as bidirectional flex strips are illustrated.

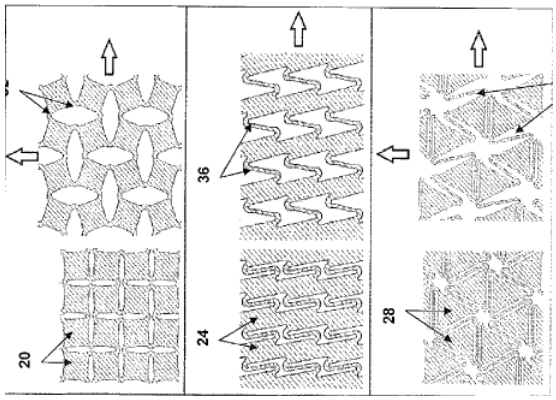


Figure 3.1: Unidirectional and bi-directional flex patters [46].

The designed flex TEG, introduced in Chapter 1, relies on 1-D stretchability, meaning that the device may expand in length only. Although 2-D was initially considered, TEG dicing limitations prevented us from moving forward.

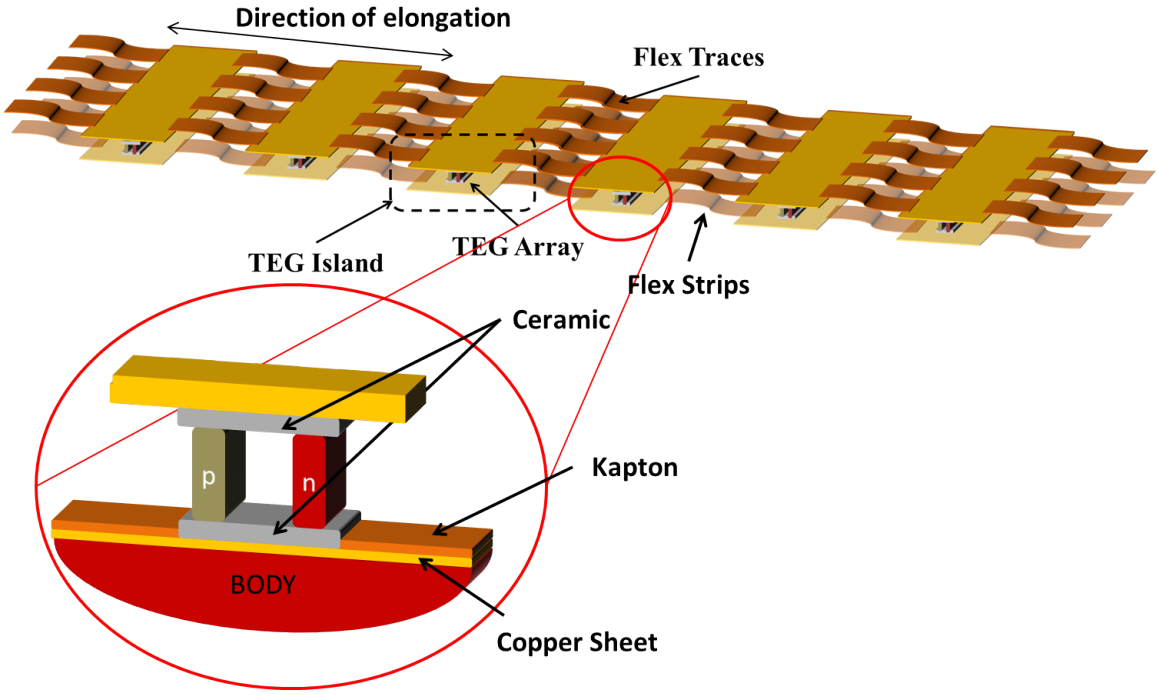


Figure 3.2: Flex TEG design.

The current design, illustrated in Figure 3.2, utilizes not only the flex strips introduced earlier, but also a 2nd layer of copper, patterned in a similar way as the flex printed circuit board (PCB). A top view of the flex PCB is illustrated in Figure 3.3. The square boundaries within each island expose the bottom layer copper. The TEG arrays are mounted on top of this exposed area.

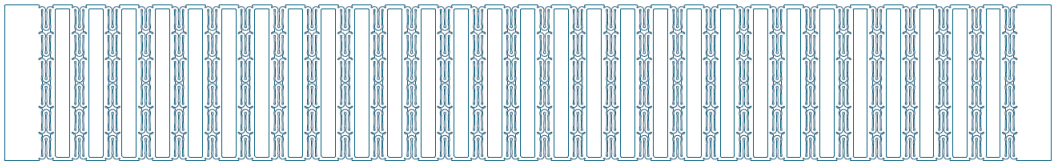


Figure 3.3: Top view of the flex kapton layer. Each island is interconnected with the flex patterns.

The PCB is composed of two layers; the first is a copper sheet layer and the second a kapton layer. The copper sheet and kapton combined have a thickness of approximately 2 mils.

Material	**Thermal Conductivity** (W/mK)
Kapton [47]	0.37
Copper	401

Table 3.1: Material properties of 1 mil copper and 1 mil kapton.

The kapton-copper material is laser-cut into the flex patterns. At particular areas on the board, the kapton is etched away in order to leave exposed copper. This is where the TEG arrays rest. On top of the kapton-copper sheet rest the electrical traces for electrically connecting adjacent TEG arrays. More details on the flex TEG fabrication will be introduced later in this chapter.

Each TEG element on an "island" (refer to Figure 3.2) is essentially a long panel of p-n thermocouples. The individual modules were cut using a dicing saw into eight strips, and each strip is contained within an island. The cold-side copper is also patterned in a similar way as the kapton-copper sheet. The TEG arrays are thermally bonded to the hot side copper sheet and cold-side copper with TIM (not shown in Figure 3.2).

Viewing the thermal conductivity properties of kapton, from Table 3.1, one may observe more than an order of magnitude difference. Translating this into a thermal resistance, assuming 1 mil thickness by 2.5 cm^2 area,

$$R_{th,copper} = \frac{\Delta x}{kA} = 0.000254\frac{K}{W} \tag{3.1}$$

$$R_{th,kapton} = 0.2745\frac{K}{W} \tag{3.2}$$

This implies that the kapton material may be assumed to be a thermally insulating material. The heat flux is then restricted to pass from the arm, through the cold-side copper sheet, and finally into the hot side ceramic of the TEG.

3.2.2 Thermal Impedance Optimization

Due to the relatively thin dimensions of the flex strips in the cold-side copper sheet and due to the difficulty of modeling, the flex strips were assumed to be absent. This is justified based on the Finite Element Analysis results in Figure 3.4, done by Dr. Katey Lo.

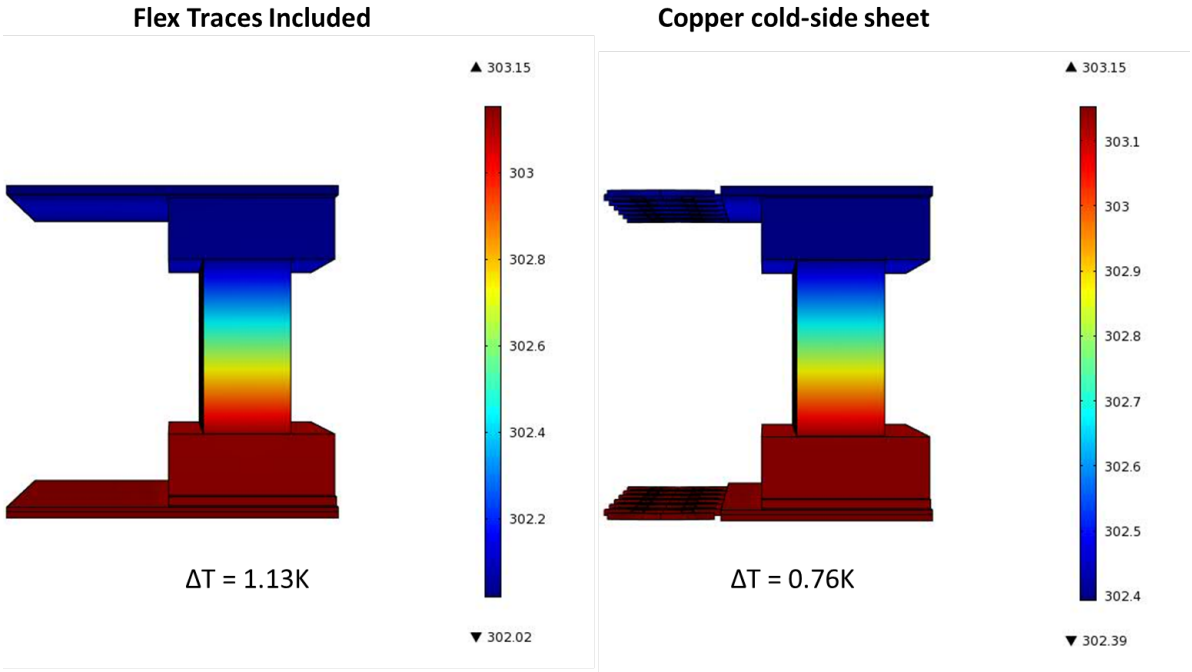


Figure 3.4: The inclusion of the flex strips yielded a lower temperature differential when compared with just replacing the strips with more copper.

Therefore, simulations proceeded with each TEG island as a standalone system, with an entire flex TEG containing roughly 25 islands.

Assuming each island contains $1/8^{th}$ of an entire TEG, from Table 2.2, it is apparent that the thermal impedance of each array is

$$R_{th,array} = 24\ \frac{K}{W} \tag{3.3}$$

Since,

$$R_{th,TEG} \approx 3\ \frac{K}{W} \tag{3.4}$$

$$R_{th,TEG} = R_{th,array\ 1} \parallel R_{th,array\ 2} \parallel ... \parallel R_{th,array\ 8} \tag{3.5}$$

Now, assuming that each copper heat-sink panel above the TEG array is approximately 4 cm x

1 cm in area, then the thermal resistance of the panel due to natural convection is

$$h = 5\frac{W}{m^2K} \tag{3.6}$$

$$R_{th,copper\ panel} = \frac{1}{hA} \tag{3.7}$$

$$= 250\frac{K}{W} \tag{3.8}$$

In order to completely match the thermal impedance of the array with that of the copper panel, one would need approximately 40 cm^2 area with the same convection coefficient. Practical limitations, discussed later in this chapter, limited the maximum area to $1/10^{th}$ that requirement.

3.2.3 Simulation Results

Finite element analysis was performed on each island. Here, as before, the hot and cold side temperatures were $33°C$ and $23°C$, respectively. The convection coefficient was again assumed to be 5 W/m^2K. Lastly, the cold and hot side copper thicknesses were 1 mil.

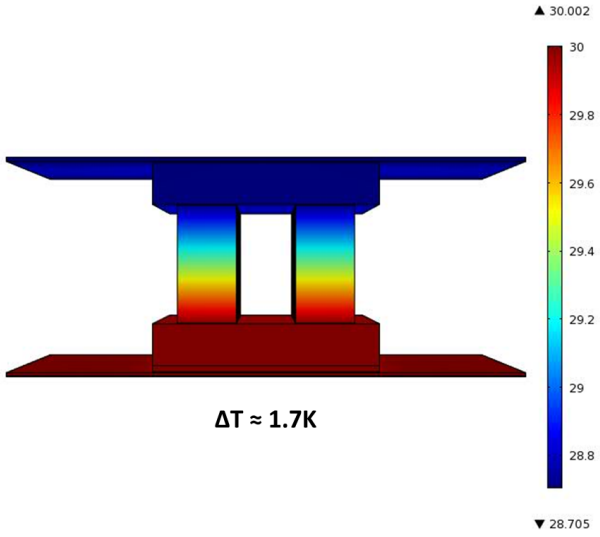


Figure 3.5: Single flex TEG island finite-analysis results.

A ΔT of $1.7°C$ was observed, yielding approximately a 0.34mV open-circuit voltage per TEG array. Assuming 35 TEG arrays per heat-sink system, this translates to about a 12 mV open-circuit voltage for the entire system. Experimental results, assuming 5 mil thickness for the cold-side copper, revealed 18mV for 24 arrays.

3.3 Fabrication and Experimental Results

The results of the simulations from the previous section as well as a preliminary analysis of the design procedure led to not only limitations but also changes in the overall flex TEG design. Further details to these mechanical and electrical limitations are noted in this section.

3.3.1 Design Procedure and Supplies

Flex PCB Design

The flex TEG requires not only the specialized flex printed circuit board (PCB) template, but also the diced TEG arrays. The design of the PCB, modeled in Figure 3.3, contains slits in each TEG island to mount the hot side of the TEG with the bottom side copper. Unfortunately, the flex circuit manufacturer, for their single layer PCB, utilize a single sheet of kapton with electrical traces on one side but are unable to cut out the slits for each island. Thus, a third party laser cutting service was necessary in order to prepare the module for TEG population. The uncut flex TEG PCB template is shown in Figure 3.6.

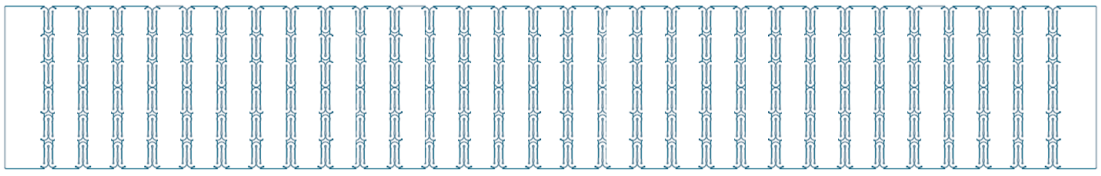


Figure 3.6: The uncut TEG required laser cutting of the slits within each TEG island as well as cuts around the electrical traces.

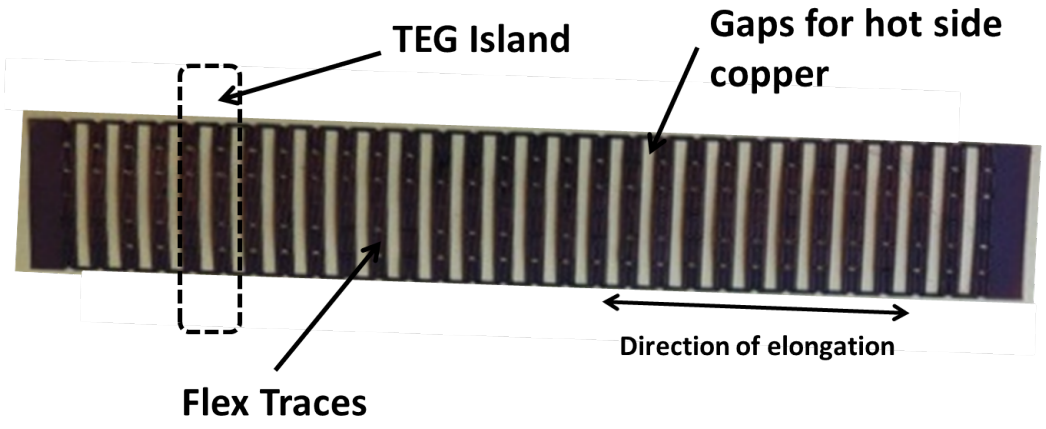


Figure 3.7: The product of the laser cut yields kapton slits on each island for the placement of the TEG arrays.

The laser cut flex TEG is illustrated in Figure 3.7. Although not clear from Figure 3.7, laser cutting around the flex traces was also necessary due to PCB manufacturing limitations. The intensity of the laser was tuned to ensure minimal burning of the kapton substrate while successfully cutting the material itself.

Hot Side Copper Strip Population

Upon cutting the flex PCB slits on each island, a thin copper sheet was appended to the bottom of the board, away from the electrical traces. This ensured adequate contact between the hot side ceramic of the TEG with the body. Figure 3.8 shows a part of the flex TEG, with the bottom layer copper added.

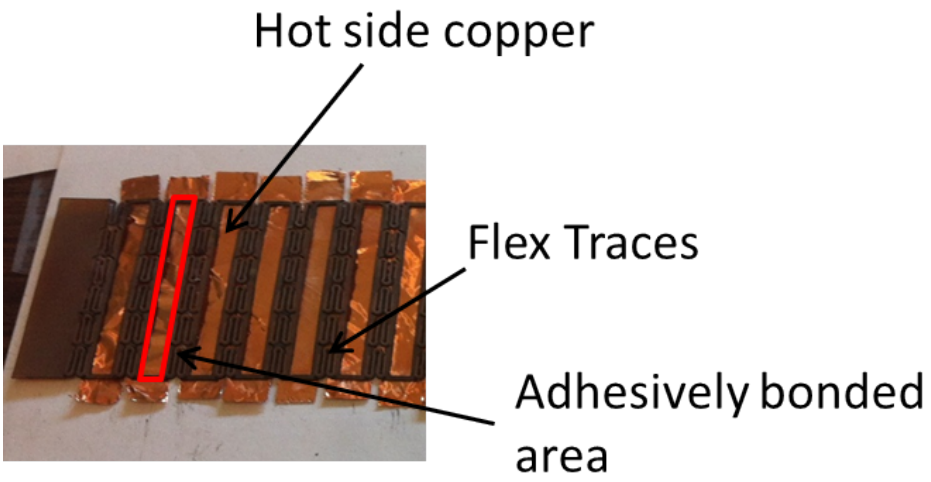


Figure 3.8: A thin copper sheet was cut into area equal to that of each individual TEG island. Adhesive was used to append the copper and the cut kapton.

Upon cutting the copper sheet into an area equal to that of the TEG island, the strips were placed beneath the flex TEG board. Each island had a separate hot side copper strip, as illustrated in Figure 3.8. Adhesive glue was applied on the four boundaries of each island. Upon doing so, the copper strip was slid underneath each area and bonded with the flex board. The result was a solid, copper platform for the TEG arrarys.

TEG Array Placement and Bonding

Figure 3.9 shows the original TEG module as well as the diced TEG arrays. The dicing was done by using a 20μm dicing saw.

The entire module was taped to a flat surface using double-stick tape. A small thread was fed

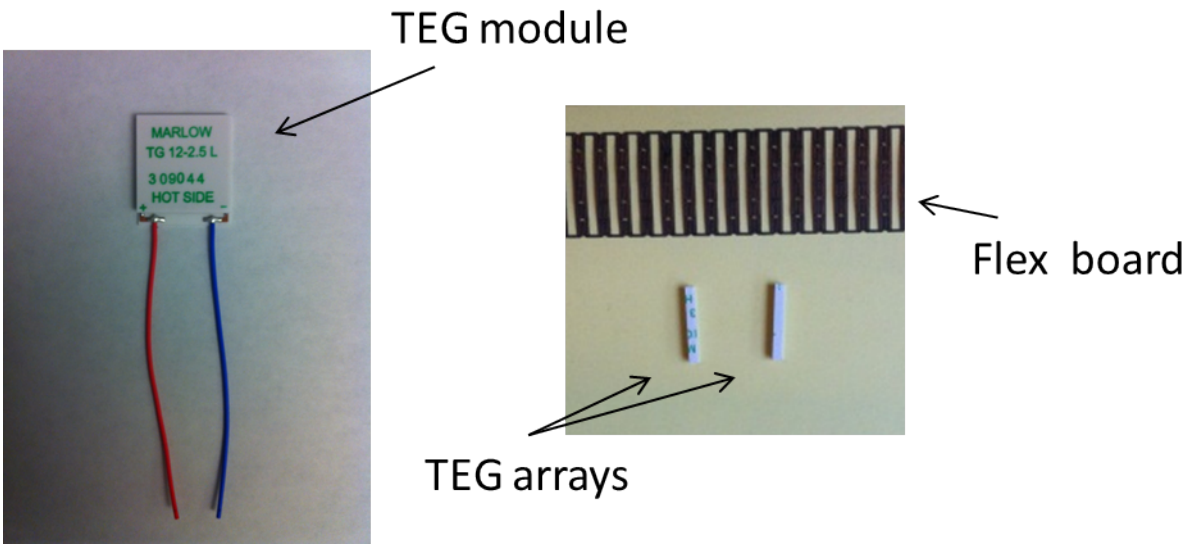


Figure 3.9: Two TEG arrays are shown after being cut with a 20μm dicing saw.

through the TEG elements, in between the two ceramic places, which aided in providing a visual guideline for the dicing saw. Due to the small dimensions, precision guidance was accomplished through a video feed from a microscope. For each module, a total of fourteen cuts were made – seven for the top ceramic plate and seven for the bottom. This yielded the necessary 8 TEG arrays.

A thermal connection between the TEG arrays and the hot side copper sheet was done with minimal thermal interface material (TIM). Additionally, an electrical connection between the leads of the TEG arrays and the board's electrical trace was made using high conductivity silver epoxy. The resulting flex TEG is shown in Figure 3.10.

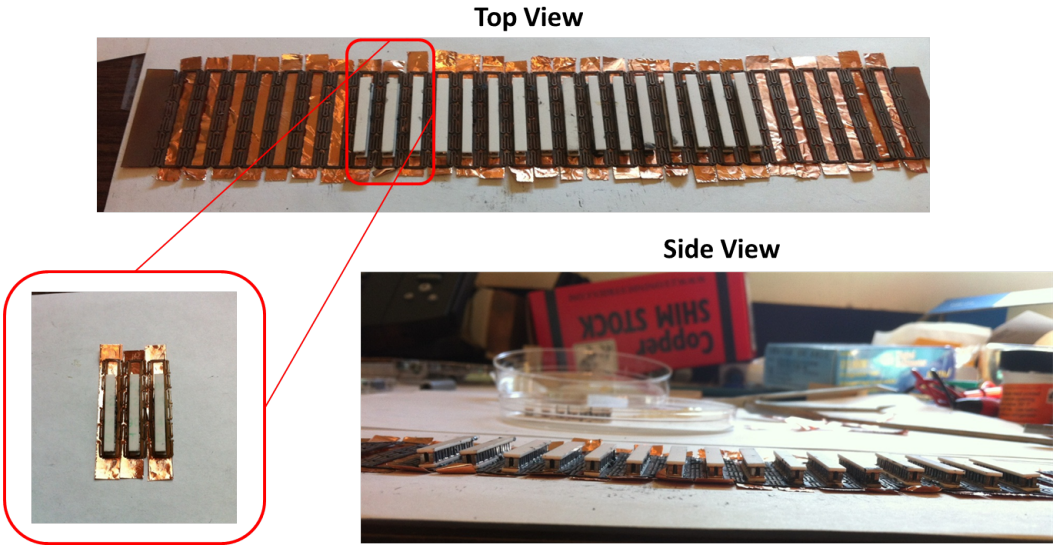


Figure 3.10: A side view and top view of the populated flex TEG is shown.

A top view and side view are shown. In Figure 3.10, two TEG modules were diced and populated, yielding a total of 16 TEG arrays. Upon thermally and electrically connecting the arrays to the board, the top, cold side, copper strips were added. Again, TIM was used to thermally connect the cold side ceramic of the TEG arrays with the cold side copper strips. The thickness of the copper was 8 mils. Figure 3.11 shows the completed flex TEG.

Figure 3.11: Upon thermally connecting the cold side copper strips with the ceramic, the flex TEG is ready for curing of the TIM (the white sticker was used to hold a thermocouple for thermal measurements).

The entire flex board, after placing the cold side copper strips, was put in an oven, set to $100°C$, in order to cure the TIM and further harden the silver epoxy. Curing took approximately 10 hours.

3.3.2 Results

Multiple tests characterizing the flex TEG were performed. The flex TEG contained the equivalent of two modules worth of arrays (or 16 arrays). First, it was placed on a hot plate and the output, open-circuit voltage as well as temperature differential was recorded as a function of time. The resulting plot is shown in Figure 3.12.

The temperature of the hot plate, initially, was approximately room temperature. Measurement began after setting the hot plate temperature to 100°C. The slow ramping up of the hot side voltage is apparent from Figure 3.12. From the data, an increase in the temperature differential across the flex TEG translates roughly to an 8.5mV increase in the open-circuit voltage. The test in Figure

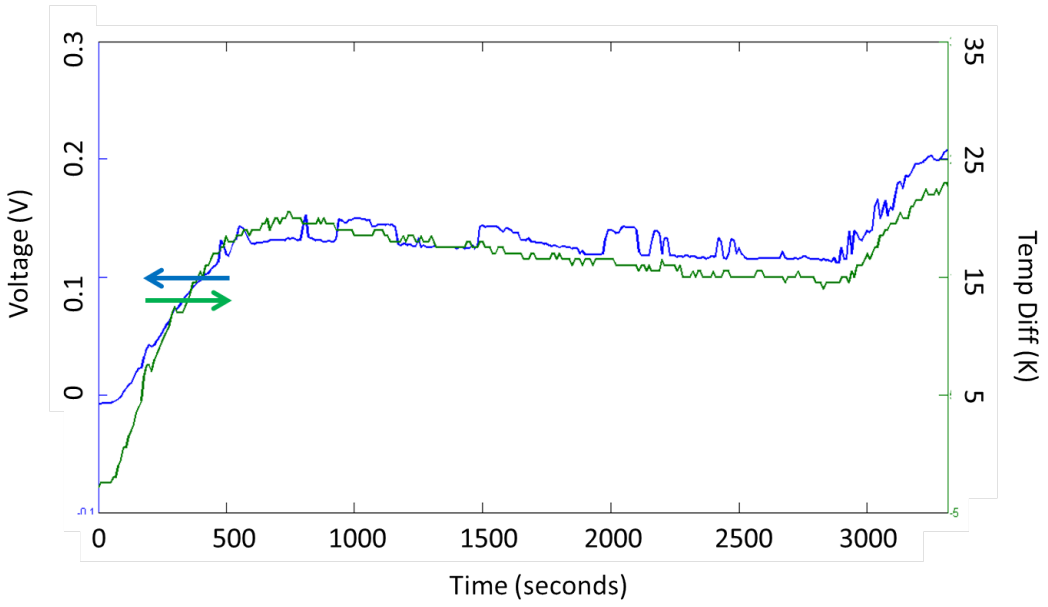


Figure 3.12: The flex TEG's open-circuit voltage and temperature difference were measured as a function of time.

3.12 was conducted for approximately 1 hour, with measurements taken every 10 seconds.

Apart from this, a second test was conducted characterizing the performance of the flex TEG when the hot side was an individual's arm. The test setup is shown in Figure 3.13.

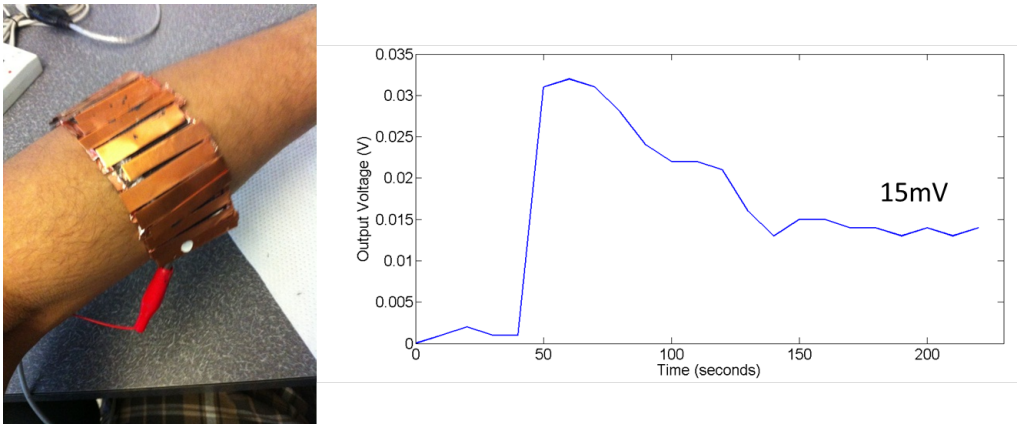


Figure 3.13: The performance of the flex TEG was recorded when worn around the upper forearm.

The flex TEG was wrapped around the upper forearm and data logger probes were used to record the output voltage from the system. At steady state, which was approximately 3.5 minutes after being worn, the system's output voltage was approximately 15mV. This indicates a 2°C temperature difference between the hot and cold sides.

Additionally, tests were conducted characterizing the optimum power and equivalent internal impedance of the flex TEG. The optimum load and power are summarized in Table 3.2.

Internal Impedance	33 Ω
Optimized Power	11 μW

Table 3.2: Internal Impedance and Power Characterization of the flex TEG.

The theoretical internal impedance is assumed to be 20Ω, due to the placement of 2 TEG modules, each with a 10Ω impedance. However, parasitics in the board itself yielded an additional 13Ω impedance. The input impedance was calculated by varying the load impedance and finding the point where the voltage across the load was half the open-circuit voltage. The optimized power at this load was calculated to be 11μW.

3.3.3 Design Limitations and Improvement

Perhaps the two greatest areas of improvement come through the varying the area of the cold-side copper heat sink strips and varying the thickness of the electrical traces in order to mitigate parasitic effects.

Cold-Side Copper Dimensions

In Section 3.2.2, we calculated the properties of the cold side copper required to optimize the output power. The result was a 40 cm^2 area. Limitations in the form of dimensions of the flex traces constrained the maximum width of the strip to approximately 1cm. Although the length may be made as long as possible, an ideal length of 40cm would be cumbersome and impractical. Thus, by increasing the length from the current 4cm to a higher value, a better performance is expected. Alternatively, by increasing the spacing between adjacent TEG islands, the constraint on the width of the system becomes more lax. However, this brings up further issues with parasitics, which will be explored next.

Trace Width and Electrical Parasitics

Multiple iterations of the flex TEG board revealed a balance in the dimension of the flex traces. Ideally, in order to minimize the electrical parasitic resistance of the board, the trace width would be made as large as possible and the trace length as small as possible. If the length of the trace is maintained constant (equivalent to fixing the distance between adjacent TEG islands), the width

would have to be increased. Currently, the trace width was approximately 5 mils or 0.13mm. By using the following expression to calculate the trace resistance,

$$R = \frac{\rho l}{A}, \tag{3.9}$$

where ρ is the trace resistivity (assumed to be $1.7 * 10^{-7}\Omega * cm$[48]), l is the length of the trace (2.5cm), and A is the cross sectional area of the trace (0.13mm x 0.13mm), we see that

$$R \approx 0.025\frac{\Omega}{trace} \tag{3.10}$$

For the entire flex TEG, which contains 17 traces, the equivalent trace resistance becomes approximately 0.5Ω.

Additional sources of electrical impedance come from the high conductivity silver epoxy used to connect the TEG arrays with the board traces. Utilizing a similar approach to that shown above, except with a volume resistivity, ρ, of 0.0174 $\Omega * cm$, a length of 0.5cm, and an area of $0.8cm^2$, then,

$$R = 0.01\frac{\Omega}{Silver\ Jumper} \tag{3.11}$$

This shows that per silver epoxy "jumper" used to connect the TEG array with the copper trace on the board, a 0.01 Ω resistance may be expected. The flex board contains a total of 32 Silver Jumpers. Thus, the total resistance contribution from the silver epoxy becomes

$$R = 0.348\Omega \tag{3.12}$$

Combined, the trace and silver epoxy resistances total to approximately 1Ω. However, 13Ω was observed during experimentation. Differences here may be attributed to improper assumptions made with the dimensions of the silver epoxy contacts.

As explored before, one possible means of reducing the parasitic resistance is to increase the width of the flex traces. However, a particular dimension of kapton is required to surround the electrical trace. More specifically, approximately 0.5mm of kapton needs to surround the electrical traces to pass the design rules set by the manufacturer. By making the electrical trace width bigger, the width of the flex traces also increases. This, in turn, makes the board more rigid, thus defeating the purpose of making it flexible. Thus, the dimension used for experimentation was the outcome of multiple design iterations yielding the correct rigidity.

3.4 Conclusion

Theoretical models as well as experimental results were introduced for the flex TEG. Thermal impedance optimization was used in order to effectively extract the maximum power from the TEG, keeping mind that this was done after maximizing the convection coefficient for the heat-sink. Due to design and practical limitations, the experimental design was constrained to dimensions differing from those theoretically calculated. Possible means of improving the performance of the flex TEG were also noted. More specifically, the electrical parasitic resistance as well as further heat sink optimization were explored.

Chapter 4

Flex EKG System

4.1 Motivation

Chapter 2 introduced the concept of 2D heat-spreading in the wristband heat sink which, in turn, aided in the effective utilization of the human body's temperature differential in comfortably generating more than 250μW of power. Chapter 3 targeted two main issues with the wristband heat sink. Namely, the rigid nature of the heat sink and the impersistent hot side contact diminished the usability of the system. In Chapter 3, the flex TEG was introduced. By utilizing a thin PCB substrate and the unique flex strip patterns, a more conformal and effective TEG and heat sink system was designed. Although the performance may be bettered through proper heat sink optimization and minimizing electrical parasitics, a basic foundation for powering applications was also created. In this chapter, the foundational template for the flex TEG will be applied in the design of a flex PCB-based EKG monitoring system. More specifically, the purpose of such a device is to reliably power and monitor a patient's EKG signal through the utilization of energy scavenging from body heat. This chapter will begin by introducing the basic design of the various sub-blocks within the system. Additionally, the reasoning behind the particular design choices will also be highlighted. Next, in Section 4.3, the board design and layout will be introduced and elaborated. The procedure for layout and population will also be detailed. The results for various tests characterizing the different aspects of the board will also be included here.

4.2 EKG System Introduction and Analysis

4.2.1 Overview

Figure 1.8, replicated in Figure 4.1 below, shows the various sub-blocks associated with the ideal body-powered EKG monitoring system.

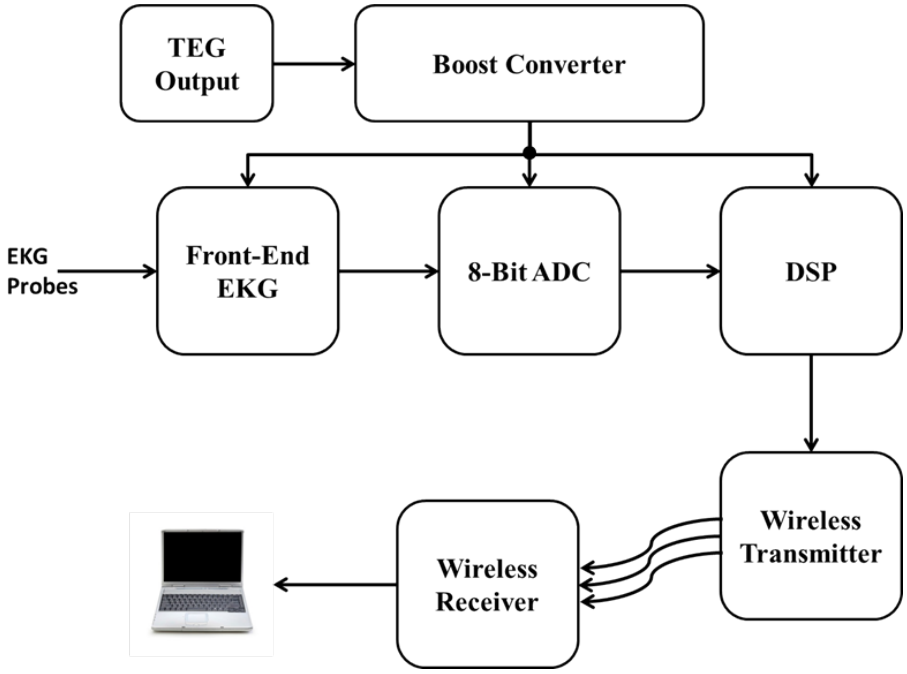


Figure 4.1: A block diagram highlighting the various sub-blocks of the EKG system is shown.

The TEG output is fed into a DC/DC Converter, which boosts the input voltage up to the necessary point required to operate the front-end analog circuitry, the analog-to-digital converter (ADC), and the digital signal processor (DSP). The data processed by the DSP would ideally be transmitted wirelessly to a receiver, which would enable further processing of the EKG data. A further introduction to the functionality of each of these sub-blocks is detailed in Chapter 1.

4.2.2 EKG Board Design and Sub-Systems

Introduction

A model of the proposed EKG monitoring is shown in Figure 4.2.

The board is composed of two main areas, the EKG Legs and the Centralized Processing Circuitry Area (CPCA). The EKG legs are composed of not only the energy harvesting flex TEG detailed in Chapter 3, but also an EKG probe. The probe itself is a copper pad placed on the bottom layer of the board in order to electrically connect with the body. The generated energy from the TEG as well

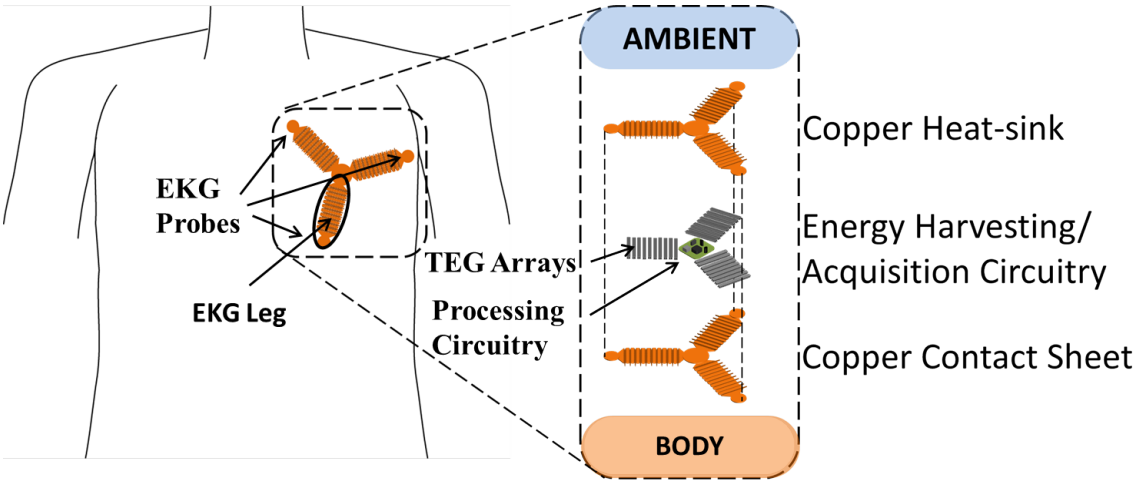


Figure 4.2: The proposed EKG system contains not only the centralized processing circuitry but also the EKG legs, which serve to acquire the EKG signal as well as generate the necessary energy from the body.

as the probe data is fed into the CPCA. Here, the analog front end and the ADC will be located. Due to design and time restrictions, an external microcontroller was used to serve as the DSP.

The EKG Legs and CPCA will be described in detail next. Additionally, the electrical as well as material interface between these areas will be discussed.

EKG Legs

As mentioned, the EKG legs are composed of the flex TEG-based energy harvester from Chapter 3 as well as an added copper pad for the appropriate EKG signal (either PLUS, MINUS, or GND for the three-probe EKG system). A top and bottom layer board layout is shown in Figure 4.3.

In Figure 4.3, notice that the flex TEG arrays, islands, and traces are essentially similar to that used in Chapter 3 for the flex TEG itself. However, the electrical trace connections were slightly modified in order to ease integration with the CPCA. Notice that the effecti1ve V_{TEG+} utilizes one of the flex traces between adjacent TEG islands in order to loop back to the left hand side of the board, towards the CPCA. The V_{TEG-} is simply extracted from the first column of traces. Lastly, the bottom side EKG pad also utilizes one flex trace from each column of traces, similar to the V_{TEG+} connection.

Centralized Processing Circuitry Area (CPCA)

The purpose of the CPCA is multi-fold. Firstly, the CPCA acquires the necessary voltages from each of the EKG legs. More specifically, the three sets of V_{TEG+} and V_{TEG-} voltages must be accumulated in order to effectively power the necessary processing circuitry. The three signals from

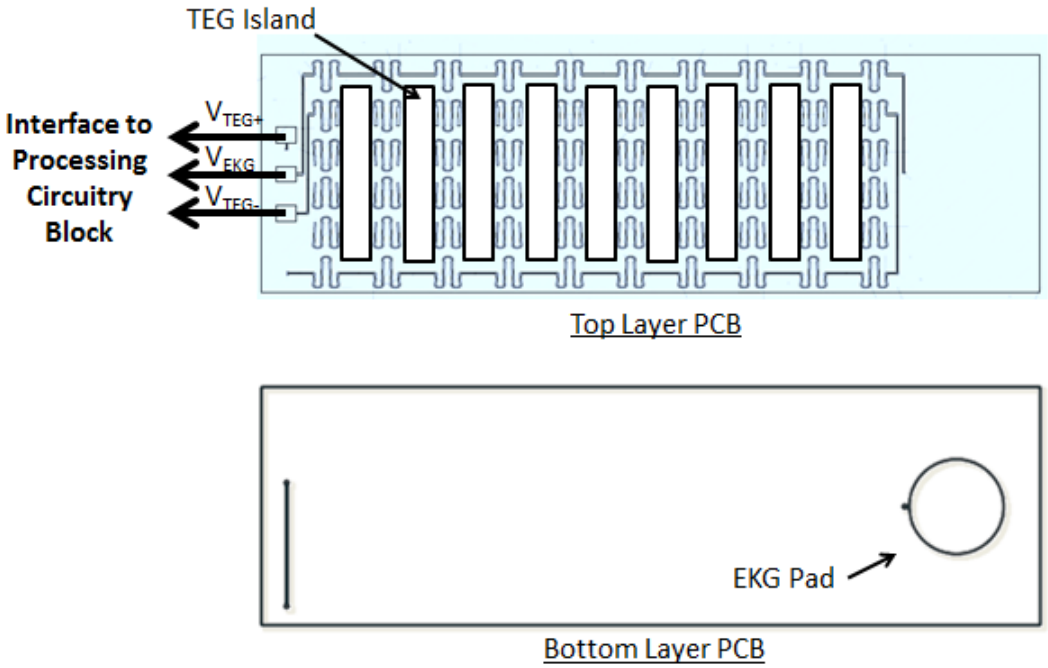


Figure 4.3: The top and bottom layers of the EKG legs are shown. The top layer consists of the TEG voltage traces (V_{TEG+} and V_{TEG-}), whereas the bottom consists of the appropriate EKG probe pad input (V_{EKG}).

the EKG probes (PLUS, MINUS, and GND) must also be carefully routed and sent to the appropriate areas of the circuitry. This will be further discussed in Section 4.3. The CPCA also contains the processing circuitry necessary to collect, amplify, digitize, and process the EKG data. For this project, the Boost Converter, Front-End EKG Analog Amplifier, and the ADC from Figure 4.1 were integrated onto the board.

Figure 4.4 shows the processing circuitry needed to boost the V_{TEG} voltage and digitize the EKG waveform. The means of collecting the V_{TEG} voltages from the three EKG legs will be detailed in the "Interface Between EKG Legs and CPCA" subsection.

In Figure 4.4, the main areas of the circuit are boxed and labeled with their appropriate functionality. Each of these areas is further studied next, beginning with the **Analog Front End Amplifier + 12-bit ADC**. Next, the **Voltage Regulation Circuitry** is studied, followed by **EKG Probe Inputs**. The **Microcontroller Interface** is also discussed, during which time an introduction to the functionality of the Chipcon CC1111 system is presented. Lastly, the **PCB Layout** will be discussed.

Analog Front End Amplifier + 12-bit ADC Marcus Yip from Professor Anantha Chandrakasan's group designed a highly programmable, ultra-low power front-end amplifier and analog-

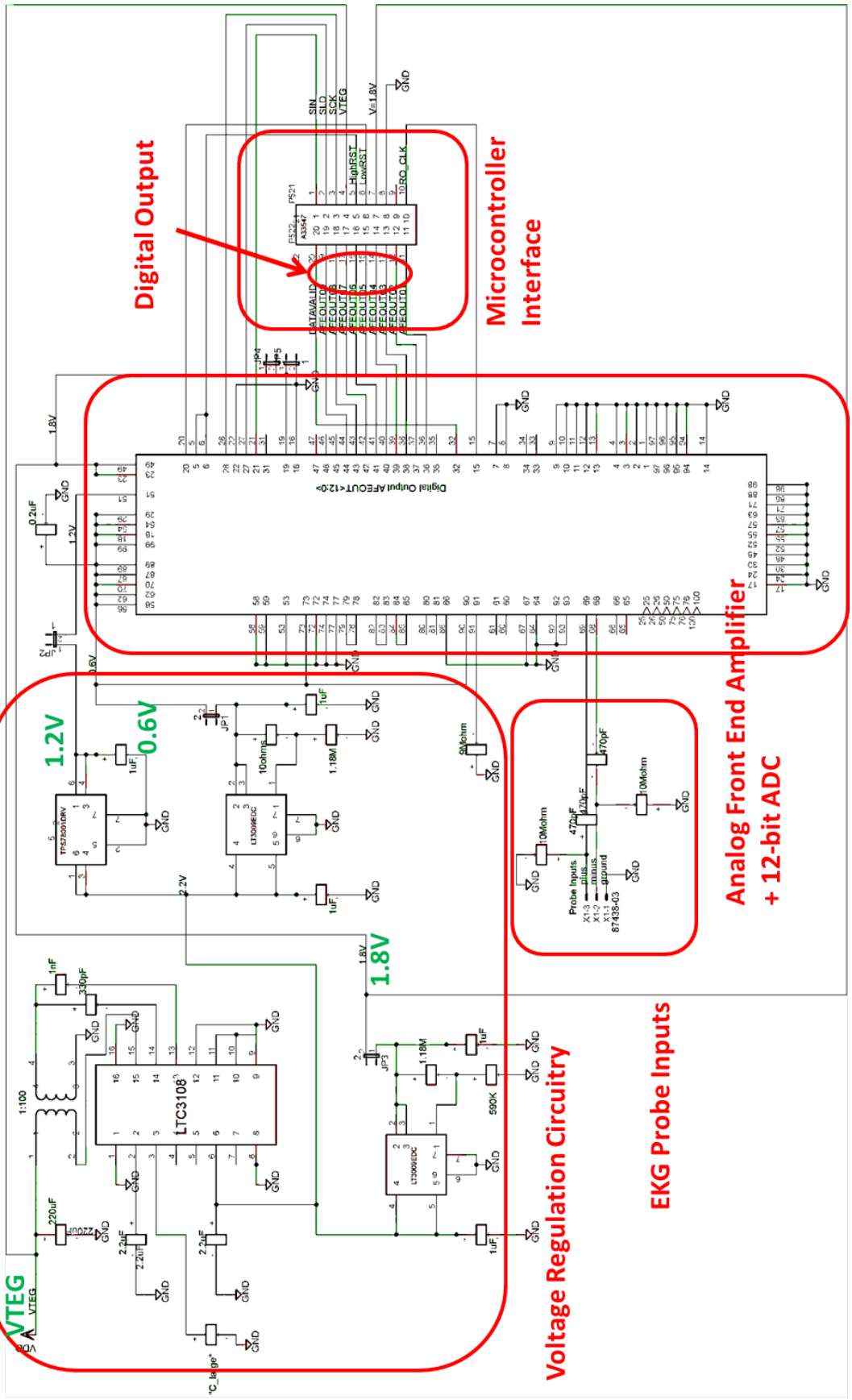


Figure 4.4: The circuit diagram for the EKG processing and voltage regulation is shown.

to-digital converter. The highly programmable nature of the chip allows the user to control most every aspect of the chip, including the sampling frequency, front-end gain, and even the output bit resolution. Table 4.1 shows some of the characteristics of the chip, including supply requirements and power consumption.

Input Supply Voltages	600mV, 1.2V, 1.8V
Typical EKG Signal Voltage Range	<8mV
End-to-End Power Consumption	2.9μW
Front-End Amplifier Gain	39dB – 70dB (programmable)

Table 4.1: Important characteristics of the front-end EKG amplifier and ADC chip are listed.

Three voltage supplies are needed to properly operate the chip, with the 1.8V powering the digital aspects of the chip. Thus, all input digital signals must maintain a 1.8V input to be labeled as a logic 'high'. The end-to-end power consumption takes into account the front-end analog circuitry as well as the ADC. The input voltage range for the EKG signals must be under approximately 8mV in order to avoid railing from the amplifier stage. The amplifier gain may be tuned based on the programming pins from 39dB to 70dB.

The functionality of the chip is controlled serially, with multiple input lines used to program the various aspects of the chip. Figure 4.5 shows the inputs and outputs of interest. Although more signals may be used to program and monitor the chip, for the purposes of this project, the following signals were adequate.

The "Probe" and "Supplies" from Figure 4.5 refer to the input voltage data from the EKG signals (PLUS, MINUS, and GND), as well as the three voltage supplies needed for the chip to function. The "Program" signals (SCK, SLD, and SIN) are used to select particular modes for the chip to operate. Figure 4.6 shows a sample timing waveform diagram for the three signals.

SCK is a 50% duty-cycled clock waveform fed into the appropriate pin of the chip. The frequency of this clock was approximately 100kHz. Upon every positive edge of SCK, the appropriate registers within the chip read the digital value on the SIN line. The chip requires 170 digital values from the SIN signal (ie 170 edges from SCK) in order to correctly program the chip. Each of these values correspond to different programmable aspects of the chip. Upon sending in 170 pulses, the SLD signal is triggered once, as shown in Figure 4.6, in order to push these values into the chip's registers,

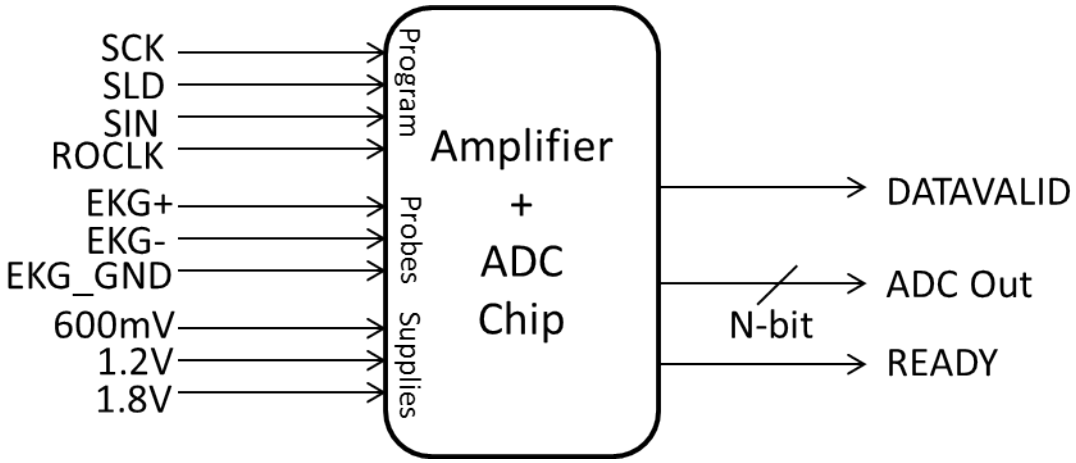


Figure 4.5: The chip requires the EKG probes, supplies, and program lines as inputs. Apart from the N-bit ADC output, the ROCLK is used to test if the chip was programmed properly.

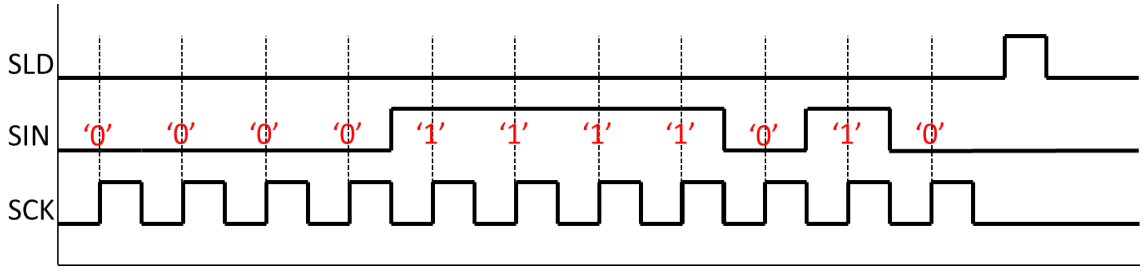


Figure 4.6: The positive edge-triggered chip reads the SIN on the appropriate edge of SCK. SLD indicates when the data is ready to be grabbed by the chip.

thereby programming it. Notice that the value on SIN changed on every negative edge of SCK, giving the signal time to stabilize to the appropriate digital value by the positive edge. The ROCLK signal input is used for testing purposes and will be described in detail later in this chapter.

The clock waveforms for SCK, SLD, and SIN were all generated on the Chipcon CC1111 system. The CC1111 is a system-on-chip (SoC) with a built-in microcontroller unit, memory, an RF Transmitter, and a USB controller. The microcontroller contains an 8051 core. All coding for the appropriate waveforms was done in assembly and compiled with a standard 8051 assembler. The coding process and results will be discussed later in this section, when detailing the **Microcontroller Interface**.

The outputs of interest from the chip is not only the digital, n-bit ADC value indicating the input analog voltage, but also a READY signal and a DATAVALID signal. The READY signals is activated upon the stabilization of the digital output of the ADC. The DATAVALID and ROCLK signals are used as initial debugging tools for testing purposes.

Voltage Regulation Circuitry In order to boost the input V_{TEG} voltage to the appropriate voltages needed by the chip, commercially available DC/DC Converters were used. Later in this chapter, possible alternatives are discussed. Due to the millivolt-scale input, boosting is necessary in order to avoid subthreshold leakage in digital circuits and inadequate linear range in analog circuits [31] within the chip.

The parts used to achieve this task were the LTC3108, TPS78001, and the LT3009. The LTC3108 is an "Ultralow Voltage Step-Up Converter and Power Manager". The chip utilizes a step-up transformer as well as a large output storage capacitor in order to efficiently boost the input voltage. The input voltage range needs a minimum of 20mV only to begin the charging process. The output from the LDO (low-dropout regulator) pin is a fixed 2.2V, with an efficiency greater than 60% for a 100mV input voltage. This 2.2V output (Pin 6 of LTC3108 from Figure 4.4) is fed into the TPS78001 and the LT3009. The TPS78001 is an ultralow power LDO and is used to buck (reduce) the input voltage from 2.2V down to 1.2V. This yields the first required chip voltage. The LT3009 is an LDO used to buck the 2.2V input down to 0.6V and 1.8V, with a maximum efficiency dictated by an output load impedance between 100Ω and 1000Ω. The resistor ratio on Pin 1 of the LT3009 dictates the output voltage from the chip. In this case, the ratios were chosen to output 0.6V and 1.8V. It is also necessary to note that although switch-mode regulators were initially considered, the requirement of a low noise output dictated the use of LDOs instead. As mentioned before, the advantage of having multiple LDO stages, where the first boosts higher than necessary to 2.2V and the second bucks down to the target output voltages, is to not only reduce the output ripple on these supplies but also to reduce the overall size of the board. The issue of output ripple will be discussed when presenting the alternative DC/DC Converter architecture. With regards to size, multiple large capacitors (in the 100μF scale) would have been required for each appropriate boosting stage. By having the first boost stage followed by the second buck stage, the number is reduced to two capacitors both on the first stage of the LTC3108.

EKG Probe Inputs The voltage data from the EKG probes came from each of the three EKG legs discussed earlier. A 470pF capacitor and 10MΩ resistor are placed on the PLUS and MINUS signals as intermediate stages before entering the chip in order to mitigate DC offsets in the signals. Due to the relative small operating voltages of these signals, equivalent-impedance wiring was necessary on the PLUS and MINUS signals. This, as well as the connectors for the probes themselves, will be discussed later in this section.

Microcontroller Interface As discussed earlier, the primary function of the microcontroller is to provide accurately timed program signals to the chip. Additionally, it may be used to process the digital output of the ADC in the chip. The Chipcon microcontroller, shown in Figure 4.7, was used to interface with the chip.

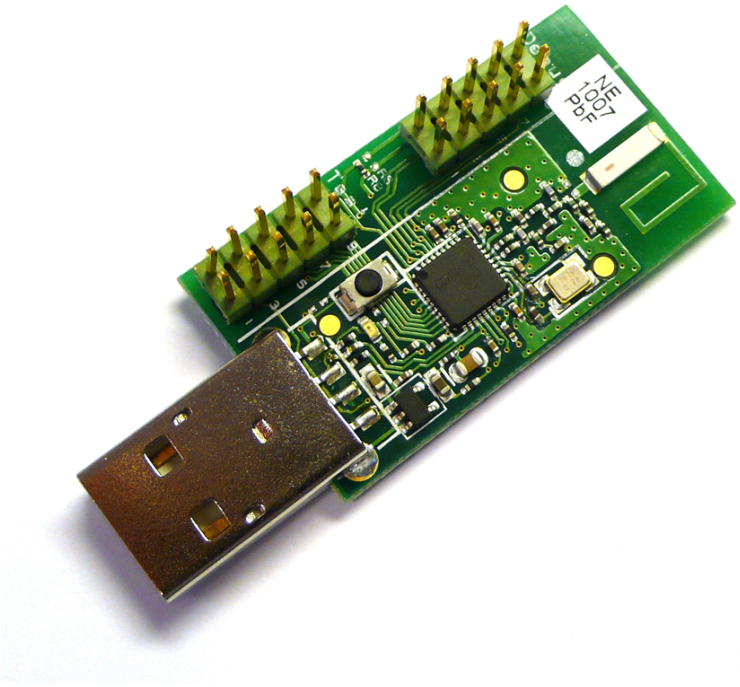


Figure 4.7: The Chipcon CC1111 board and debugger were used to program the front-end and ADC chip [49].

The CC1111 contains 12 port pins to interact with the external world. Three port pins were used for the SCK, SLD, and SIN signals into the chip. Sample code to program the chip with an arbitrary sequence of bits for SIN is shown in Appendix A. A simple lookup table was utilized in order to indicate the appropriate SIN value for the given SCK pulse. Additionally, all SIN values were changed on the negative edge of the SCK clock, thereby allowing a stable digital value to be read on the positive edge. Simple delays were implemented mainly using the `djnz` (decrement and jump if not) command. Registers were loaded with the appropriate digital delay value which controlled the duration that the microcontroller looped and waited. The delays were used to not only control the duration of the positive and negative cycles of SCK, but also the duration of the SLD signal after concluding the programming sequence.

Figure 4.8 shows the generated waveform from the microcontroller.

The three signals were outputted on the ports of the CC1111 board and a network analyzer was used to record the digital data. The sequence was repeated after each 170-pulse sequence in order

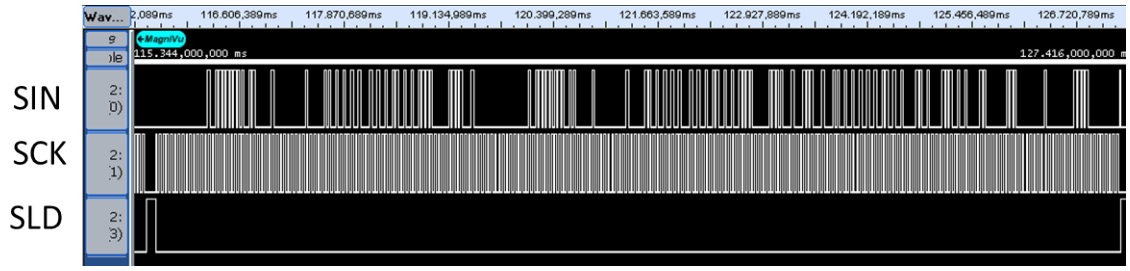


Figure 4.8: The SLD, SIN, and SCK signals generated from the microcontroller are shown. The sequence was repeated to ease capturing the waveforms on a network analyzer, thereby containing an initial SLD pulse.

to ease the recording process. Thus, an SLD signal is initially given indicating the end of the last sequence and the start of the new one. All of the digital pulses for the three signals have a logic 'high' value of 1.8V, analogous with the chip's digital values.

Printed Circuit Board Layout and Design The layout and testing of the board was done using Eagle for both the schematic and PCB designs. Both are shown in Figure 4.9, along with a labels showing the appropriate areas of the board and schematic. The board was designed on a 0.02cm kapton substrate, enabling folding and bending of the board. Details of the fabrication and population process are introduced in the next section.

The footprints for the various components were first made. The dimensions of the pins and package were available through their appropriate data sheets. The front end and ADC chip required a specialized footprint, as shown in Figure 4.10.

Test jumpers, shown in Figure 4.9 as JP1 through JP7, were placed on the voltage lines (600mV, 1.2V, and 1.8V) before entering the chip. This better enabled modular testing of the board. JP1, JP2, and JP3 were used to connect or disconnect the 600mV, 1.2V, and 1.8V lines, respectively. JP4 and JP5 were used to enable/disable the on chip notch filter. JP6 and JP7 were simple connectors used to scope particular test pins on the chip.

All of the chips were surface mount components, chosen purposefully in order to eliminate chip-to-body contact when the system is worn. Although the jumpers were through-hole, the leads may be shortened and electrical tape may be placed over the connector in order to eliminate contact issues.

The EKG probe pads line the exterior of the circular board. Three copper pads were placed for each EKG leg connection. Notice that the V_{TEG+} and V_{TEG-} from each EKG leg are connected to one another in order to create a series-voltage configuration. This interface will be further discussed in the next section.

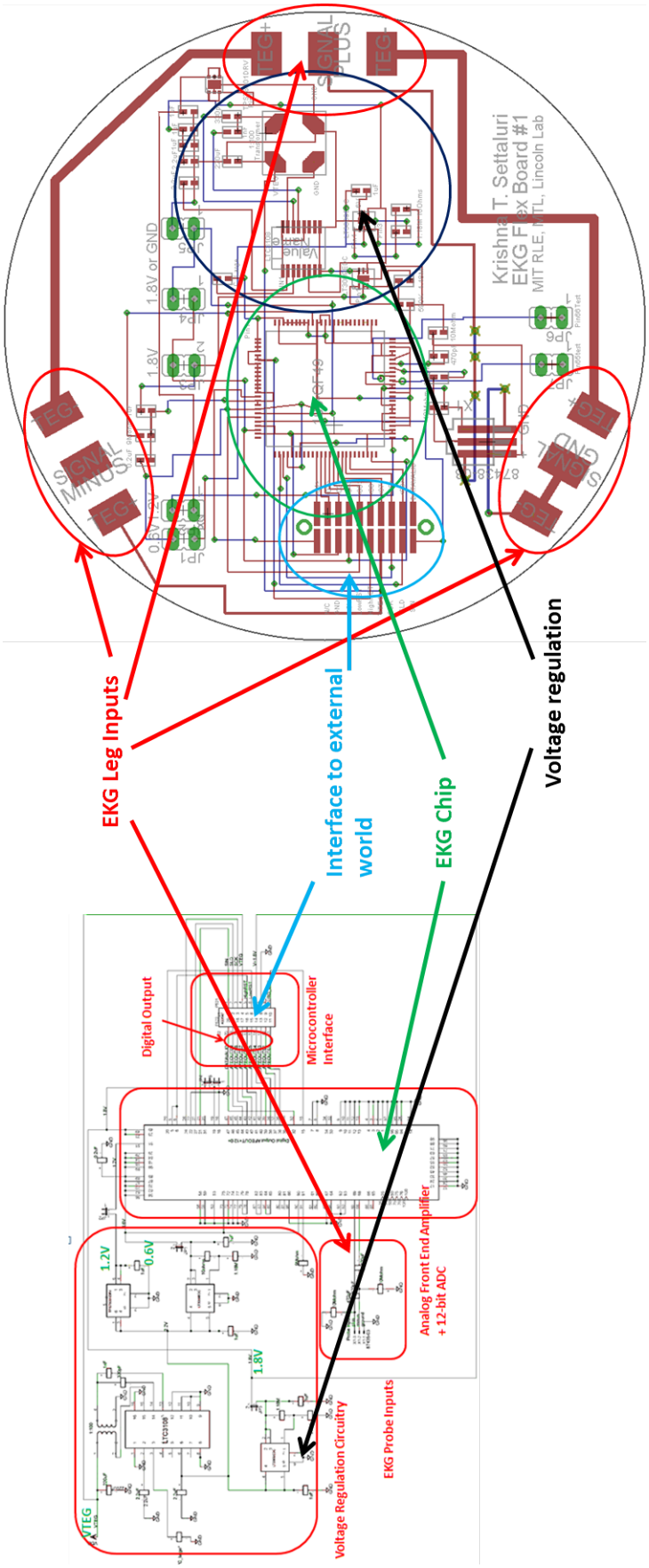
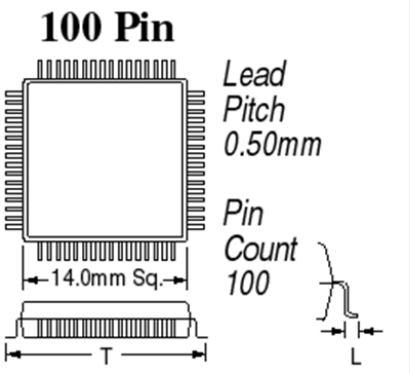


Figure 4.9: The schematic and corresponding PC Board design for the flex EKG's processing circuitry is shown.



ET Footprint Code	Footprint Type	T = Tip to Tip Dimension (mm)	L = Foot Length (mm)
100-QF49A	A	17.9	0.80
100-QF49B	B	17.2	0.80
100-QF49C	C	16.6	0.50
100-QF49	D	16.0	0.50

Figure 4.10: The footprint for the front end amplifier and ADC chip package is shown. The pin width and length were also specified.

Interface Between EKG Legs and CPCA

Large, rectangular copper pads were used to interface between the EKG legs and the CPCA. The copper pads lined the top of both the boards. Figure 4.11 shows this connection.

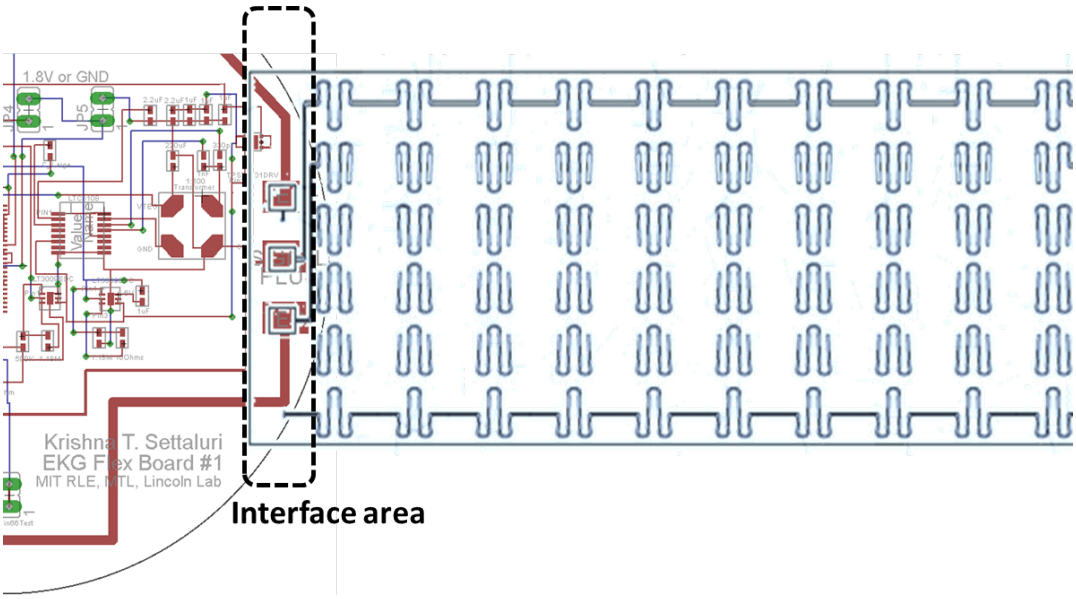


Figure 4.11: The electrical connection between the EKG legs and the CPCA is made with solder paste as well as material epoxy.

Solder paste aids in electrically connecting the EKG legs and the CPCA. Additionally, material epoxy may also be used in order to provide a stronger bond between the two boards. The bonding is similar to all three legs, as the spacing between the pads were standardized.

4.3 Fabrication and Testing of the Flex EKG board

4.3.1 Fabrication

As mentioned earlier, both the EKG legs as well as the CPCA were printed on a thin, 0.02cm kapton insulating layer. The finished board is illustrated in Figure 4.12.

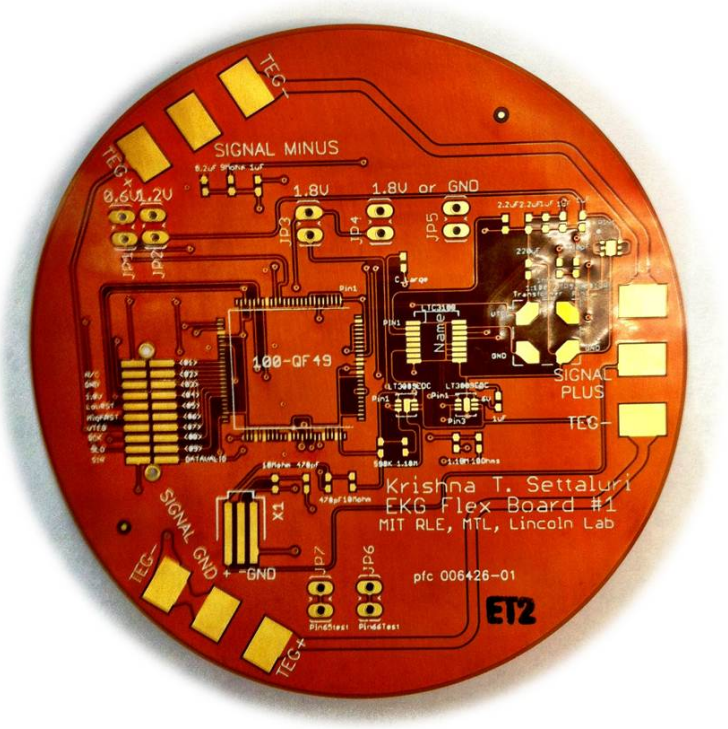


Figure 4.12: The printed CPCA, shown, has a diameter of 6.4cm.

The designed board had a diameter of 6.4cm and consisted of bottom and top trace layers with the kapton layer in between. Once the wiring was finished, a ground plane surrounding the traces was placed on the bottom layer. The top layer consisted of a 1.8V power plane. The utilization of the ground and power planes aided in further reducing the noise on the supplies [50].

Due to the thin kapton substrate, the board may be bent and folded and remain conformal. Figure 4.13 clearly shows this.

The board was populated with components using standard soldering techniques and solder paste. For the EKG chip, solder paste was evenly distributed over all of the pins after the component was in place with the footprint on the board. A soldering iron was run through each of the pins, thereby electrically connecting the pin with the pad. All pins were checked for proper contact after connecting the component. The resulting populated board is shown in Figure 4.14.

Two large capacitors, shown placed above the board in Figure 4.14, were necessary on the input

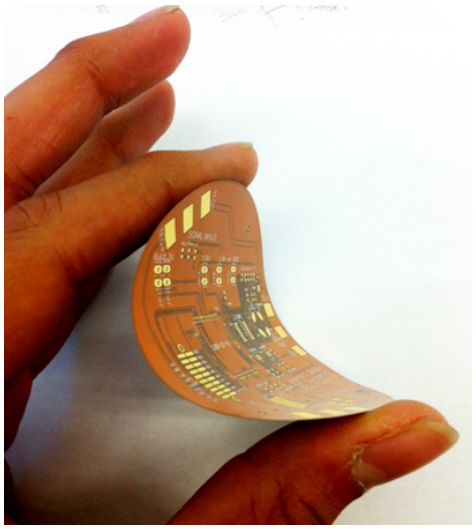


Figure 4.13: Due to the minimal thickness of the board, it may be bent and folded as shown.

of the first stage booster composed of the LTC3108 component. These capacitor were 220μF in value and aided in storing the excess charge from the TEG voltage input.

4.3.2 Testing and Results

Voltage Regulation Stage

The voltage regulation stage consisting of the LTC3108, TPS78001, and the LT3009's was first tested for proper functionality on the board. A test voltage was inputted into the V_{TEG+} probe of one of the EKG legs, with the V_{TEG-} grounded. The V_{TEG+} and V_{TEG-} on the other two legs were simply shorted for simplicity. This meant that a single voltage supply was inputted into the voltage regulation stage. The voltage connection from this stage to the EKG chip was left open. Rather, an equivalent load impedance was tied to each of the supply outputs from the regulation stage. More specifically, a 220kΩ resistor was tied to the 600mV supply, an 780kΩ on the 1.8V, and a 840kΩ on the 1.2V. These resistor values were determined based on the expected current drawn during steady-state operation from the chip. Additionally, in order to mimic the effects of the V_{TEG} source further, a current limit of 5mA was set on the input supply. This limited the maximum power that may be drawn from the supply at any time. The results of the experiment are shown in Figure 4.15.

The results show a constant DC voltage on the 1.8V, 1.2V, and 600mV lines (orange, blue, and pink in Figure 4.15, respectively). The input power was capped at approximately 60μW initially from a time of 20 seconds up to 170 seconds. At 170 seconds, the power was reduced to approximately 35μW, whereby the functionality of the boost stage failed, with a 5 second discharge time.

Figure 4.14: The populated CPCA (minus the jumpers) is shown. The two large components are 220μF capacitors for the input of the voltage regulation stage.

Front End Amplifier and ADC Chip

Preliminary tests of the EKG chip were conducted in order to test the functionality of the board and chip together. The microcontroller's port outputs were connected to the appropriate pins on the board's connector. The chip was soldered onto the board using the techniques discussed earlier. A test input sequence, SIN, was sent in order to test the chip's functionality and ability to communicate with the microcontroller. In this test, when the chip is programmed and a clocked ROCLK waveform is inputted thereafter, a duty-cycled DATAVALID output is expected. Figure 4.16 shows waveforms of the inputs to the chip in order to activate this duty-cycled output.

Notice that, in Figure 4.16, two additional sequences, besides SIN, SLD, and SCK, are needed. LowRST and HighRST are reset signals for the analog and digital parts of the chip. Upon programming, the LowRST and HighRST must be pulsed in order to reinitialize the chip completely. Notice also that a clocked ROCLK waveform is sent in upon programming. Programming completion occurs after the SLD signal is triggered once.

Figure 4.17 shows the DATAVALID signal after programming the chip and letting it run for some time.

As expected, the output DATAVALID signal is approximately a 20% duty-cycled waveform. The ROCLK waveform was maintained at approximately 420kHz for testing purposes. The peak-to-peak value of both waveforms was 1.8V, as they are both digital signals.

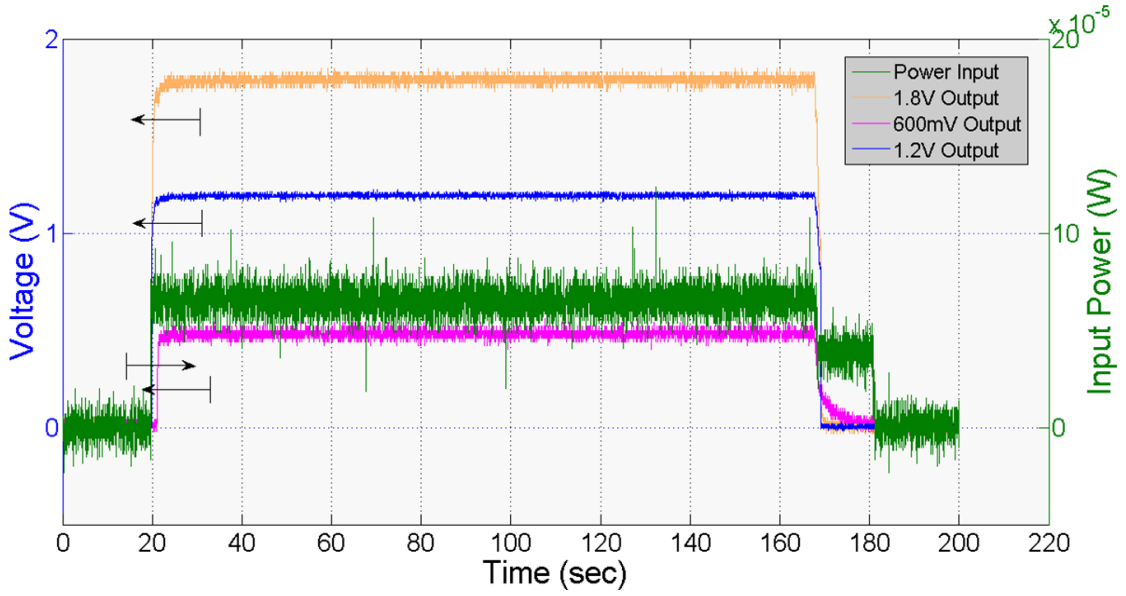


Figure 4.15: The input power and output voltage waveforms are shown for the 600mV, 1.2V, and 1.8V sources.

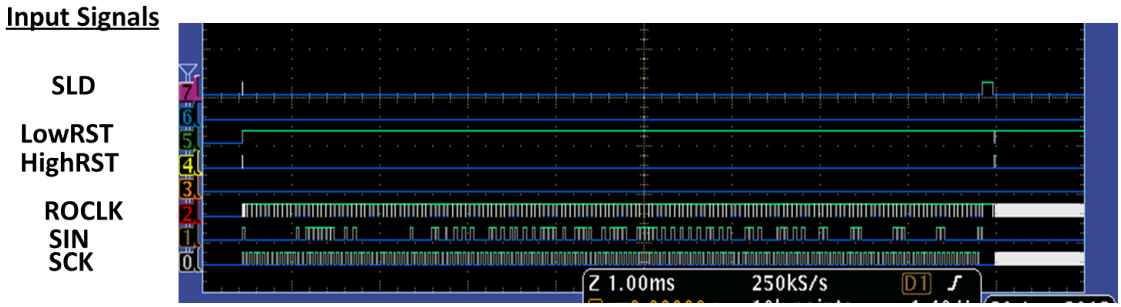


Figure 4.16: The input sequences to the various pins of the chip are shown. This mode is used to test the chip's external oscillator functionality.

Apart from this, the internal oscillator of the chip was also used to check the chip and board's functionality. Similar to the above waveform, the SCK and SLD signals were sent into the chip. However, the SIN sequence was slightly modified in order to disable the ROCLK input and activate the internal oscillator of the chip. Figure 4.18 shows the output waveform of the DATAVALID signal.

Even when the input ROCLK waveform's frequency was changed, the output remained fixed at approximately 10kHz. Additionally, when particular bits controlling the oscillator frequency in the input SIN sequence were changed, the output DATAVALID signal did indeed change.

Issues and Next Steps

Due to supply limitations and time constraints, only initial tests were performed for proof of functionality. The following details not only the biggest issues faced with the design of the flex EKG

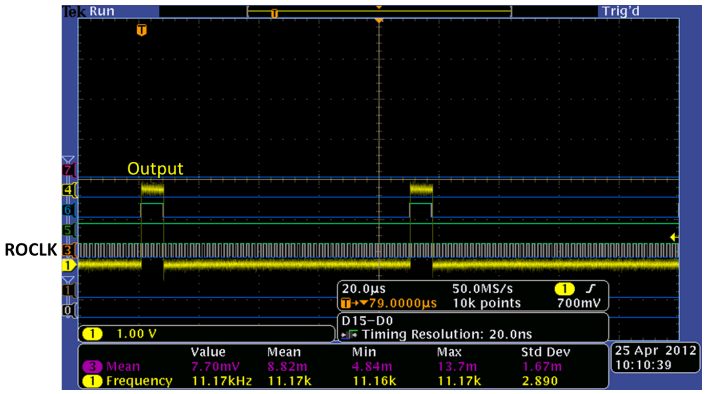


Figure 4.17: The output DATAVALID is approximately a 20% duty-cycled waveform. The ROCLK signal is also shown.

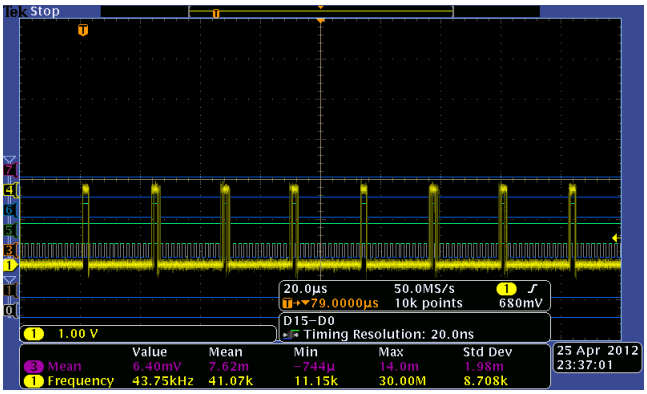


Figure 4.18: A test of the internal oscillator reveals the expected 20% duty-cycled DATAVALID signal.

board, but also provides possible avenues of future exploration within this project.

Flex Substrate and Solder Connections Due to the flexible nature of the board itself, upon soldering the component, the connection between the chip's pin and pad would frequently break as a result of slight bending in the board. Additionally, the 100-pin EKG chip contained pins with very small surface contact areas. This added to the difficulty with soldering and maintaining connection with the pad itself.

A possible solution to mitigate this issue might be to increase the length of each pad in the footprint. In doing so, more solder may be used to adhere the component with the board. This would hopefully result in a lower probability of broken connections.

ESD Protection On Chip Electrostatic Discharge (ESD) protection issues are attributed to random chip failure on the board. Three front end amplifier and ADC chips were tried in all. Although a proper protective wristband was worn following the failure of the first chip, the second

chip still managed to fail after initially working. The results for the above external and internal oscillator tests are obtained from this chip. The reason behind this is due to possible signal noise on the microcontroller when initially resetting. The failure of the third, and final, chip was due to contact degradation of a pad on the EKG chip, resulting in a missed connection. The lack of this contact pad arose during the desoldering process of the second chip from the board.

Initial Microcontroller Port Noise Upon burning the compiled 8051 code, port noise is observed on the output of the microcontroller. The microcontroller requires an initial bit sequence to be written on two of the port activation registers (`0f4h` and `0feh` from the code in Appendix A) in order to initialize the appropriate ports and set them as inputs or outputs. During this time, noise on the signal is observed on all lines, including the SIN, SCK, and SLD signals. This may have led to the failure of the second chip.

Next Steps... Due to limited supplies, additional EKG chips were not available. As a result, further testing could not proceed. The ideal first step after acquiring the chip is to ensure proper operation on the board. ESD issues should be carefully fixed. Unfortunately, no evident fix was found to mitigate the initial microcontroller noise. Because the noise was a byproduct of the assembler and burning process itself, a possible fix seems difficult. However, assuming that the microcontroller noise was not the cause of the second chip's failure, the external and internal oscillator tests may proceed as before.

Upon again successfully producing the 20% duty-cycled DATAVALID signal, the front end amplifier characterization may begin. The frequency of interest for the operation of the front end amplifier is below 10kHz. Although a network analyzer may be used to characterize the amplitude, the lower bound frequency for the device is no less than 1MHz. Thus, the magnitude plot must be made manually, by inputting a small input AC voltage into the EKG+ terminal and varying the input frequency.

The conclusion of the amplifier characterization ensures proper operation of the front end. By design, the digital output from the ADC in the chip should work by this point. The jumpers connecting the voltage regulation circuitry and the chip may now be activated. A power limited supply may be inputted to the V_{TEG} of one of the legs, as done before. Operation of the chip should still be maintained as a result.

The final step is to integrate the EKG legs with the CPCA and, again, ensure proper operation after the system becomes body-powered.

4.4 Conclusion

The foundations for a self-sufficient flex EKG monitoring system was introduced in this chapter. The utilization of the flex TEG patters introduced in Chapter 3 as well as an added processing platform (CPCA) aided in achieving this task. Various tests were performed in order to characterize the performance of the sub-blocks. Notably, the voltage regulation circuitry, which generated appropriate voltages from a small V_{TEG} voltage, was tested. Additionally, functionality of the chip was also tested. Unfortunately, due to limited time and supplies, combining the EKG legs and the CPCA was not possible. Further analysis of three of the sub-blocks within the EKG monitoring system is detailed in Appendix B. More specifically, the DC/DC Converter, front end amplifier, and an 8-bit ADC are modeled, studied, and tested.

Chapter 5

Conclusion

The utilization of the human body for energy harvesting opens new avenues of research for the design of optimized, low power applications in both the defense as well as medical fields. This report introduced not only a new technique for scavenging energy through body heat, but also applied the concept in designing a completely self-sustaining EKG monitoring system. In total, the implementation of a body-powered EKG monitoring system depends equally on the ability to scavenge energy through body heat as well as the design of ultra low power processing technology. Further iterations of the flex TEG is required in order to better the output performance. More specifically, improvements in heat sink impedance matching and reduction in electric parasitic resistance are needed. With regards to the processing electronics, optimized coupling amongst sub-blocks greatly aids in efficiency and processing ability.

Chapter 1 provided a foundation and research platform for the various fields of focus addressed in this thesis. A thorough analysis of current wearable, TEG-based applications may also be found here. Chapter 1 began with an overview of the physics of a thermoelectric generator and the concept of heat sink optimization, both of which were applied extensively in the design of the wearable wristband system as well as the flex TEG. Additionally, the concept and motivation behind the design of the monitoring system was also introduced. More specifically, a thorough review to current research in the various sub-blocks of the EKG monitoring system may also be found here.

Chapter 2 introduced the wristband heat sink system. With the objective being to remain low profile and comfortable, the wearable heat sink was designed with constraints on the maximum thickness of the system. Heat sink optimization and thermal impedance matching were utilized in order to maximize the output power from the thermoelectric generator plus heat sink system. The results showed a competitive output power when the electrical load was matched accordingly.

Additionally, an 80-minute field test was conducted, where the output of the wristband heat sink was connected to a low power DC/DC converter. Not only did the output of the DC/DC Converter remain at the desired value, but the entire system was comfortable and low profile. Lastly, in Chapter 2, test loads were placed on the output of the DC/DC Converter. More specifically, a wireless transmitter system was connected in order to show a proof-of-concept design of wireless transmission of data through a body-powered supply.

With the conclusion of a thorough analysis of the wristband heat sink system in Chapter 2, issues and possible improvements for the system were targeted in Chapter 3. More specifically, the rigidity of the wristband as well as the contact between the body and TEG were the main focus. With that in mind, the design of the flexible TEG was introduced. This system utilized unique flex traces connected between small TEG arrays in order to increase the system's overall length by up to 30%. Theoretical analysis of the designed system showed the importance of the traces as well as heat sink specifications in order to optimize the output power. Experimental tests were performed in order to further characterize the device. Lastly, possible means of improving the system were studied.

The design of the flex TEG from Chapter 3 was applied in order to create the basis for a completely self-sustained EKG monitoring system in Chapter 4. The chapter began with an analysis of the various components required within the system, ranging from the front end amplifier to the analog-to-digital converter. A proposed flex board design for the system was also introduced. The board consisted of the central processing circuitry area and the EKG legs. The legs were responsible for not only the energy harvesting but also the EKG signal acquisition. The central processing circuitry area was responsible for the energy management as well as amplification and digitization of the input EKG signal. Tests were run on various blocks of the system. However, due to supply and time limitations, not all desired tests were performed. Apart from the introduction of this flex board, schematic-level analysis was done for three of the main blocks within the EKG processing system is also detailed in Appendix B – the front end EKG amplifier, the DC/DC Converter, and the ADC. Extensive simulations were run on each of these blocks ensuring proper operation.

5.1 Future Research Path

Moving forward, extensive research may still be done in different avenues of this project. Firstly, the concept for the flex TEG may be applied to not only wearable and independent boards but may be integrated with clothing in order to provide a more comfortable means of wearing the device. Although integration of the TEGs in clothing has been researched to some extent, room

for optimization still remains [54]. Additionally, fabric-based systems may also contain external processing circuitry such as the studied EKG monitoring system besides the energy harvesting area. Varying materials with better thermal conductivities may also be researched. More specifically, the utilization of graphene as possible heat sink material poses advantages due to the high thermal conductivity nature of the material.

Apart from these, another interesting research avenue exists at the notion of systems-level design centered around supply constraints rather than sub-block optimization. More specifically, designing external monitoring circuitry, such as the EKG system, say, should depend fully on the characteristics of the input supply, rather than rely on individual sub-block optimization. Due to the varying nature of the TEG-based supply used in this work, it may be found that state-of-the-art front end amplifiers or ADCs or boost converters were not necessary, or even advised, when trying to optimize the performance of the system. Further research is needed in order to confirm this hypothesis.

Appendix A

8051 Sample Code for Chip Programmability

```
;P1.1 - Data
;P1.7 - Ready signal
;P1.0 - Clk
;P1.5 - HighRst
;P1.6 - LowRst
org 00h
ljmp start
org 100h
start:
        mov 0f4h, #00h
        mov 0feh, #0ffh
        mov P1, #00h
        clr P1.0
        clr P1.1
        clr P1.7
        clr P1.4
        clr P1.5
        setb P1.6
        mov R3, #00h
```

```
mov dptr, #getvalue2
mov R4, #00h
mov R5, #00h
lcall hugedelay
lcall hugedelay
lcall hugedelay
lcall hugedelay
lcall hugedelay
mov R7, #00h

loop:
        cpl P1.0
        cpl P1.4
         lcall bigdelay
         minval:
         jnb P1.0, plusval
                 ; P1.0 = 0
                 lcall minbigdelay
                 ;clr P1.1
                 ljmp loop
         plusval:
         jb P1.0, minval
                 cjne R4, #0ffh, keepgoing:
                         mov R4, #00h
                         mov dptr, #getvalue2
                 keepgoing:
                 clr a
                 movc a, @a+dptr
                 inc dptr
                 inc R4
                 jb acc.0, is_plus
                         clr P1.1
                         ljmp is_min
```

```
                is_plus:
                        setb P1.1
                is_min:
                lcall bigdelay
        inc r5
        cjne r5, #170d, midstring
                clr P1.1
                clr P1.0
                mov dptr, #getvalue2
                lcall hugedelay
                lcall hugedelay
                sjmp programdone
        midstring:
        sjmp loop
programdone:
        testclk:
        mov r5, #00h
        mov r1, #00h
        lcall readydelay
        clr P1.7
        loopnest:
                cpl P1.4
                inc r5
                nop
                cjne r5, #0ffh, loopnest
                inc r1
                mov r5, #00h
                cjne r1, #10h, loopnest
        lcall customdelay1
        lcall customdelay2
        setb P1.6
        lcall customdelay1
        lcall customdelay
```

```
                clr P1.5
                testclk1:
                        cpl P1.4
                        nop
                sjmp testclk1
        sjmp loop


smalldelay:
        mov R1, #10h
        delay: djnz R1, delay
ret
bigdelay:
        mov R1, #20h
        delay2: djnz R1, delay2
ret
minbigdelay:
        mov R1, #20h
        delay4: djnz R1, delay4
ret
hugedelay:
        mov R1, #0ffh
        delay3: djnz R1, delay3
ret
readydelay:
        mov R1, #00h
        setb P1.7
        ;clr P1.6
        loopcustomready:
                cpl P1.4
                inc R1
                cjne R1, #0ffh, loopcustomready
        ret
customdelay:
```

```
        mov R1, #00h
        setb P1.5
        ;clr P1.6
        loopcustom:
                cpl P1.4
                inc R1
                cjne R1, #0ffh, loopcustom
        ret
customdelay1:
        mov R1, #00h
        looproclk:
                cpl P1.4
                inc R1
                cjne R1, #0ffh, looproclk
ret
customdelay2:
        mov R1, #00h
        ;setb P1.5
        clr P1.6
        loopcustom2:
                cpl P1.4
                inc R1
                cjne R1, #0ffh, loopcustom2
ret
getvalue2:
db '0'
db '0'
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Appendix B

EKG Chip Sub-Systems Analysis

B.1 EKG Chip Sub-Systems

In an effort to make the EKG system full custom, the DC/DC Converter stage as well as the front end amplifier and an 8-bit ADC have been designed. The following discussion will begin by introducing the schematic and layout for an ultra-low power front end EKG amplifier, based on work by Professor Rahul Sarpeshkar and with grateful assistance from Allen Yin [9]. Next, a DC/DC Converter was designed in 90nm processing along with an 8-bit SAR ADC, done with guidance and assistance from Dr. Duke Xanthopoulos, Kevin Zheng, and Kat Kononov. The performance and characteristics for these two stages will be analyzed. Finally, the DC/DC Converter and SAR ADC will be combined in order to further characterize the system.

B.1.1 Front End EKG Amplifier

As stated, the front end EKG amplifier was designed based on work done by Professor Rahul Sarpeshkar. 600nm processing was utilized to layout the amplifier along with its respectful pad ring.

Schematic Design

The architecture for the amplifier follows the simple two-stage amplifier design, with common mode rejection occuring in the first stage and a simple gain stage proceeding it. The basic schematic design, done in Cadence, is shown in Figure B.1.

A rigorous analysis of the design is presented in [9]. The first stage contained two identical ordinary transconductance amplifiers (OTAs). The second stage contained a differently sized OTA

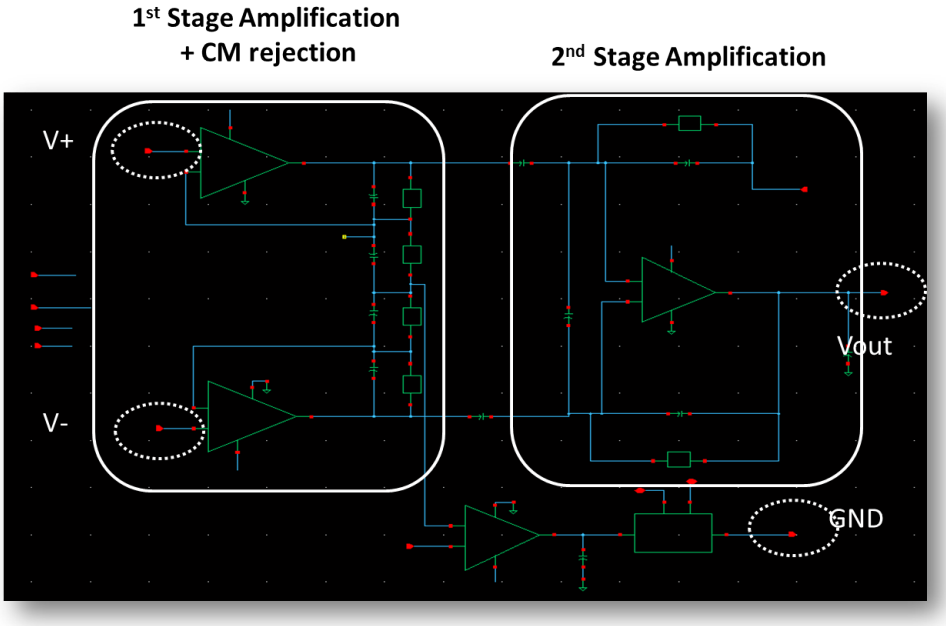

Figure B.1: The two stage topology was used in designing the EKG amplifier.

matching that of the fourth feedback OTA, connected to a buffer which in turn connected to the GND probe. The theoretical gain of the two stages was targeted to be approximately 100. However, due to imperfections during layout, the gain specification was changed to target approximately 800.

Layout

The layout of the front end EKG amplifier, done in 600nm processing, contained not only the four OTAs for the input and output stages, but also various feedback and gain stage capacitors as well as a 1mm x 1mm pad ring surrounding the circuit. The layout is shown in Figure B.2.

The OTAs as well as the capacitors took up the largest areas, with both laid out using the common-centroid technique in order to reduce the effects of silicon doping gradients on the wafer.

Results

Multiple tests characterizing the various aspects of the amplifier were performed for differing non-idealities. Firstly, capacitor mismatch was taken into account. Here, the capacitor values were offset by up to 10% to emulate the effects of actual layout. Additionally, after layout, the design was extracted back and the specs were again tested. The results for the ideal case, the mismatched capacitor case, and the extracted layout case are shown in Figure B.3.

The results show a worst-case power consumption of under 5μW with the differential gain re-

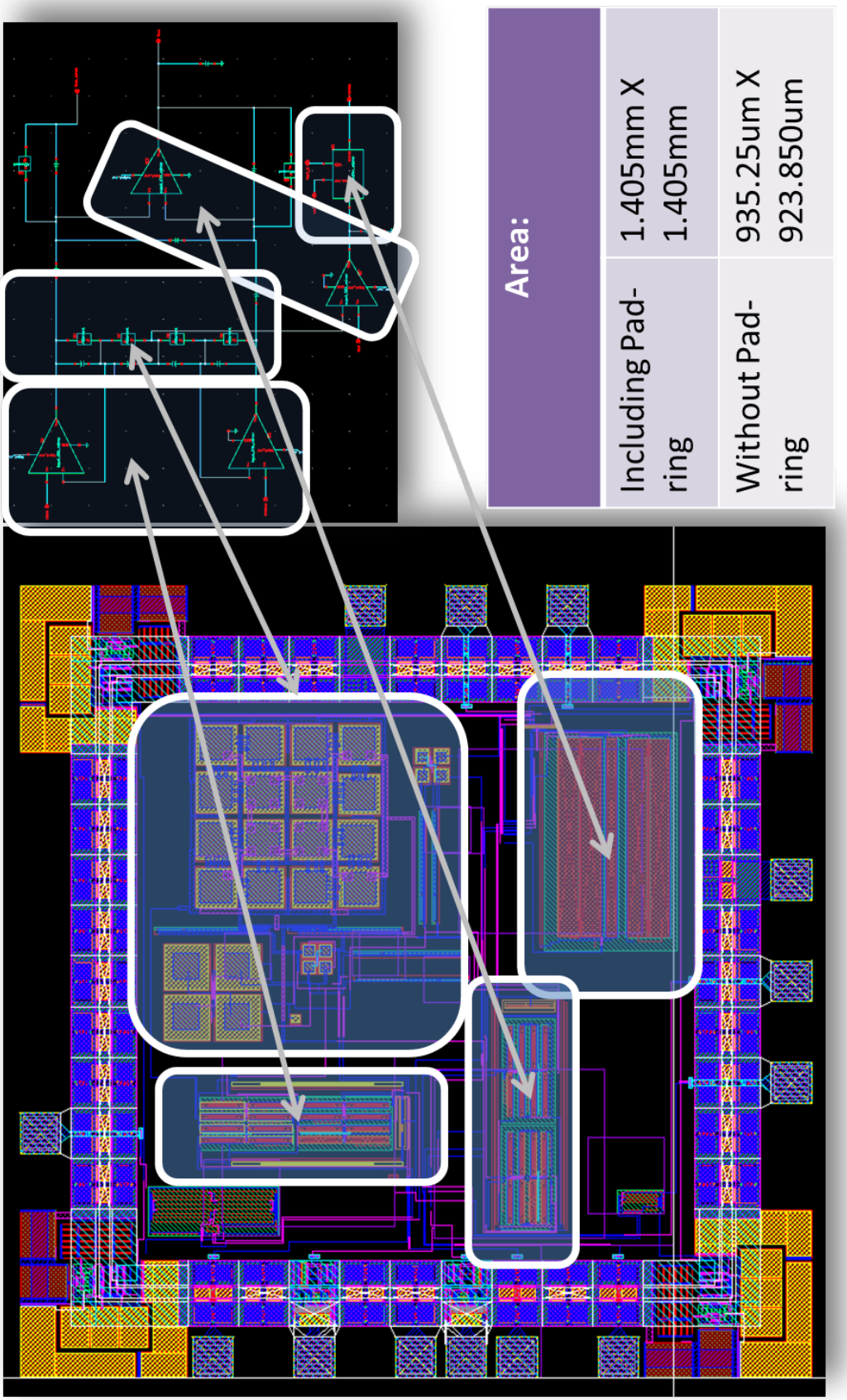

Figure B.2: The layout for the amplifier as well as the corresponding schematic and dimensions are shown.

	Ideal		Mismatched Capacitances	
Schematic	Common mode rejection	--128 dB	Common mode rejection	-60.86 dB
	Differential Gain	41.34 dB	Differential Gain	42.96dB
	CMRR	169.34 dB	CMRR	103.825dB
	Noise	8.036µV	Noise	9.976µV
	Bandwidth	2.829kHz	Bandwidth	2.2kHz
	Power	4.597µW	Power	4.597µW

Extracted		
	Common mode rejection	-60.86 dB
	Differential Gain	42.96dB
	CMRR	103.825dB
	Noise	8.133µV
	Bandwidth	2.2kHz
	Power	4.597µW

Figure B.3: The specs for three different cases are shown.

maining above 40dB. The noise, common mode rejection, and bandwidth are also listed.

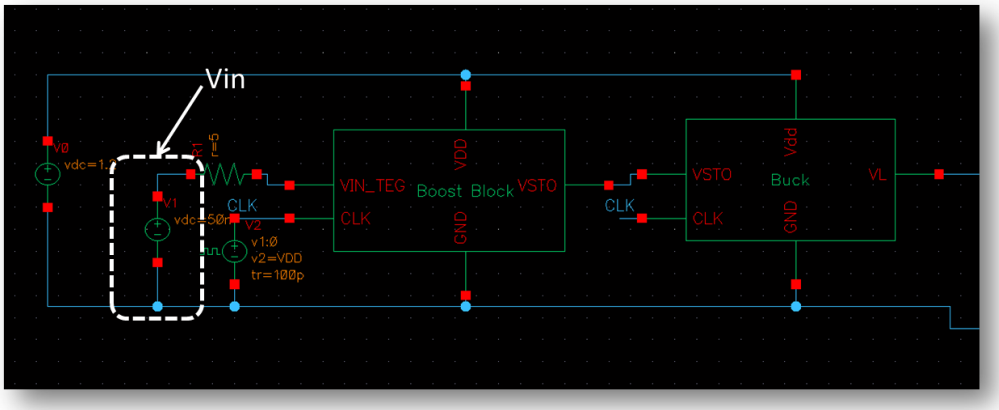

Figure B.4: The block diagram-level design of the DC/DC Converter is shown.

B.1.2 DC/DC Converter

Schematic and Design

The DC/DC Converter was designed in 90nm General Process Design Kit (gpdk090) and is based on work done by Yogesh Ramadass and Professor Anantha Chandrakasan [32]. The design consists of a boost converter followed by a buck converter. The first stage boost converter boosts the input voltage up to approximately 2.2V. The second buck stage reduces the voltage down to 1.2V. The reason for this initial boost followed by a reduction rather than boosting to the final voltage value is due to output ripple. By having this second stage, the output ripple is reduced drastically.

The basic block diagram-level design is shown in Figure B.4.

The Boost Block takes as input not only the VIN_{TEG} (which is loaded with a 10Ω resistance to simulate experimental characteristics) but also a CLK signal for the switching. The Buck Block, similarly, takes a CLK input as well as the output from the Boost Block stage. The internals of the Boost Block and the Buck Block are shown in Figure B.5.

The Boost Block contains a simple, comparator-based feedback loop dictating the ON/OFF state of the switch based on the value of the output, VSTO. More specifically, the logic simply states that if VSTO passes a particular threshold, keep the switch on and continue increasing the current through the input inductor. However, if the output drops below this threshold, turn off the switch and dump the current onto the output capacitor.

Similarly, the Buck Block contains feedback loops in order to stabilize the final value, V_L, at 1.2V, or turn off the Buck stage altogether if the output from the Boost Block, VSTO, drops below another set threshold. These feedback loops become apparent when looking at the output waveform.

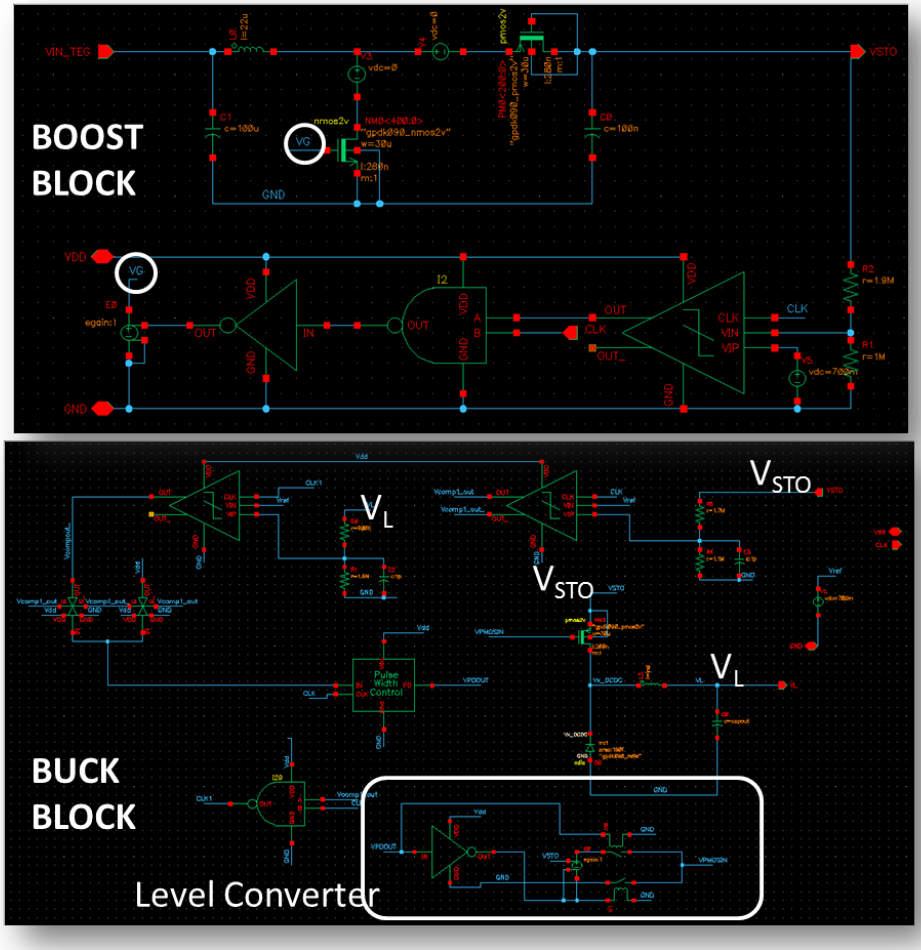

Figure B.5: The internals of the Boost and Buck Blocks are shown.

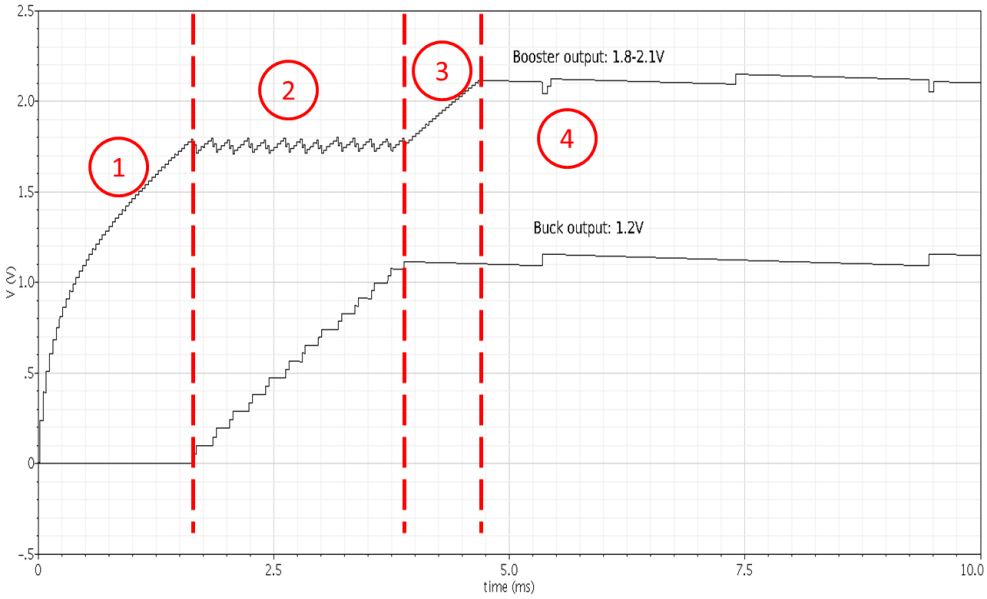

Figure B.6: The output waveforms, divided into four phases, of the Boost Block and the Buck Block after a 50mV input was applied.

Results

Figure B.6 shows the output waveform generated when a 50mV input voltage was applied to the system.

The output waveform is divided into four phases, with each phase being activated through a different feedback loops. Initially in phase 1, the Buck Block is completely inactive in order to facilitate the speedy of the output of the Boost Converter. Upon passing a particular threshold, the output of the Boost Block (VSTO) activates the first feedback loop within the Buck Block, thereby entering phase 2. Here, the Buck is continuously switching between the ON/OFF states in order to maintain the output of the Boost Block. Simultaneously, the output of the Buck Block (V_L) is picking up in order to meet the 1.2V mark. At this point, phase 3 is entered and the third feedback loop, in the Buck Block, activates and tries to maintain the V_L at 1.2V. During this time, any excess charge is stored on the output capacitor of the Boost Block, resulting in a quick increase in VSTO. Finally, in phase 4, the Boost Block feedback activates in order to maintain the voltage at 1.8V.

B.1.3 8-bit SAR ADC

Design

Block Diagram The Successive Approximation Register (SAR) ADC requires not only a comparator and charge-scaling DAC, but also a SAR block in order to alter the DAC output. Figure B.7 shows the block-level designed, 8-bit ADC.

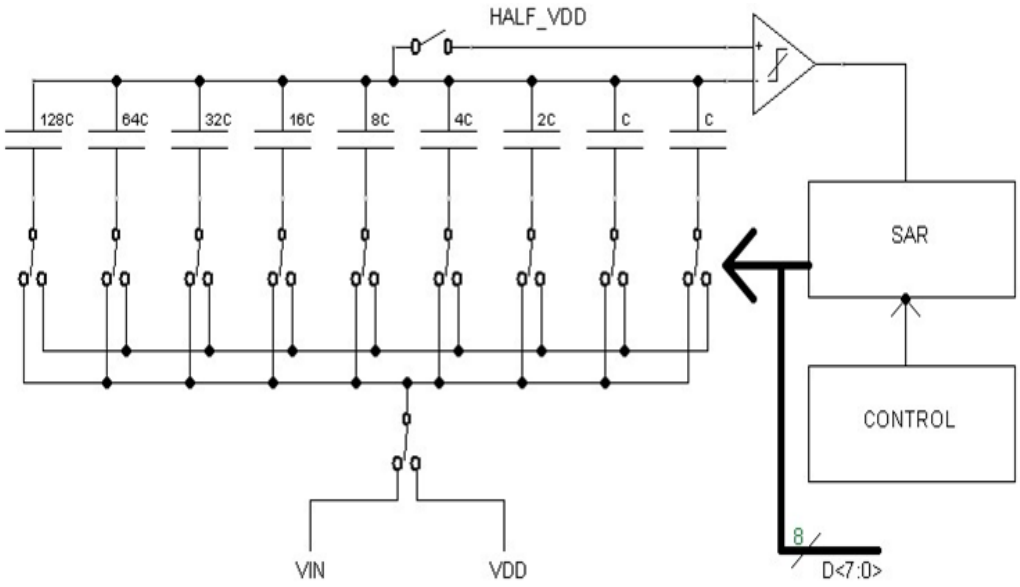

Figure B.7: A block diagram-level SAR ADC is shown.

The comparator's output dictates the necessary change in the digital output of the SAR block. Once the last bit of the digital output settles, the Control Block sends a ready signal indicating the conclusion of conversion. The following discussion details the comparator and SAR block architectures.

Comparator Architecture The designed comparator contains three stages, as illustrated in Figure B.8.

Due to the presence of an inherent offset in the 2nd stage latch, the Pre-Amplifier is placed beforehand in order to reduce this offset [51]. The Cross Inverter Latch works by having only two states on its outputs through positive feedback, either a '01' pair or a '10' pair on the OUT and OUT_ (logically negated). The choice of which state the latch enters is determined by the rate of discharge of the output load capacitors of the Cross Inverter Latch stage [52]. The final, third stage SR latch is placed to hold the state of the variables. The advantage of such a comparator architecture is to not only have a higher resolution as a result of the reduced effects of the offset, but also have no static power dissipation due to the utilization of dynamic circuit techniques.

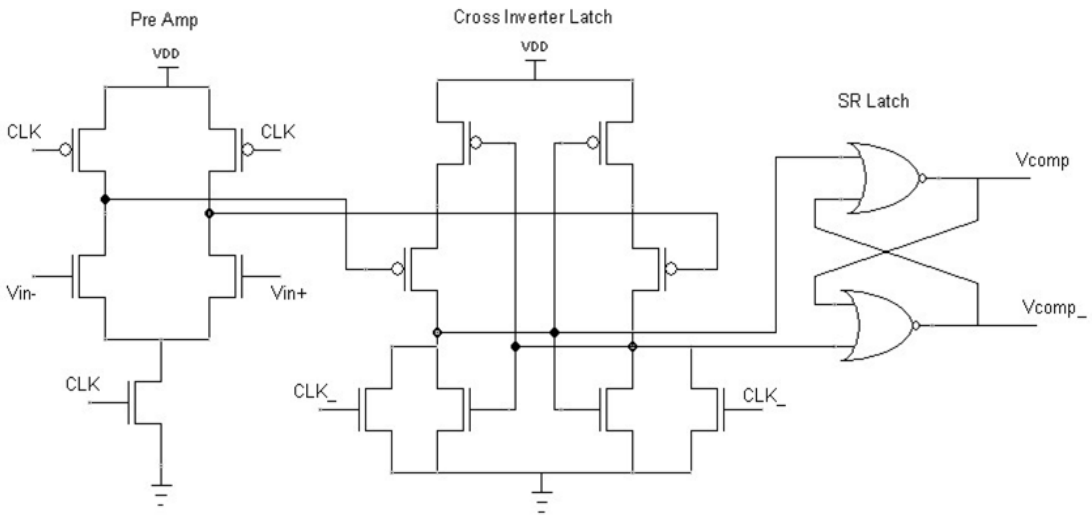

Figure B.8: The comparator contains a pre-amplifier stage followed by a cross inverter latch, and a final SR Latch in order to effectively store its state.

SAR Logic The logic dictating the state of the switches in the DAC is within the SAR block. The SAR block architecture is based on work done by T.O. Anderson and is illustrated in Figure B.9 [53].

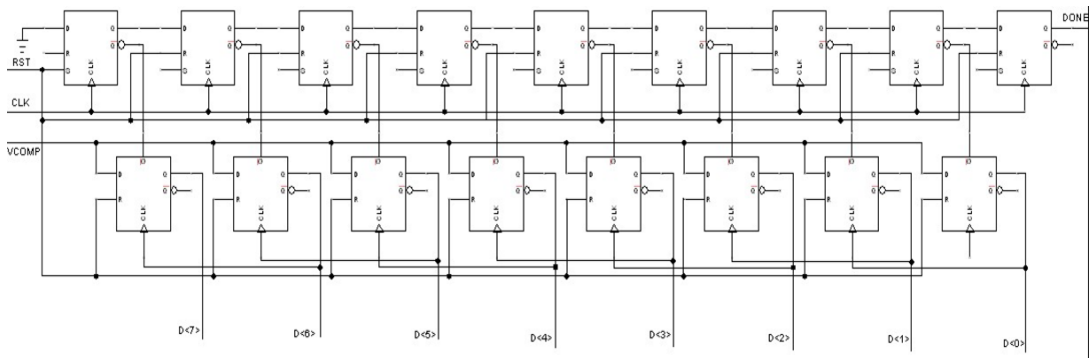

Figure B.9: The logic for the SAR block contains the sequencer and the code register.

The basic architecture of the SAR block contains the sequencer and the code register. A final DONE signal along with the digital bits is outputted upon concluding the value of the LSB. A thorough analysis of the workings of the design is presented in [53].

Results

Capacitor Array Voltage into Comparator In order to test the functionality of the SAR block, the voltage at the output of the capacitor array (or the negative input of the comparator), is plotted as a function of time in Figure B.10.

The three phases of the waveform are labeled, beginning with the input voltage reading, followed

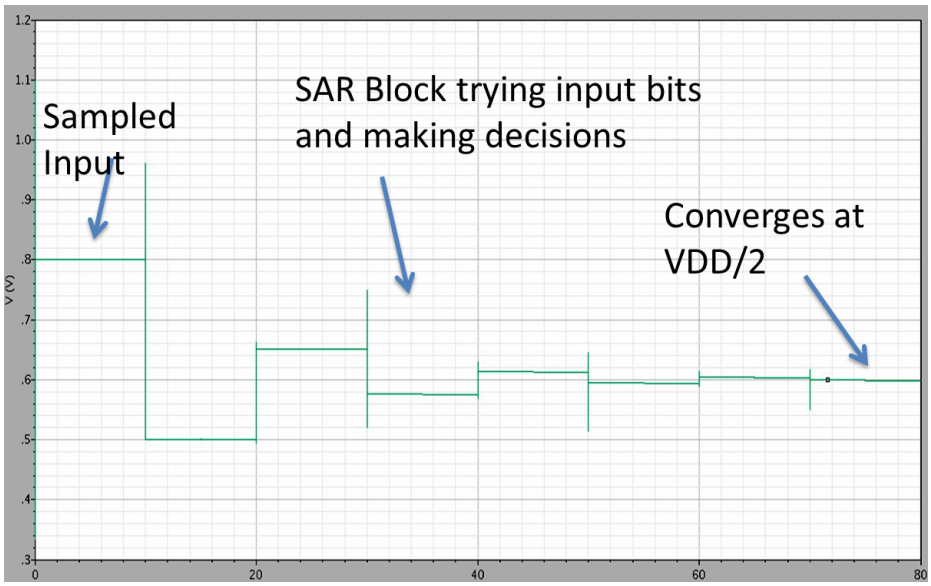

Figure B.10: The negative input of the capacitor converges correctly to the positive input of the comparator at VDD/2.

by the switching of SAR block, and finally the convergence at the correct output.

ADC Input-Output Characteristics Additionally, an input ramp was applied to the ADC in order to test the appropriate digital output. An ideal DAC was used on the ADC output in order to convert the value back into the analog domain. The results are shown in Figure B.11.

Slight offset as well as full scale errors are observed on the transfer function in Figure B.11.

B.1.4 DC/DC Converter + 8-bit ADC Test Results

Lastly, the DC/DC Converter and the 8-bit ADC were coupled together and an input, simulated EKG waveform was applied. The resulting output is shown in Figure B.12.

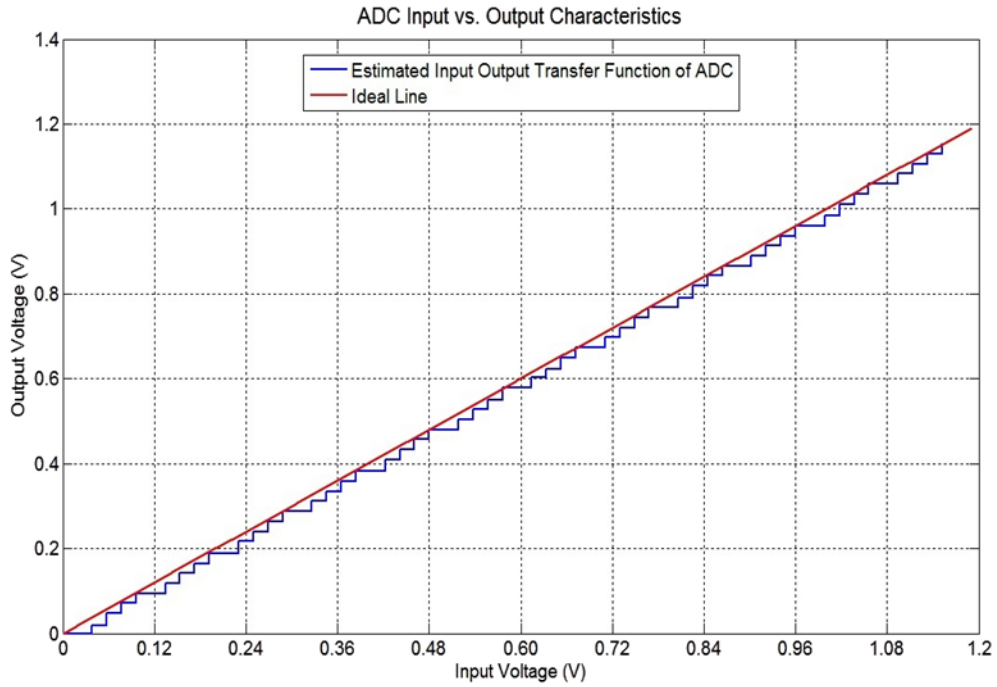

Figure B.11: An input ramp, when applied to the ADC, yielded the following output waveform.

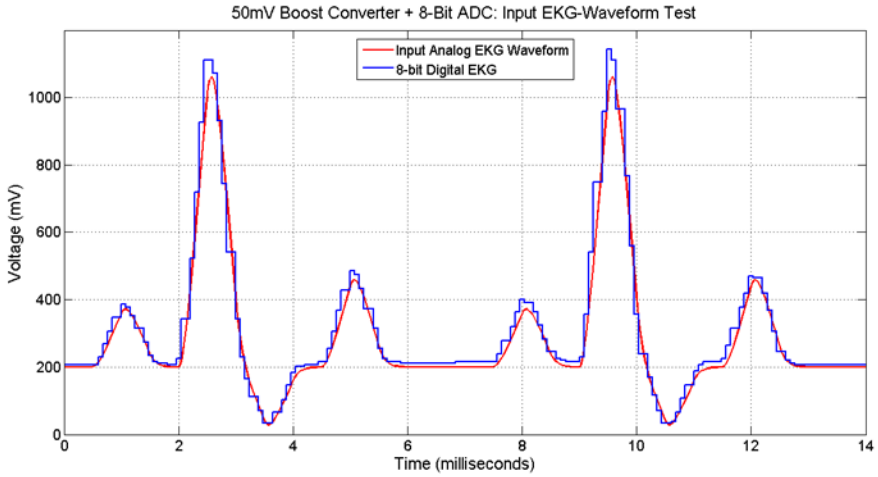

Figure B.12: The output of the DC/DC Converter plus 8-bit ADC when an input EKG waveform is applied is shown.

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