Design, Manufacture and Performance of Germanium Bipolar Transistors

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Abstract–Germanium NPN bipolar transistors have been manufactured using phosphorus and boron ion implantation processes. Implantation and subsequent activation processes have been investigated for both dopants. Full activation of phosphorus implants has been achieved with RTA schedules at 535°C without significant junction diffusion. However, boron implant activation was limited and diffusion from a polysilicon source was not practical for base contact formation. Transistors with good output characteristics were achieved with an Early voltage of 55V and common emitter current gain of 30. Both Silvaco process and device simulation tools have been successfully adapted to model the Ge BJT(bipolar junction transistor) performance.

Introduction

CMOS is the main technology for implementing digital circuits. As device dimensions are scaled these circuits can operate at higher frequencies. However, scaling is reaching its limits and further increase in integrated circuit performance requires the introduction of new materials. Silicon dioxide is no longer suitable as the gate dielectric and is being replaced with higher permittivity (high-k) metal oxide based dielectrics such as hafnium dioxide (HfO_2)[1,2]. To further improve performance strained silicon on insulator has been used to improve hole and electron mobility and reduce parasitic capacitance. The replacement of SiO_2 as the gate dielectric has lead to the research of other semiconductors for MOSFETs. Germanium with a higher electron mobility than in silicon and with the highest hole mobility has promise for higher performance RF circuits.

For RF circuits it is desirable to integrate passives along with the transistors. However, the quality factor of inductors is degraded with resistance losses in the handle substrates [3]. For mixed signal circuits employing both analogue and digital circuits, cross-talk from the digital part to the sensitive analogue circuits can be an important issue [4]. Therefore, many special purpose RF circuits are implemented in silicon on sapphire (SOS) technology. For higher performances RF circuits germanium on sapphire (GeOS) technology is being investigated [5]. However, for many analogue circuits, bipolar transistors are preferred. For applications requiring low noise amplifiers the MOS transistors are considered to be too noisy. Most of this noise comes from the fast interface states at the gate dielectric silicon interface. In the case of germanium MOS transistors the density of interface states will probably be greater than for silicon. It is therefore necessary for rf and millimetre wave integrated circuits (MMICs) to investigate the fabrication of bipolar transistors in germanium. The original germanium transistors

employed alloy junctions,[6,7] but such technology is unlikely to give the dimension control required for current devices. It is therefore essential to investigate the manufacture of Ge BJTs using process steps normally employed in a silicon foundry.

Transistor Design And Background Technology

The process design for a germanium bipolar transistor is very different from that of a silicon transistor. For the latter, the diffusion of the acceptor boron is relatively fast compared to that for donor impurities. This has facilitated the use of an extended polysilicon base contact with a self-aligned polysilicon emitter. The acceptor concentration at the polysilicon-crystalline silicon base contact is enhanced by out-diffusion of boron from the heavily doped polysilicon. The main difficulty is in avoiding enhanced diffusion of the p-base during emitter implant anneal. In contrast the diffusion of donor impurities in germanium is fast, but that of acceptors is very slow [8]. Initial tests on the out-diffusion of boron from ion implanted polysilicon were carried out to check the feasibility of such a process. Polysilicon layers 0.3 μm thick were deposited on germanium at 580°C and implanted with a dose of $5\times10^{15}cm^{-2}$ boron at an energy of 30 keV. A 0.5 μm APCVD oxide was deposited front and back to avoid surface breakup and minimise out-diffusion during drive-in at 800°C. The profiles of boron after 6 hrs and 11 hrs drive-in as determined by Secondary Ion Mass Spectrometry (SIMS) are shown in Fig.1.

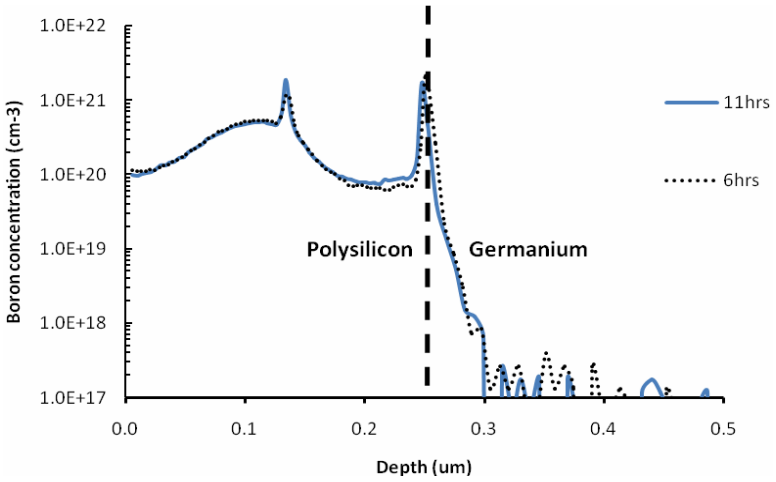

Figure 1. Boron diffusion from polysilicon to germanium

It can be seen from the SIMS results that the in-diffusion of boron into the germanium substrate is very small. Thus for the initial transistor designs it was decided to employ a very basic structure as shown in Fig. 2.

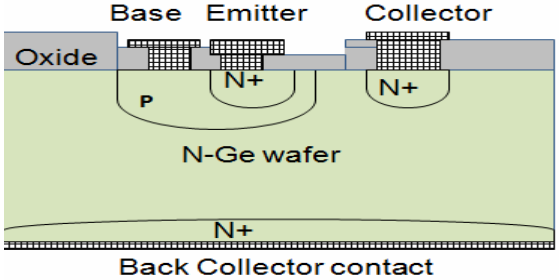

Figure 2. Cross-section of the bipolar transistor

The structure employs an n-type germanium substrate for the collector, a boron implanted base region and a phosphorus implanted emitter. The emitter stripes were 18μm wide with lengths of 18, 36 and 54μm and the base regions were 45μm wide with lengths of 34, 56 and 68μm. A common collector is employed for the transistors and it can be contacted globally at the back of the wafer or at localized surface contacts. To achieve an emitter-base breakdown voltage of ~2V and to minimise base series resistance, the targeted average base concentration was $3\text{-}5\times10^{17}cm^{-3}$. To avoid premature emitter-base breakdown voltage at the oxide interface of the emitter-base junction it was necessary to keep the surface concentration of boron at, or below $5\times 10^{17}cm^{-3}$. Since boron diffusion in germanium is negligible, it was decided to employ two implant energies for the boron. One higher energy boron implant was used to give the desired base doping under the emitter and an additional lower energy implant was used to give a high concentration at the base contact.

High dose phosphorus implants in germanium which give a concentration maximum above the equilibrium solid solubility limit of $2\times10^{20}cm^{-3}$ can lead to phosphorus complexes and precipitates giving a low level of activation [9]. The insoluble phosphorus complexes formed are stable at temperatures up to 550°C. Redistribution of the phosphorus is extremely fast as the solid phase epitaxy takes place. For phosphorus concentrations above the intrinsic carrier level a concentration dependent diffusion takes place. To avoid the formation of phosphorus complexes and rapid diffusion, a phosphorus dose of $1\times10^{15}cm^{-2}$ was implanted at an energy of 100keV. Post implant anneals were carried out for 2 hrs at temperatures of 535°C, 600°C and 680°C. The spreading resistance analysis (SRP) plots for the chemical phosphorus in the germanium samples are shown in Fig. 3.

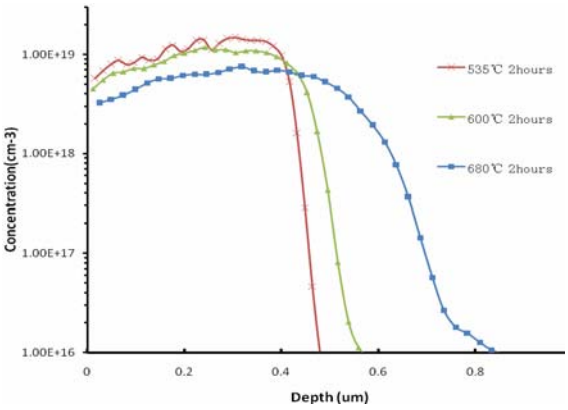

Figure 3. SRP of phosphorus profiles in germanium diffused at 535°C, 600°C and 680°C

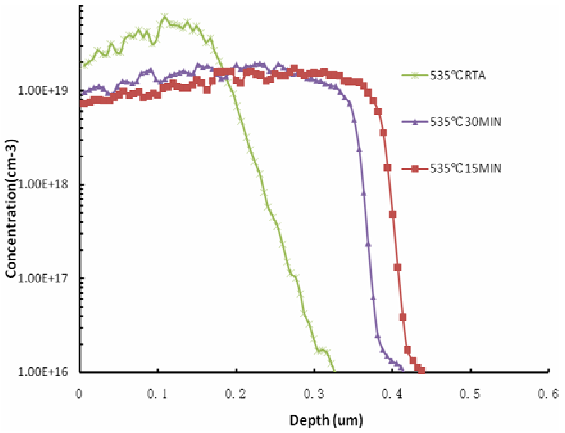

Figure 4. SRP of phosphorus profiles in germanium diffused at 535°C for different anneal time.

Since the intrinsic carrier density is of the order of 10^{18} cm^{-3} non-Gaussian profiles with abrupt concentration falls at a concentration of $7\times10^{18}cm^{-3}$ are observed for the lower thermal budget diffusions with $C_{max} \geq 10^{19}cm^{-3}$. For the 680°C anneal the maximum concentration has fallen to $7\times10^{18}cm^{-3}$ the profile is Gaussian like and the fall to lower concentrations is less steep. The depth for a concentration of $10^{17}cm^{-3}$ is of the order of 0.5 μm for 535°C diffusion. This is considered on the deep side for an emitter implant considering that the boron base does not diffuse. Thus it was decided to study

the phosphorus profiles after activation at 535°C for reduced times. Phosphorus profiles obtained by SRP for the phosphorus implants annealed for 30 mins, 15mins and for 1 min RTA are given in Fig. 4.

The furnace anneal profiles for 15 and 30 mins show box like profiles associated with concentration dependent diffusion with steep drop-offs from $7\times10^{18}cm^{-3}$. The concentration drops to $10^{17}cm^{-3}$ close to 0.4 μm from the surface, which is considered to be still too deep. The RTA 535°C 1 min anneal has produced a concentration maximum of $5\times10^{19}cm^{-3}$ and a fall to $10^{17}cm^{-3}$ at a depth of 0.3μm. To check the degree of activation of the phosphorus implant for the RTA anneal, spreading resistance analysis was also carried out. The phosphorus concentration obtained by SRP and SIMS analysis are given in Fig. 5 and confirm that high level activation of the phosphorus has been achieved.

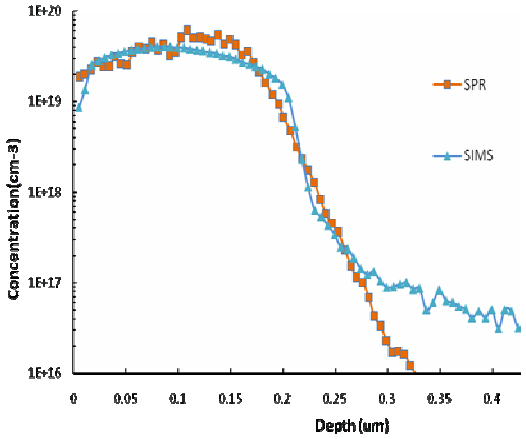

Figure 5. A comparison of the electrically active phosphorus profile as determined by SRP with the chemical phosphorus profile obtained from SIMS

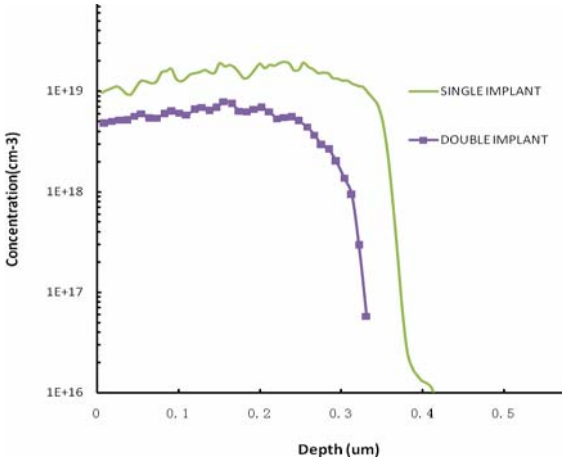

Figure 6. Concentration of phosphorus obtained by SRP analysis for phosphorus implant into virgin Ge and previously boron implanted substrate.

It has generally been found that the active concentration of phosphorus in germanium is less than the equilibrium value while that for boron is higher. It is known that point defects in boron can act as acceptors and that it is the residual defects that lead to reduction in active phosphorus[10]. It was therefore decided to compare the active phosphorus achieved from implantation into a virgin germanium substrate with one that had been given the proposed boron implantation for the transistor base. The concentration profiles determined by spreading resistance are given in Fig. 6.

It can be seen that the reduction in phosphorus concentration is greater than that obtained by a simple subtraction of the implanted boron profile. The reduction is therefore attributed to some de-activation of the phosphorus through insoluble complexes formed from residual damage after the boron activation. A comparison of the active boron concentration as determined by SRP with the chemical boron concentration as determined by SIMS is given in Fig. 7. The boron implant was subjected to a post implant anneal at 535°C for 2 hrs while covered with a 0.2 μm layer of PECVD oxide. The boron implant of 2×10^{13} cm^{-2} at 160keV + 2×10^{13} cm^{-2} at 70keV is below that required to form an amorphous layer of $\sim10^{14}cm^{-2}$. The activation for the boron is about 60% of the implant dose.(From week8 report No dopant loss for the laser and furnace

annealed sample at 525C for 30 min. furnace only sample exhibits a severe dose loss of about 55%. This clear difference of the dose loss behavior between the two cases above is indicative of the important role that initial implant damage plays.)

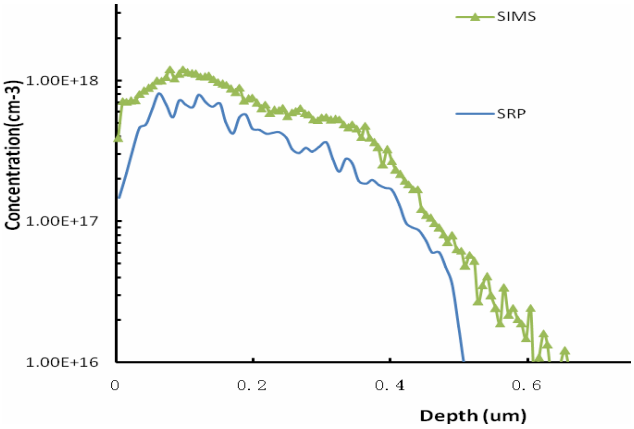

Figure 7, A comparison of the electrically active boron profile as determined by SRP with the chemical boron profile obtained from SIMS

Transistor Fabrication

N-type germanium (100) orientation wafers, with an antimony concentration of 9×10^{15} cm^{-3} were obtained from Umicore, Belgium. The wafers were cleaned by HF water cycling before 1µm of PECVD SiO_2 was deposited on the front and a 0.1µm layer on the back. The window for the base implantation was opened by photolithography and dry etching. A 0.1µm thick PECVD oxide was deposited to protect the base region. The base was formed by implanting boron through the thin oxide with a dose of $2\times10^{13}cm^{-2}$ at 160 keV and a dose of $2\times10^{13}cm^{-2}$ at 70 keV. A 0.4µm PECVD oxide was deposited at 300°C before the boron was activated by annealing at 535°C for 2 hrs. The emitter and collector contact windows were patterned in the oxide layer by wet etching. A phosphorus dose of $1\times10^{15}cm^{-2}$ was implanted at an energy of 100 keV. The back of the germanium was then given a similar phosphorus implant to provide an ohmic collector contact. A 0.2µm PECVD oxide was deposited before the phosphorus was given an RTA at 535°C for 60 sec. The contact windows to emitter, base and collector were opened by photolithography and wet etching before sputter deposition of 0.5µm of aluminium. The aluminium was patterned by wet chemistry and a 0.2µm layer of aluminium was then deposited on the back of wafer. The devices were annealed at 200°C for 20mins to reduce the sputtering damage. This low temperature was used in order to avoid damage to the diffused junctions by interaction between the Ge and the Al. The SRP profiles for emitter and base regions are shown in Figure 8.

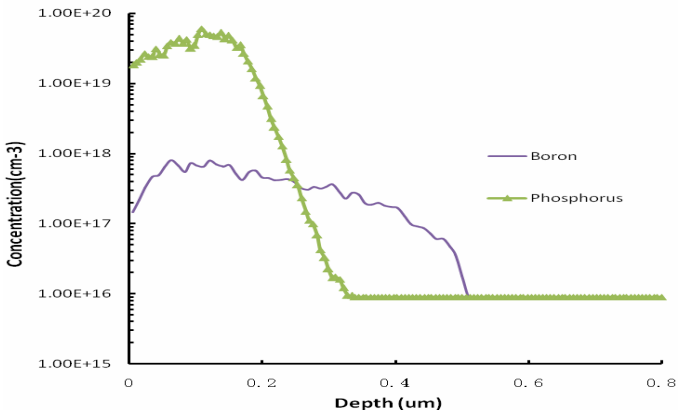

Figure 8 Active impurities profile obtained by SRP for emitter and base regions

Device Characteristics

The I-V characteristic of an emitter–base diode with an emitter 18µm × 18µm is given in Fig 9.

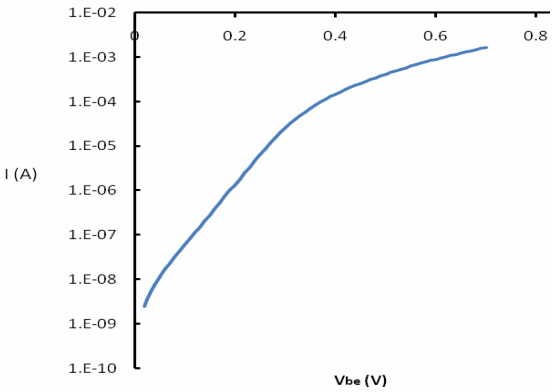

Figure 9. I-V characteristic for emitter-base diode.

The series resistance is determined from log I vs V curves to be ~140Ω. The ideality factor n = 1.17 at 0.1V and the reverse breakdown voltage was 3.5 V. The log I vs V characteristic for a base – collector (substrate) diode is given in Figure 10(a). The ideality factor n=1.16. The series resistance for this diode with a base area of 34µm × 45µm is 12Ω. This indicates that the series resistance of E-B diode is mainly due to the emitter to aluminium contact. Thus for an emitter contact window of 6µm × 6µm the specific contact resistivity of aluminium to n+ Germanium is ~ 5×10^{-5} Ω.cm^2. The base-collector breakdown voltage shown in Figure 10(b) is ~15V. Both emitter/base and base/collector diodes show good characteristics with a turn on voltage of 0.35V.

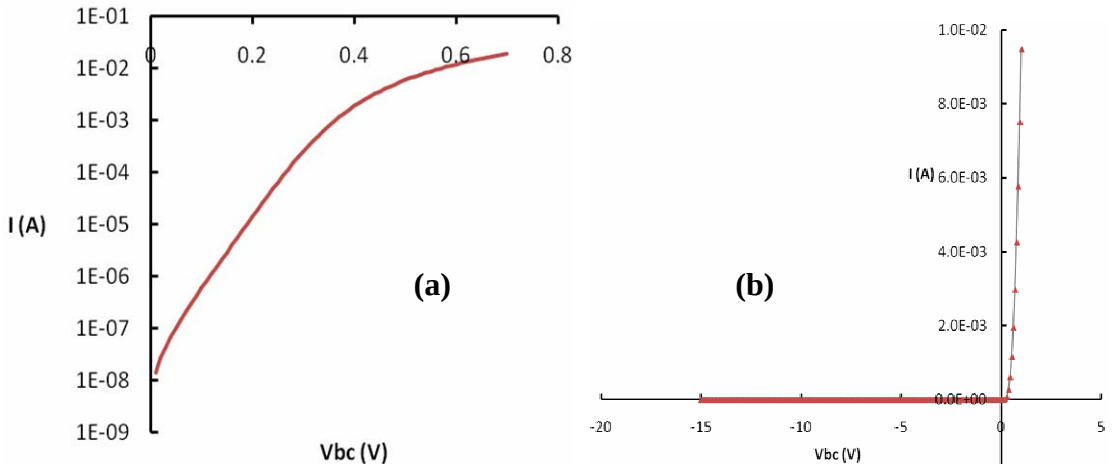

Figure 10 Base to Collector (substrate) diode (a) Log I vs V characteristic and (b) I-V characteristic under reverse bias

The transistor I_C - V_{CE} characteristics are shown in Figure 11. The transistor output impedance in the forward active mode is high with a value of the order of 7×10^4 Ω. The Early voltage for the transistor is 55V. The common emitter curent gain for a transistor is given in Fig. 12 as a function of collector current. The gain increases with collector current indicating a high recombination current in the emitter-base depletion region. The collector – emitter breakdown voltage V_{CEO} is 8V.

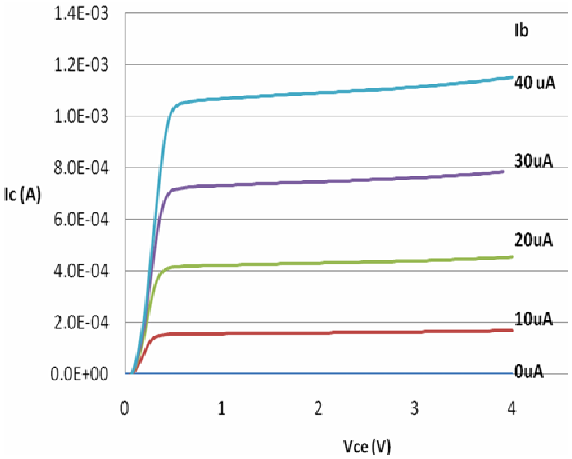

Figure 11 The collector current-voltage characteristics for a transistor.

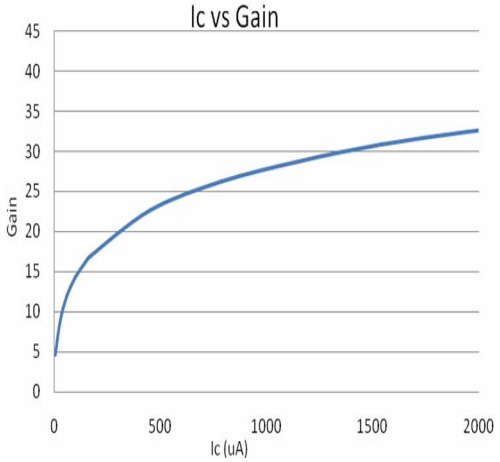

Figure 12. Common emitter current gain β for a transistor with collector current.

Process and Device Simulation

Process and device simulation has been undertaken. Process parameters concerning implantation into Ge, and dopant diffusivity in Ge were input to Ssuprem3 to support the design of the process flow described. The comparisons of SIMS and simulation for both phosphorus and boron are given in Fig. 13.

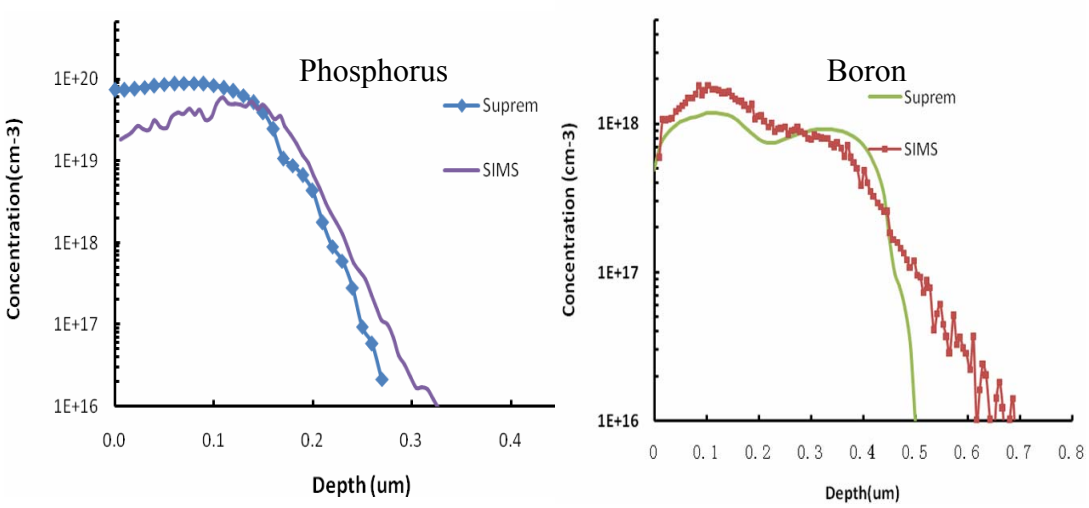

Figure 13 Comparisons of the dopant profile obtained by SIMS and Suprem3 simulation.

Since there is discrepancy between SIMS and SRP profiles for boron, it was decided to use SRP profiles for both dopants as input to Atlas to simulate transistor electrical characteristics. Key parameters have been defined for Ge which include bandgap, electron and hole density of states, electron and hole mobilities, and generation/recombination lifetimes. The I-V characteristic of emitter–base diode was simulated and is compared with measured data in figure 14. The comparison of Gummel plots are also provided in figure 15. It can be seen that the simulation gives a reasonably good agreement with the actual measurements.

Simulation of transistor output characteristics show good agreement with a slightly higher current gain of 35 as shown in figure 16. The frequency response of the transistor has also been simulated and as shown in figure 17 a maximum cut-off frequency of ~7GHz is obtained.

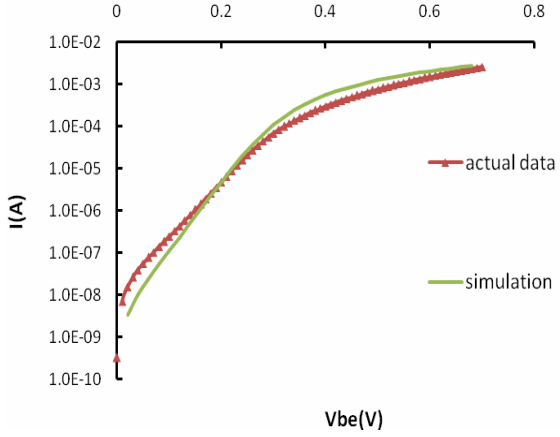

Fig14 I-V characteristics for the base-emitter diode

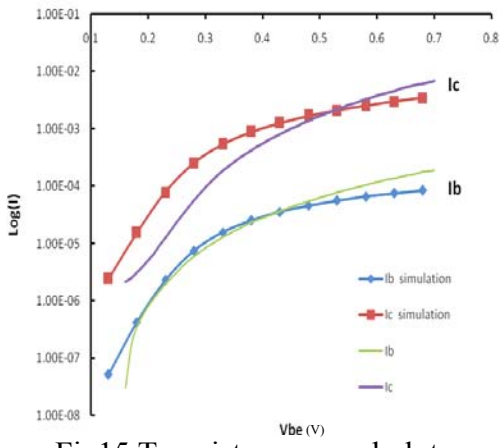

Fig15 Transistor gummel plot

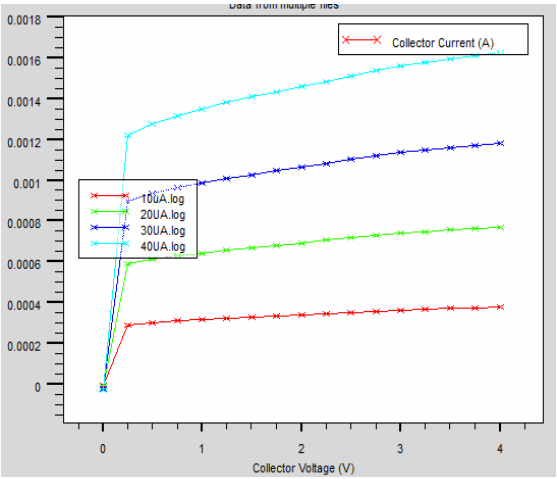

Fig 16.Simulation of the transistor output characteristics

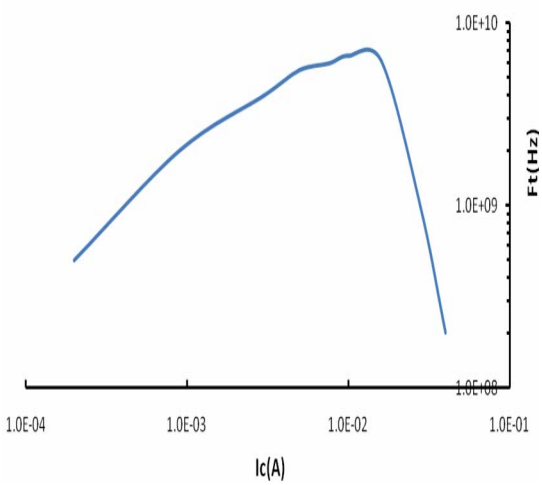

Fig17. Variation of cut-off frequency with collector current.

For comparison purpose, the frequency responses of a silicon BJT and a germanium BJT designed with same parameters are given in figure 18. It can be seen that the f_t of Ge is 5 times higher than that of Si, which is mainly due to higher electron mobility in Ge.

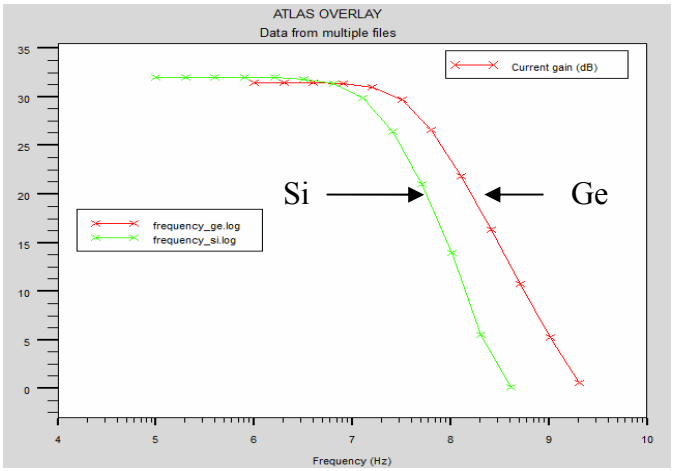

Fig18. Comparison of Frequency response for Si BJT and Ge BJT

Conclusions

A bipolar manufacturing process has been established with very low temperature processing of germanium. Activation processes have been investigated for both dopants. Full activation of phosphorus implants has been achieved with RTA schedules at 535°C without significant junction diffusion. However, only 60% activation of boron was achieved which increases the recombination current at the emitter-base junction reducing the gain at low current drive. Ssuprem3 simulation has been adapted to aid design of emitter and base doping profiles with reasonable accuracy. Atlas simulation has also been successfully adapted to model the Ge BJT performance. Transistors with good output characteristics, an Early voltage of 55V and a common emitter current gain of 30 have been produced. All the above results are achieved on a low temperature process and a non-optimized structure. They are highly encouraging for germanium transistor applications in RF circuits.

Acknowledgment

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References

1. S. Kubicek et al., *Low VT CMOS using doped Hf-based oxides, TaC-based Metals and Laser-only Anneal*, IEDM Tech. Dig., 2007.
2. C.S. Park et al., *Achieving Low Vt (<-0.3V) and Thin EOT (~1.0nm) in Gate First Metal/High-k pMOSFET for High Performance CMOS Applications,* Proc. VLSI-TSA (2008), pp. 154-155.
3. I Lagnado and PR de la Houssaye, *Silicon on sapphire*, in Properties of Crystalline Silicon, Ed R Hull.
4. P.Baine, M.Jin, H.S.Gamble, B.M.Armstrong, D.Linton and F.Mohammed, *Cross-talk suppression in SOI substrates*, Solid State Electronics V9.N0.9,pp1461-1465,Sept. 2005.
5. PT Baine, HS Gamble, BM Armstrong, DW McNeill, S.J.N Mitchell, YH Low, PV Rainey , *Germanium on Sapphire By Wafer Bonding,* Solid State Electronics 52 pp1840–1844 2008
6. R. Dahlberg and D. Gerstner, *Planar Technik fur Germanium*, Internat'l Elek. Rundschau, 21No2 (1967) p27.
7. F.H. Dill, A.S. Farber and H.N. Yu, *Silicon vs. germanium in picosecond logic circuits*, Internat'l Solid-State Device Conf. Philadelphia 1967
8. P. Gansauge, Double *Diffused High-Speed Germanium Transistors*, IEEE Trans. Elect. Dev. ED-15(10) p728 (1968)
9. A. Satta, E. Simeon, R. Duffy, T. Janssens, T. Clarysse, A. Benedetti, M. Meuris and W. Vandervorst, *Diffusion, activation, and regrowth behavior of high dose P implants in Ge*, Appl. Phys. Letts. 88, 162118 (2006)
10. Omachi Y. Nishioka T. and Shinoda Y, *The heteroepitaxy of Ge on Si(100) by vacuum evaporation,* Appl. Phys. 54(9), 5466-5469(1983)