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A. Kranti, C.-W. Lee, I. Ferain, R. Yan, N. Akhavan, P. Razavi, R. Yu, G.A. Armstrong and J.-P. Colinge

The design of a 6T SRAM cell with 20 nm junctionless (JL) MOSFETs is reported. It is shown that a 6T SRAM cell designed with JL MOSFETs achieves a high static noise margin (SNM) of 185 mV, retention noise or hold margin (RNM) of 381 mV and writability current (I_{WR}) of 33 μA along with a low leakage current (I_{LEAK}) of 2 pA at a supply voltage (V_{DD}) of 0.9 V for cell and pull-up ratios of 1. Results offer a new opportunity to design future SRAM cells with nanoscale JL MOSFETs.

Introduction: Lateral doping gradient or abruptness of source/drain (S/D) extension regions is a key process/device parameter which significantly impacts the S/D series resistance as well as short-channel effects (SCEs) in nanoscale MOS devices and is a crucial technological factor limiting device scaling into the nanoscale regime. To overcome the technological difficulties in the formation of ultra-sharp S/D extension regions in nanoscale devices, the concept of the junctionless (JL) MOS transistor in silicon-on-insulator (SOI) and bulk technologies has been recently reported [1–3]. The JL transistor is an MOS device where the channel doping is the same as that of heavily doped S/D regions. The use of identical doping in the S/D and channel regions circumvents the necessity of controlling S/D gradients in the extension regions near the gate edge. In this work we analyse the performance of a 6T SRAM cell comprising JL MOSFETs and demonstrate its superiority over conventional 6T SRAM with inversion mode devices.

Simulations: JL [1–3] nMOS and pMOS devices analysed in this Letter were simulated using the Lombardi mobility model in ATLAS simulator [4], with gate length (L_g) of 20 nm, oxide thickness (T_{ox}) of 1 nm, width (W_g) of 60 nm, film thickness (T_{si}) of 7 nm, nMOS gate workfunction (Φ_{mn}) = 5.02 eV and pMOS gate workfunction (Φ_{mp}) = 4.52 eV with a channel doping of 1×10^{19} cm^{-3}. Additional S/D implantation of 1×10^{20} cm^{-3} with an underlap (spacer) region of 10 nm was utilised to improve current drive for JL devices.

Results: A JL MOSFET [1–3] is a device with the same doping in channel and source/drain (S/D) regions. Simulated current (I_{ds}) – voltage (V_{gs}) curves of 20 nm JL MOSFETs with channel doping of 1×10^{19} cm^{-3} (Fig. 1*a*) demonstrate excellent characteristics: high on–off current ratio ~10^8 (nMOS) and 10^7 (pMOS) with a subthreshold slope (*S*-slope) and drain induced barrier lowering (DIBL) parameter of 64 mV/dec and ~ 40 mV/V, respectively.

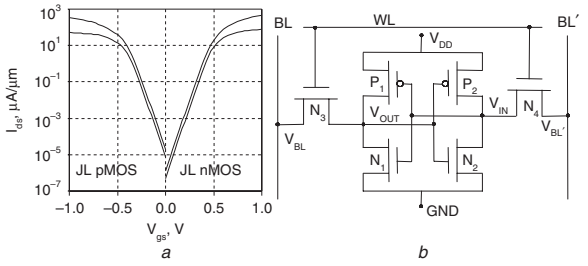

Fig. 1 *JL MOSFET for SRAM cell*

a I_{ds} – V_{gs} curves for nMOS and pMOS JL MOSFETs at drain voltages (V_{ds}) of 50 mV and 1 V
b Schematic diagram of 6T SRAM cell

Owing to the N^+–N^+–N^+ (or P^+–P^+–P^+) design of the MOSFET, no lateral S/D junction (along the current flow path) is formed and no diffusion takes place, which relaxes the processing thermal budget and the need for developing ultra fast annealing techniques. The thin silicon film (= 7 nm) ensures full depletion, resulting in low leakage current ~10^{-6} μA/μm (nMOS) and 10^{-5} μA/μm (pMOS) and full device functionality is observed even in the absence of reverse biased lateral pn-junctions.

A 6T SRAM cell (Fig. 1*b*) was designed with identical structural parameters for nMOS and pMOS JL devices, resulting in cell ratio $CR = (W_g/L_g)_{N1,N2}/(W_g/L_g)_{N2,N4}$ and pull-up ratio $(PR = (W_g/L_g)_{P1,P2}/(W_g/L_g)_{N2,N4})$ of 1. Various SRAM metrics are defined in [5]. The butterfly curves for hold and read modes (Figs. 2*a* and *b*) show an impressive RNM > $0.4V_{DD}$ i.e. 381 and 296 mV and a high SNM (~ $0.2V_{DD}$) of 185 and 165 mV at supply voltage (V_{DD}) of 0.9 and 0.7 V, respectively. Owing to the high threshold voltages and relative immunity from SCEs in JL devices [1], the ratio of RNM to SNM increases from 0.48 at V_{DD} = 0.9 V to 0.56 at V_{DD} = 0.7 V. Higher RNM, SNM and RNM/SNM values at lower V_{DD} values demonstrate the potential of the JL SRAM cell for low voltage operation. Read/write N-curves (Figs. 2*c* and *d*) demonstrate full SRAM stability along with I_{WR} of 33 μA (or 14 μA) for V_{DD} of 0.9 V (or 0.7 V).

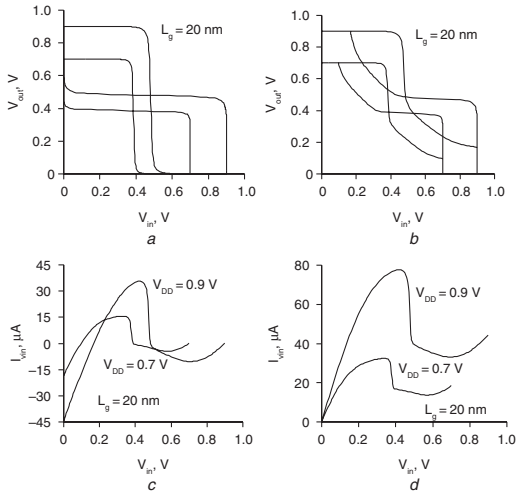

Fig. 2 *JL SRAM performance metrics*

a Butterfly curve for HOLD mode
b Butterfly curve for READ mode
c N-curve for READ mode
d N-curve for WRITE mode

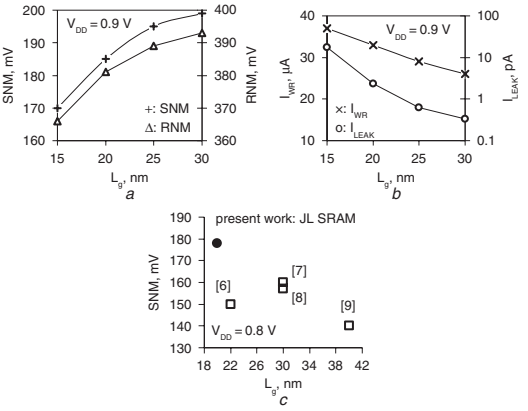

Fig. 3 *Dependence of JL SRAM metrics on gate length*

a SNM and RNM on gate length
b Writability and leakage current
c Comparison of SNM predicted by JL SRAM with published data for conventional inversion mode 6T SRAM cell
+ SNM
Δ RNM
× I_{WR}
o I_{LEAK}
□ Experimental SNM values for inversion mode SRAM cells [6–9]
• SNM value for JL SRAM cell

As shown in Figs. 3*a* and *b*, SNM and RNM reduce with gate length owing to short channel effects. However, the performance of the JL SRAM cell can be maintained down to L_g = 15 nm, with SNM ~ 170 mV (~ 0.2 V_{DD}) and RNM ~ 365 mV (~ 0.4 V_{DD}), SNM/RNM ~ 0.47, along with a high ratio of write-ability to leakage current (I_{WR}/I_{LEAK}) of ~10^6 (I_{WR} of 38 μA and I_{LEAK} of 18 pA). A twofold (15 to 30 nm) increase in gate length improves I_{LEAK} by an order of magnitude at the expense of a minor degradation in I_{WR} from 38 to 26 μA. The leakage current can be maintained below 1 pA for L_g = 25 nm without any significant degradation in other performance metrics. As shown in Fig. 3*c*, the proposed JL SRAM design achieves SNM values significantly higher than published [6–9] for inversion mode (IM) FinFET-based

SRAM cells. While performance metrics in IM devices can be improved by adopting an underlap S/D design in which S/D doping concentration sharply decreases by 5 decades i.e. 10^{20} cm^{-3} to 10^{15} cm^{-3} over a few nanometres [5]. Such an approach will require precise control of S/D doping gradient in the S/D extension regions and additional process complexity which may be extremely difficult to optimise. A JL MOS-based SRAM design exhibits improved performance along with a simpler fabrication process.

Conclusion: An ultra-low leakage (~2 pA) JL 6T SRAM cell design exhibiting high SNM values ($> 0.2V_{DD}$) along with RNM of $\sim 0.4V_{DD}$, without compromising cell write-ability, has been presented. A JL device design offers a new paradigm for improving 6T SRAM performance metrics.

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References

1 Lee, C.-W., Afzalian, A., Dehdashti Akhavan, N., Yan, R., Ferain, I., and Colinge, J.-P.: 'Junctionless multigate field-effect transistor', *Appl. Phys. Lett.*, 2009, **94**, (5), article no. 053511
2 Colinge, J.-P., *et al.*: 'Nanowire transistors without junctions', *Nature Nanotechnology*, 2010, **5**, (3), pp. 225–229
3 Kranti, A., *et al.*: 'Junctionless nanowire transistor (JNT): properties and design guidelines'. Proc. European Solid State Device Research Conf. (ESSDERC), Seville, Spain, 2010, pp. 357–360
4 ATLAS Users Manual, Silvaco, 2009
5 Rashmi, Kranti, A., and Armstrong, G.A.: '6-T SRAM cell design with nanoscale double-gate SOI MOSFETs: impact of source/drain engineering and circuit topology', *Semicond. Sci. Technol.*, 2008, **23**, (7), article no. 075049
6 Guillorn, M., *et al.*: 'Trigate 6T SRAM Scaling to 0.06 μm^2'. Proc. Int. Electron Devices Meeting (IEDM) Technical Digest, Baltimore, MD, USA, 2009, pp. 961–964
7 Collaert, N., *et al.*: 'Low-voltage 6T FinFET SRAM cell with high SNM using HfSiON/TiN gate stack, fin widths down to 10 nm and 30 nm gate length'. Proc. Int. Conf. Integrated Circuit Design and Technology (ICICDT), Grenoble, France, 2008, pp. 59–62
8 Mérelle, T., *et al.*: 'First observation of FinFET specific mismatch behavior and optimization guidelines for SRAM scaling'. Proc. Int. Electron Devices Meeting (IEDM) Technical Digest, San Francisco, CA, USA, 2008, pp. 241–244
9 Veloso, A., *et al.*: 'Demonstration of scaled 0.099 μm^2 FinFET 6T-SRAM cell using full-field EUV lithography for (sub-)22nm node single-patterning technology'. Proc. Int. Electron Devices Meeting (IEDM) Technical Digest, Baltimore, MD, USA, 2009, pp. 301–304